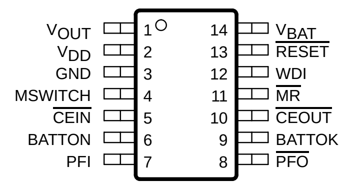
features

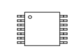
- **Supply Current of 40 μA (Max)**
- **Precision Supply Voltage Monitor**
  - **2.0 V, 2.5 V, 3.3 V, 5.0 V**
  - **Other Versions on Request**
- **Watchdog Timer With 800-ms Time-Out**
- **Backup-Battery Voltage Can Exceed V_{DD}**
- **Power-On Reset Generator With Fixed 100-ms Reset Delay Time**
- **Battery OK Output**
- **Voltage Monitor for Power-Fail or Low-Battery Monitoring**
- **Manual Switchover to Battery-Backup Mode**
- **Chip-Enable Gating –3 ns (at V_{DD} = 5 V) Max. Propagation Delay**
- **Manual Reset**
- **Battery Freshness Seal**
- **14-Pin TSSOP Package**
- **Temperature Range . . . –40°C to 85°C**

typical applications

- **Fax Machines**
- **Set-Top Boxes**
- **Advanced Voice Mail Systems**
- **Portable Battery Powered Equipment**
- **Computer Equipment**
- **Advanced Modems**
- **Automotive Systems**
- **Portable Long-Time Monitoring Equipment**
- **Point of Sale Equipment**

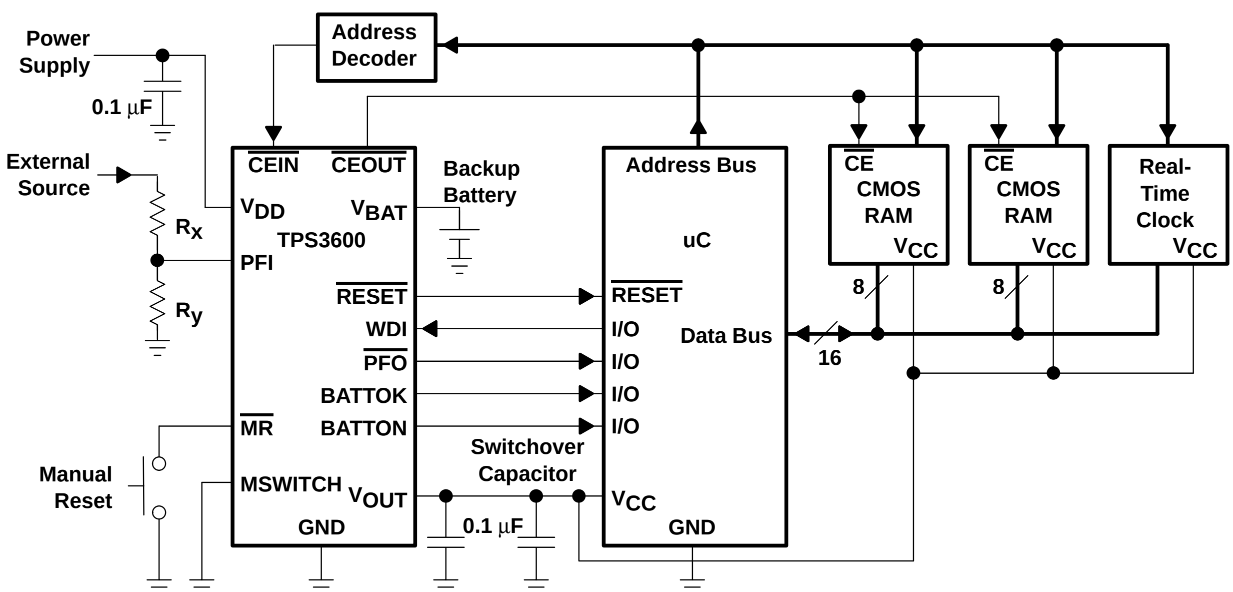
TSSOP (PW) Package
(TOP VIEW)





ACTUAL SIZE
(5,10mm x 6,60mm)

typical operating circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description

The TPS3600 family of supervisory circuits monitor and control processor activity. In case of power-fail or brownout conditions, the backup-battery switchover function of TPS3600 allows to run a low-power processor and its peripherals from the installed backup battery without asserting a reset beforehand.

During power on, $\overline{\text{RESET}}$ is asserted when the supply voltage (V_{DD} or V_{BAT}) becomes higher than V_{res}. Thereafter, the supply voltage supervisor monitors V_{OUT} and keeps $\overline{\text{RESET}}$ output active as long as V_{OUT} remains below the threshold voltage (V_{IT}). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. This delay timer starts its time-out, after V_{OUT} has risen above the threshold voltage (V_{IT}). In case of a brownout or power failure of both supply sources, a voltage drop below the threshold voltage (V_{IT}) get detected and the output becomes active (low) again.

The product spectrum is designed for supply voltages of 2 V, 2.5 V, 3.3 V, and 5 V. The circuits are available in a 14-pin TSSOP package. They are characterized for operation over a temperature range of –40°C to 85°C.

PACKAGE INFORMATION

T_A	DEVICE NAME
–40°C to 85°C	TPS3600D20
	TPS3600D25
	TPS3600D33
	TPS3600D50

ordering information application specific versions (see Note)

TPS360 0 D 20 PW R

- **R** — **Reel**
- **PW** — **Package**
- **20** — **Nominal Supply Voltage**
- **D** — **Nominal BATTOK Threshold Voltage**
- **0** — **Functionality**
- **TPS360** — **Family**

DEVICE NAME	NOMINAL VOLTAGE, V_{NOM}
TPS3600x20 PW	2.0 V
TPS3600x25 PW	2.5 V
TPS3600x33 PW	3.3 V
TPS3600x50 PW	5.0 V

DEVICE NAME	NOMINAL BATTOK THRESHOLD VOLTAGE, V_{BOK}
TPS3600Dxx PW	V_{IT} + 7%
TPS3600Fxx PW†	V_{IT} + 6%
TPS3600Hxx PW†	V_{IT} + 8%
TPS3600Jxx PW†	V_{IT} + 10%

† For the application specific versions, please contact the local TI sales office for availability and lead time.

FUNCTION TABLES

$V_{DD} > V_{SW}$	$V_{OUT} > V_{IT}$	$V_{DD} > V_{BAT}$	MSWITCH	$\overline{MR}$	V_{OUT}	BATTON	$\overline{RESET}$	$\overline{CEOUT}$
0	0	0	0	0	V_{BAT}	1	0	DIS
0	0	0	0	1	V_{BAT}	1	0	DIS
0	0	0	1	0	V_{BAT}	1	0	DIS
0	0	0	1	1	V_{BAT}	1	0	DIS
0	0	1	0	0	V_{DD}	0	0	DIS
0	0	1	0	1	V_{DD}	0	0	DIS
0	0	1	1	0	V_{BAT}	1	0	DIS
0	0	1	1	1	V_{BAT}	1	0	DIS
0	1	0	0	0	V_{BAT}	1	0	DIS
0	1	0	0	1	V_{BAT}	1	1	EN
0	1	0	1	0	V_{BAT}	1	0	DIS
0	1	0	1	1	V_{BAT}	1	1	EN
0	1	1	0	0	V_{DD}	0	0	DIS
0	1	1	0	1	V_{DD}	0	1	EN
0	1	1	1	0	V_{BAT}	1	0	DIS
0	1	1	1	1	V_{BAT}	1	1	EN
1	1	0	0	0	V_{DD}	0	0	DIS
1	1	0	0	1	V_{DD}	0	1	EN
1	1	0	1	0	V_{BAT}	1	0	DIS
1	1	0	1	1	V_{BAT}	1	1	EN
1	1	1	0	0	V_{DD}	0	0	DIS
1	1	1	0	1	V_{DD}	0	1	EN
1	1	1	1	0	V_{BAT}	1	0	DIS
1	1	1	1	1	V_{BAT}	1	1	EN

$V_{BAT} > V_{BOK}$	BATTOK
0	0
1	1

CONDITION: $V_{OUT} > V_{DD(min)}$

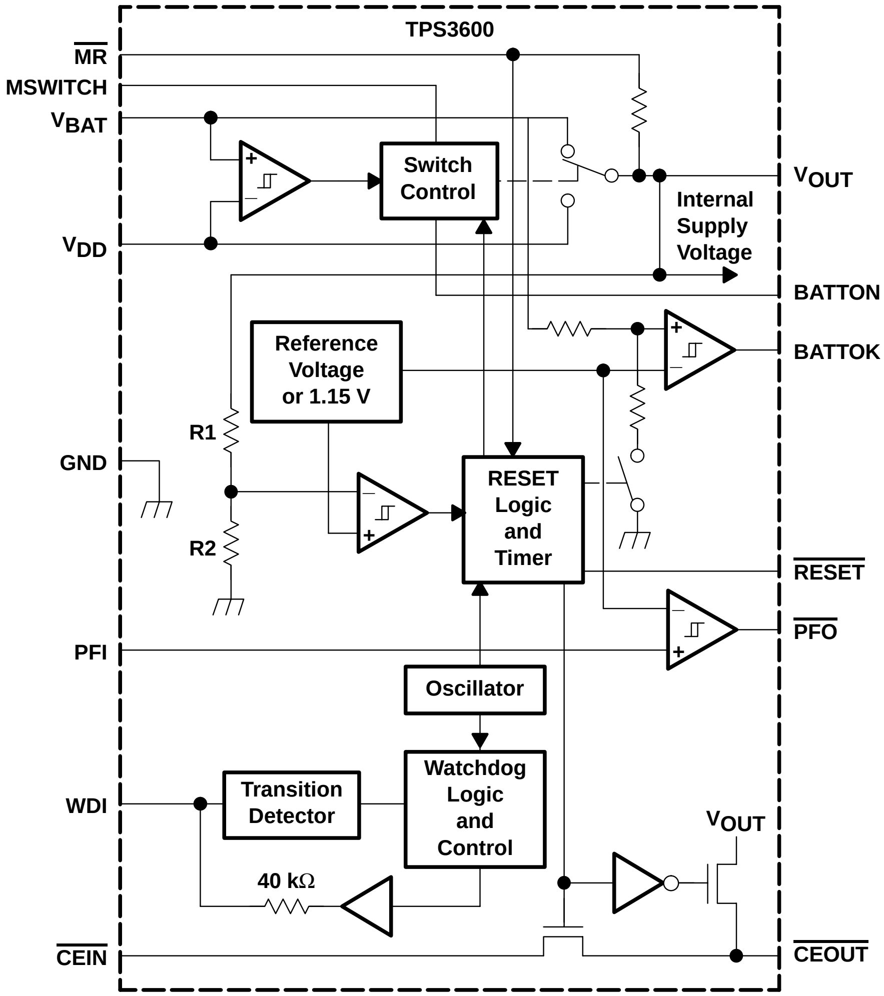
$\overline{CEIN}$	$\overline{CEOUT}$
0	0
1	1

CONDITION: Enabled

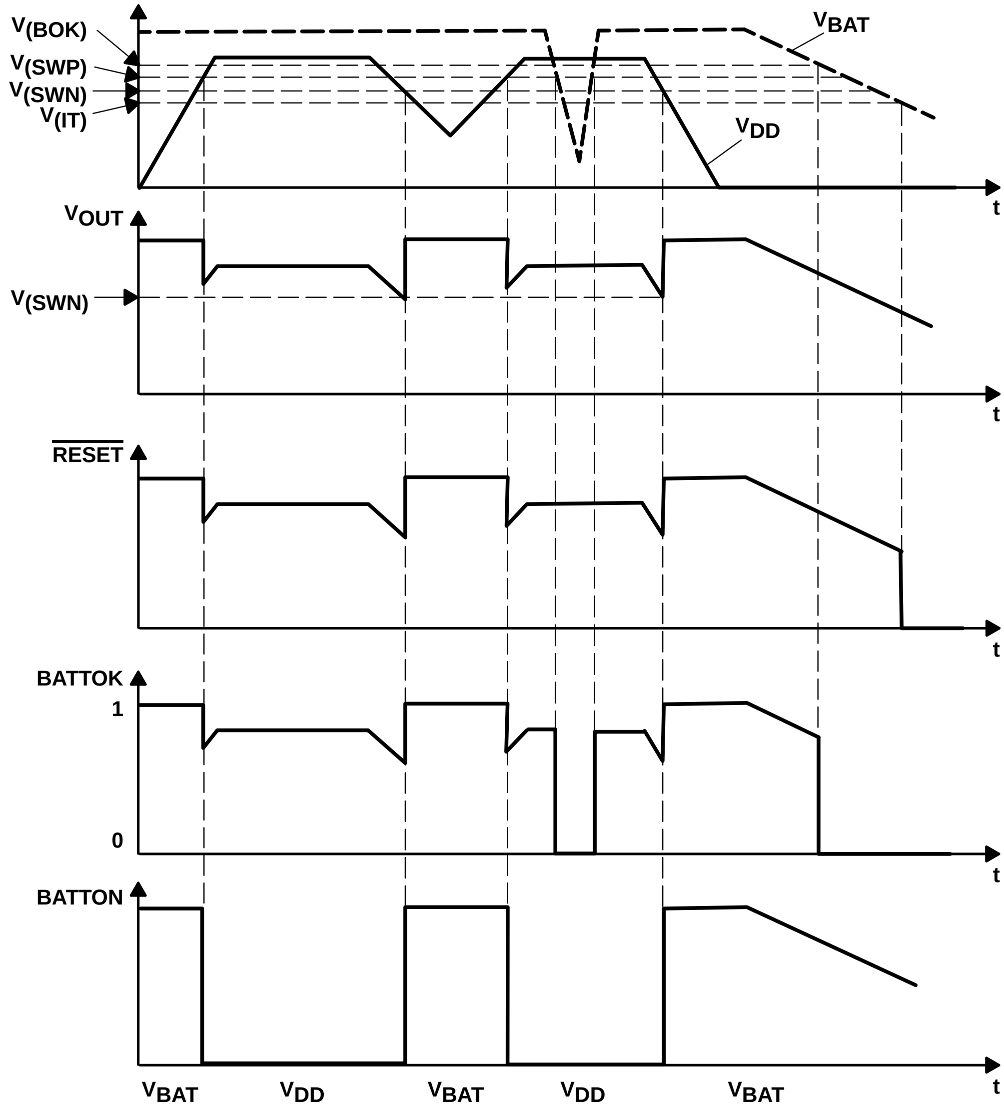
$PFI > V_{PFI}$	$\overline{PFO}$
0	0
1	1

CONDITION: $V_{OUT} > V_{DD(min)}$

functional schematic



timing diagram



NOTES: A. MSWITCH = 0, $\overline{MR}$ = 1
NOTES: B. Timing diagram shown under normal operation, not in freshness seal mode.

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
BATTOK	9	O	Battery status output
BATTON	6	O	Logic output/external bypass switch driver output
$\overline{\text{CEIN}}$	5	I	Chip-enable input
$\overline{\text{CEOUT}}$	10	O	Chip-enable output
GND	3	I	Ground
$\overline{\text{MR}}$	11	I	Manual reset input
MSWITCH	4	I	Manual switch to force device into battery-backup mode (connect to GND if not used)
PFI	7	I	Power-fail comparator input (connect to GND if not used)
$\overline{\text{PFO}}$	8	O	Power-fail comparator output
$\overline{\text{RESET}}$	13	O	Active-low reset output
V_{BAT}	14	I	Backup-battery input
V_{DD}	2	I	Input supply voltage
V_{OUT}	1	O	Supply output
WDI	12	I	Watchdog timer input

detailed description

battery freshness seal

The battery freshness seal of the TPS3600 family disconnects the backup battery from the internal circuitry until it is needed. This ensures that the backup battery connected to V_{BAT} should be fresh when the final product is put to use. The following steps explain how to enable the freshness seal mode:

1. Connect V_{BAT} ($V_{BAT} > V_{BAT(min)}$)
2. Ground $\overline{\text{PFO}}$
3. Connect PFI to V_{DD} or PFI > $V_{(PFI)}$
4. Connect V_{DD} to power supply ($V_{DD} > V_{IT}$)
5. Ground $\overline{\text{MR}}$
6. Power down V_{DD}
7. The freshness seal mode is entered and pins $\overline{\text{PFO}}$ and $\overline{\text{MR}}$ can be disconnected.

The battery freshness seal mode is disabled by the positive-going edge of $\overline{\text{RESET}}$ when V_{DD} is applied.

BATTOK output

This is a logic feedback of the device to indicate the status of the backup battery. The supervisor checks the battery voltage every 200 ms with a voltage divider load of approximately 100 KΩ and a measure cycle on-time of 25 µs. This measurement cycle starts after the reset is released. If the battery voltage V_{BAT} is below the negative-going threshold voltage $V_{(BOK)}$, the indicator BATTOK does a high-to-low transition. Otherwise, its status remains to the V_{OUT} level.

Table 1. Typical Values for BATTOK Indication

SUPERVISOR TYPE	V_{IT} TYP	V_{BOK} MIN	V_{BOK} TYP	V_{BOK} MAX
TPS3600D20	1.78 V	1.84 V	1.91 V	1.97 V
TPS3600D25	2.22 V	2.3 V	2.38 V	2.46 V
TPS3600D33	2.93 V	3.04 V	3.14 V	3.24 V
TPS3600D50	4.40 V	4.56 V	4.71 V	4.86 V

detailed description (continued)

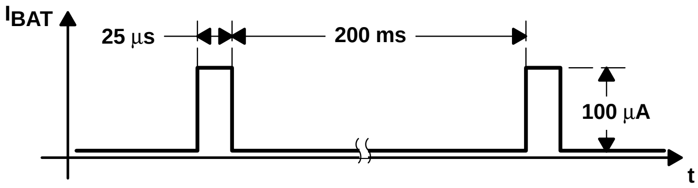


Figure 1. BATTOK Timing

chip-enable signal gating

The internal gating of chip-enable signals (CE) prevents erroneous data from corrupting CMOS RAM during an under-voltage condition. The TPS3600 use a series transmission gate from $\overline{\text{CEIN}}$ to $\overline{\text{CEOUT}}$. During normal operation (reset not asserted), the CE transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short CE propagation delay from $\overline{\text{CEIN}}$ to $\overline{\text{CEOUT}}$ enables the TPS3600 devices to be used with most processors.

The CE transmission gate is disabled and $\overline{\text{CEIN}}$ is high impedance (disable mode) while reset is asserted. During a power-down sequence when V_{DD} crosses the reset threshold, the CE transmission gate will be disabled and $\overline{\text{CEIN}}$ immediately becomes high impedance if the voltage at $\overline{\text{CEIN}}$ is high. If $\overline{\text{CEIN}}$ is low during reset is asserted, the CE transmission gate will be disabled same time when $\overline{\text{CEIN}}$ goes high, or 15 µs after reset asserts, whichever occurs first. This will allow the current write cycle to complete during power down. When the CE transmission gate is enabled, the impedance of $\overline{\text{CEIN}}$ appears as a resistor in series with the load at $\overline{\text{CEOUT}}$. The overall device propagation delay through the CE transmission gate depends on V_{OUT}, the source impedance of the device connected to $\overline{\text{CEIN}}$ and the load at $\overline{\text{CEOUT}}$. To achieve minimum propagation delay, the capacitive load at $\overline{\text{CEOUT}}$ should be minimized, and a low-output-impedance driver be used.

During disable mode, the transmission gate is off and an active pullup connects $\overline{\text{CEOUT}}$ to V_{OUT}. This pullup turns off when the transmission gate is enabled.

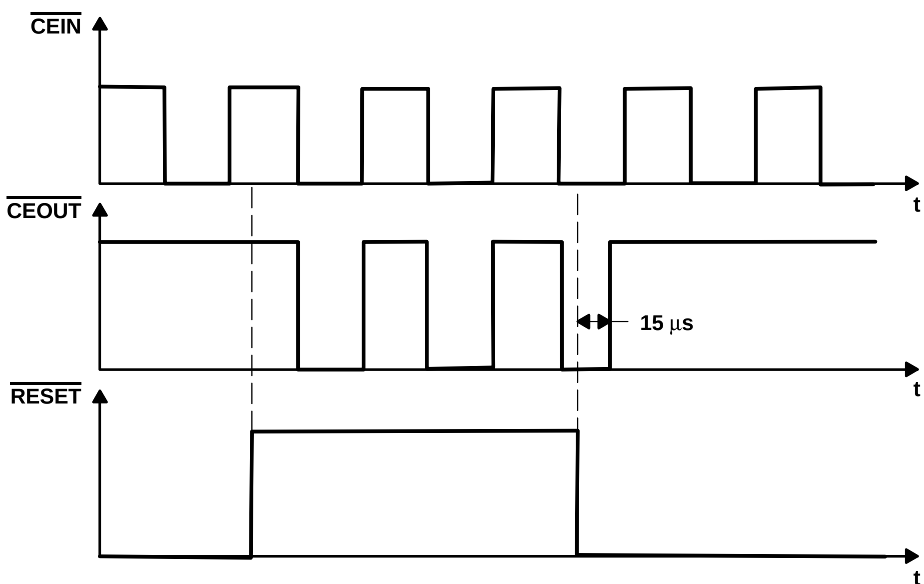


Figure 2. Chip-Enable Timing

detailed description (continued)

power-fail comparator (PFI and $\overline{PFO}$)

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail input (PFI) will be compared with an internal voltage reference of 1.15 V. If the input voltage falls below the power-fail threshold, $V_{(PFI)}$, of 1.15 V typical, the power-fail output ($\overline{PFO}$) goes low. If it goes above $V_{(PFI)}$ plus about 12-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltages above $V_{(PFI)}$. The sum of both resistors should be about 1 MΩ, to minimize power consumption and also to ensure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage.

If the power-fail comparator is unused, connect PFI to ground and leave $\overline{PFO}$ unconnected.

BATTON

Most often BATTON is used as a gate drive for an external pass transistor for high-current applications. In addition it can be also used as a logic output to indicate the battery switchover status. BATTON is high when V_{OUT} is connected to V_{BAT}.

BATTON can be directly connected to the gate of a PMOS transistor (see Figure 3). No current-limiting resistor is required. When using a PMOS transistor, it must be connected backwards from the traditional method (see Figure 3). This method orients the body diode from V_{DD} to V_{OUT} and prevents the backup battery from discharging through the FET when its gate is high.

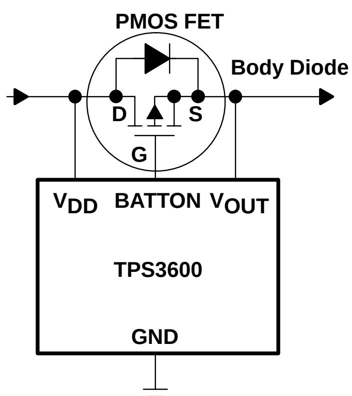


Figure 3. Driving an External MOSFET Transistor With BATTON

backup-battery switchover

In the event of a brownout or power failure, it may be necessary to keep a processor running. If a backup battery is installed at V_{BAT}, the devices automatically connect the processor to backup power when V_{DD} fails. In order to allow the backup battery (e.g., a 3.6-V lithium cell) to have a higher voltage than V_{DD}, this family of supervisors will not connect V_{BAT} to V_{OUT} when V_{BAT} is greater than V_{DD}. V_{BAT} only connects to V_{OUT} (through a 2-Ω switch) when V_{OUT} falls below $V_{(SWN)}$ and V_{BAT} is greater than V_{DD}. When V_{DD} recovers, switchover is deferred either until V_{DD} crosses V_{BAT}, or when V_{DD} rises above the threshold $V_{(SWP)}$. (See the timing diagram)

$V_{DD} > V_{BAT}$	$V_{DD} > V_{(SW)}$	V_{OUT}
1	1	V_{DD}
1	0	V_{DD}
0	1	V_{DD}
0	0	V_{BAT}

detailed description (continued)

manual switchover (MSWITCH)

While operating in the normal mode from V_{DD}, the device can be manually forced to operate in the battery-backup mode by connecting MSWITCH to V_{DD}. The table below shows the different switchover modes.

	MSWITCH	STATUS
V_{DD} mode	GND	V_{DD} mode
	V_{DD}	Switch to battery-backup mode
Battery-backup mode	GND	Battery-backup mode
	V_{DD}	Battery-backup mode

If the manual switchover feature is not used, MSWITCH must be connected to ground.

watchdog

In a microprocessor- or DSP-based system, it is not only important to supervise the supply voltage, it is also important to ensure the correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, microcontroller, or the DSP have to toggle the watchdog input within typically 0.8 s to avoid a time-out from occurring. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected the watchdog is disabled and will be retriggered internally.

saving current while using the watchdog

The watchdog input is internally driven low during the first 7/8 of the watchdog time-out period, then momentarily pulses high, resetting the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog time-out period, pulsing it low-high-low once within 7/8 of the watchdog time-out period to reset the watchdog timer. If instead, WDI is externally driven high for the majority of the time-out period, a current of e.g. 5 V/40 kΩ ≈ 125 µA can flow into WDI.

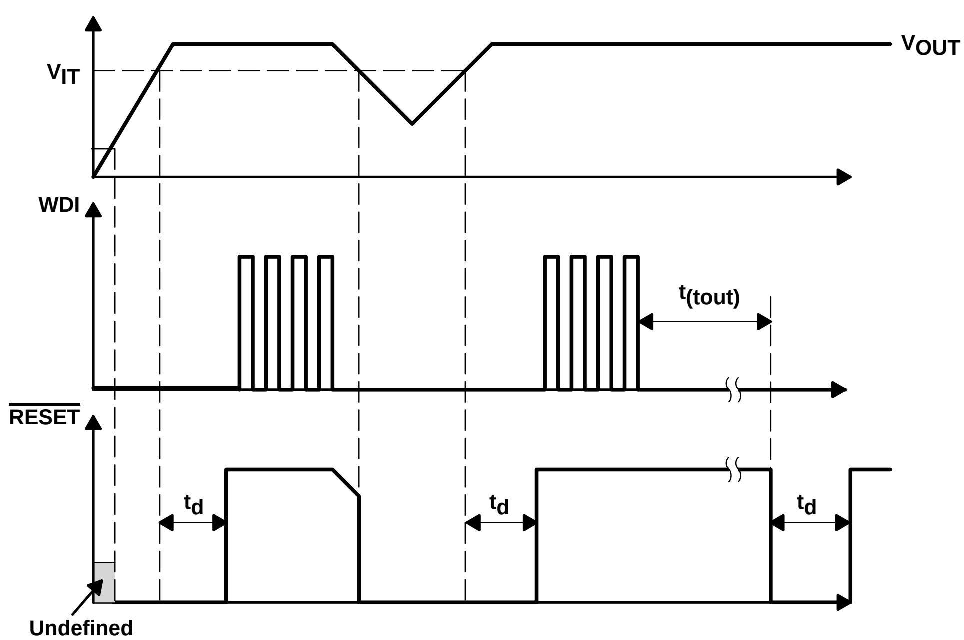


Figure 4. Watchdog Timing

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage: V_{DD} (see Note1) . . . . 7 V
All other pins (see Note 1) . . . . –0.3 V to 7 V
Continuous output current at V_{OUT}: I_O . . . . 300 mA
All other pins, I_O . . . . ±10 mA
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t = 1000h continuously.

DISSIPATION RATING TABLE

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
PW	700 mW	5.6 mW/°C	448 mW	364 mW

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.65	5.5	V
Battery supply voltage, V_{BAT}	1.5	5.5	V
Input voltage, V_I	0	V_{OUT} + 0.3	V
High-level input voltage, V_{IH}	0.7 x V_{OUT}		V
Low-level input voltage, all other pins, V_{IL}		0.3 x V_{OUT}	V
Continuous output current at V_{OUT}, I_O		200	mA
Input transition rise and fall rate at WDI, MSWITCH, $\Delta t/\Delta V$		100	ns/V
Slew rate at V_{DD} or V_{BAT}		34	mV/µs
Operating free-air temperature range, T_A	–40	85	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{\text{RESET}}$, BATTOK, BATTON	V_{OUT} = 2.0 V, I_{OH} = –400 μA	V_{OUT} – 0.2 V			V
			V_{OUT} = 3.3 V, I_{OH} = –2 mA	V_{OUT} – 0.4 V			
			V_{OUT} = 5.0 V, I_{OH} = –3 mA				
		$\overline{\text{PFO}}$	V_{OUT} = 1.8 V, I_{OH} = –20 μA	V_{OUT} – 0.3 V			
			V_{OUT} = 3.3 V, I_{OH} = –80 μA	V_{OUT} – 0.4 V			
			V_{OUT} = 5.0 V, I_{OH} = –120 μA				
		$\overline{\text{CEOUT}}$ Enable mode $\overline{\text{CEIN}}$ = V_{OUT}	V_{OUT} = 2.0 V, I_{OH} = –1 mA	V_{OUT} – 0.2 V			
			V_{OUT} = 3.3 V, I_{OH} = –2 mA	V_{OUT} – 0.3 V			
			V_{OUT} = 5.0 V, I_{OH} = –5 mA				
		$\overline{\text{CEOUT}}$ Disable mode	V_{OUT} = 3.3 V, I_{OH} = –0.5 mA	V_{OUT} – 0.4 V			
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$, $\overline{\text{PFO}}$, BATTOK	V_{OUT} = 2.0 V, I_{OL} = 400 μA			0.2	V
			V_{OUT} = 3.3 V, I_{OL} = 2 mA			0.4	
			V_{OUT} = 5.0 V, I_{OL} = 3 mA				
		BATTON	V_{OUT} = 1.8 V, I_{OL} = 500 μA			0.2	
			V_{OUT} = 3.3 V, I_{OL} = 3 mA			0.4	
			V_{OUT} = 5.0 V, I_{OL} = 5 mA				
		$\overline{\text{CEOUT}}$ Enable mode $\overline{\text{CEIN}}$ = 0 V	V_{OUT} = 2.0 V, I_{OL} = 1 mA			0.2	
			V_{OUT} = 3.3 V, I_{OL} = 2 mA			0.3	
			V_{OUT} = 5.0 V, I_{OL} = 5 mA				
V_{res}	Power-up reset voltage (see Note 2)		V_{BAT} > 1.1 V OR V_{DD} > 1.4 V, I_{OL} = 20 μA			0.4	V
V_{OUT}	Normal mode		I_O = 5 mA, V_{DD} = 1.8 V	V_{DD} – 50 mV			V
			I_O = 75 mA, V_{DD} = 3.3 V	V_{DD} – 150 mV			
			I_O = 150 mA, V_{DD} = 5 V	V_{DD} – 250 mV			
	Battery-backup mode		I_O = 4 mA, V_{BAT} = 1.5 V	V_{BAT} – 50 mV			
			I_O = 75 mA, V_{BAT} = 3.3 V	V_{BAT} – 150 mV			
$r_{ds(on)}$	V_{DD} to V_{OUT} on-resistance		V_{DD} = 3.3 V		1	2	Ω
	V_{BAT} to V_{OUT} on-resistance		V_{BAT} = 3.3 V		1	2	
V_{IT}	Negative-going input threshold voltage (see Notes 3 and 4)	TPS3600x20	T_A = –40°C to 85°C	1.74	1.78	1.82	V
		TPS3600x25		2.17	2.22	2.27	
		TPS3600x30		2.57	2.63	2.69	
		TPS3600x33		2.87	2.93	2.99	
		TPS3600x50		4.31	4.40	4.49	
$V_{(PFI)}$		PFI		1.13	1.15	1.17	
$V_{(BOK)}$		TPS3600Dxx		V_{IT} + 5.8%	V_{IT} + 7.1%	V_{IT} + 8.3%	
$V_{(SWN)}$	Battery switch threshold voltage negative-going V_{OUT}			V_{IT} + 1%	V_{IT} + 2%	V_{IT} + 3.2%	V

NOTES: 2. The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. $t_{r(VDD)} \geq 15$ μs/V.
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near the supply terminal.
4. Voltage is sensed at V_{OUT}

electrical characteristics over recommended operating conditions (unless otherwise noted) (continued)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hys}	Hysteresis	V_{IT}	1.65 V < V_{IT} < 2.5 V		20		mV
			2.5 V < V_{IT} < 3.5 V		40		
			3.5 V < V_{IT} < 5.5 V		50		
		BATTOK	1.65 V < $V_{(BOK)}$ < 2.5 V		30		
			2.5 V < $V_{(BOK)}$ < 3.5 V		60		
			3.5 V < $V_{(BOK)}$ < 5.5 V		100		
		PFI			12		
		$V_{(BSW)}$	V_{DD} = 1.8 V		66		
		$V_{(SWN)}$	1.65 V < $V_{(SWN)}$ < 2.5 V		85		
			2.5 V < $V_{(SWN)}$ < 3.5 V		100		
			3.5 V < $V_{(SWN)}$ < 5.5 V		110		
I_{IH}	High-level input current	WDI (see Note 5)	WDI = V_{DD} = 5 V			150	μA
		$\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 5 V	–33		–76	
I_{IL}	Low-level input current	WDI (see Note 5)	WDI = 0 V, V_{DD} = 5 V			–150	
		$\overline{MR}$	$\overline{MR}$ = 0 V, V_{DD} = 5 V	–110		–255	
I_I	Input current	PFI, MSWITCH	V_I < V_{DD}	–25		25	nA
I_{OS}	Short-circuit current	$\overline{PFO}$	$\overline{PFO}$ = 0 V, V_{DD} = 1.8 V			–0.3	mA
			$\overline{PFO}$ = 0 V, V_{DD} = 3.3 V			–1.1	
			$\overline{PFO}$ = 0 V, V_{DD} = 5 V			–2.4	
I_{DD}	V_{DD} supply current		V_{OUT} = V_{DD}			40	μA
			V_{OUT} = V_{BAT}			8	
$I_{(BAT)}$	V_{BAT} supply current		V_{OUT} = V_{DD}	–0.1		0.1	μA
			V_{OUT} = V_{BAT}			40	
I_{lkg}	$\overline{CEIN}$ leakage current		Disable mode, V_I < V_{DD}			±1	μA
C_i	Input capacitance		V_I = 0 V to 5.0 V		5		pF

NOTE 5: For details on how to optimize current consumption when using WDI, see the detailed description section.

timing requirements at R_L = 1 MΩ, C_L = 50 pF, T_A = –40°C to 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	V_{DD}	$V_{IH} = V_{IT}$ + 0.2 V, $V_{IL} = V_{IT}$ – 0.2 V	5	1		µs
		$\overline{MR}$	$V_{DD} > V_{IT}$ + 0.2 V, V_{IL} = 0.3 x V_{DD}, V_{IH} = 0.7 x V_{DD}	100			ns
		WDI					

switching characteristics at R_L= 1 MΩ, C_L = 50 pF, T_A = –40°C to 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{DD} \geq V_{IT}$ + 0.2 V, $\overline{MR} \geq$ 0.7 x V_{DD}, See timing diagram	60	100	140	ms
$t_{(tout)}$	Watchdog time-out		$V_{DD} > V_{IT}$ + 0.2 V, See timing diagram	0.48	0.8	1.12	s
t_{PLH}	Propagation (delay) time, low-to-high-level output	50% $\overline{RESET}$ to 50% $\overline{CEOUT}$	$V_{OUT} = V_{IT}$		15		µs
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{RESET}$	$V_{IL} = V_{IT}$ – 0.2 V, $V_{IH} = V_{IT}$ + 0.2 V		2	5	µs
		PFI to $\overline{PFO}$	$V_{IL} = V_{(PFI)}$ – 0.2 V, $V_{IH} = V_{(PFI)}$ + 0.2 V		3	5	µs
		$\overline{MR}$ to $\overline{RESET}$	$V_{DD} \geq V_{IT}$ + 0.2 V, V_{IL} = 0.3 x V_{DD}, V_{IH} = 0.7 x V_{DD}		0.1	1	µs
		50% $\overline{CEIN}$ to 50% $\overline{CEOUT}$ CL = 50 pF only (see Note 6)	V_{DD} = 1.8 V		5	15	ns
			V_{DD} = 3.3 V		1.6	5	ns
			V_{DD} = 5 V		1	3	ns
	Transition time	V_{DD} to BATTON	$V_{IL} = V_{BAT}$ – 0.2 V, $V_{IH} = V_{BAT}$ + 0.2 V, $V_{(BAT)} < V_{IT}$			3	µs

NOTE 6: Ensured by design.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$r_{DS(on)}$	Static Drain-source on-state resistance V_{DD} to V_{OUT}	vs Output current	5
	Static Drain-source on-state resistance V_{BAT} to V_{OUT}		6
	Static Drain-source on-state resistance	vs Chip enable input voltage	7
I_{DD}	Supply current	vs Supply voltage	8, 9
V_{IT}	Normalized threshold voltage	vs Free-air temperature	10
V_{OH}	High-level output voltage at $\overline{RESET}$	vs High-level output current	11, 12
	High-level output voltage at $\overline{PFO}$		13, 14
	High-level output voltage at $\overline{CEOUT}$		15, 16, 17, 18
V_{OL}	Low-level output voltage at $\overline{RESET}$	vs Low-level output current	19, 20
	Low-level output voltage at $\overline{CEOUT}$		21, 22
	Low-level output voltage at BATTON		23, 24
$t_{p(min)}$	Minimum Pulse Duration at V_{DD}	vs Threshold voltage overdrive at V_{DD}	25
	Minimum Pulse Duration at PFI	vs Threshold voltage overdrive at PFI	26

TYPICAL CHARACTERISTICS

STATIC DRAIN SOURCE ON-STATE RESISTANCE (V_{DD} TO V_{OUT}) vs OUTPUT CURRENT

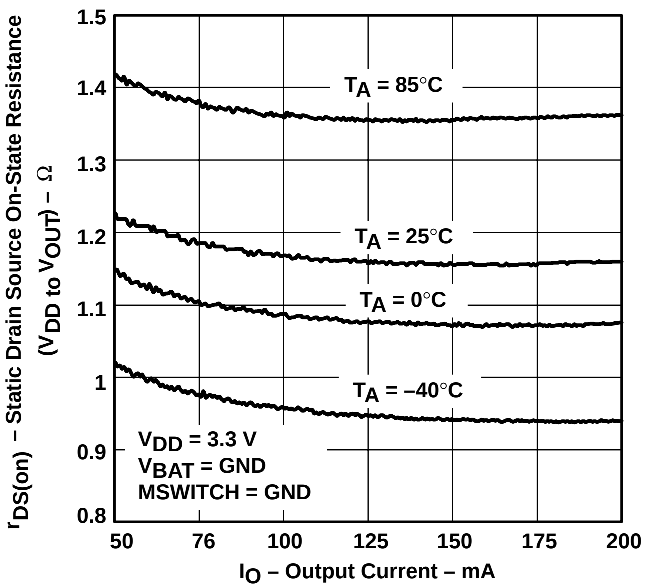


Figure 5

STATIC DRAIN SOURCE ON-STATE RESISTANCE (V_{BAT} TO V_{OUT}) vs OUTPUT CURRENT

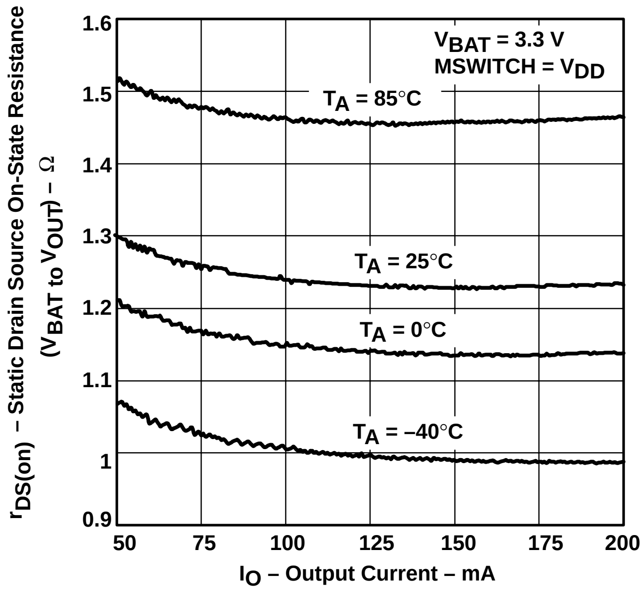


Figure 6

STATIC DRAIN SOURCE ON-STATE RESISTANCE ($\overline{CEIN}$ to $\overline{CEOUT}$) vs CHIP-ENABLE INPUT VOLTAGE

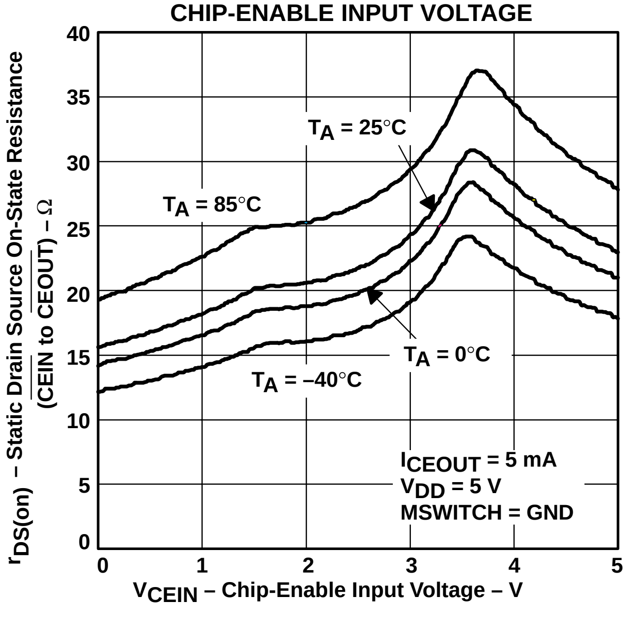


Figure 7

SUPPLY CURRENT vs SUPPLY VOLTAGE

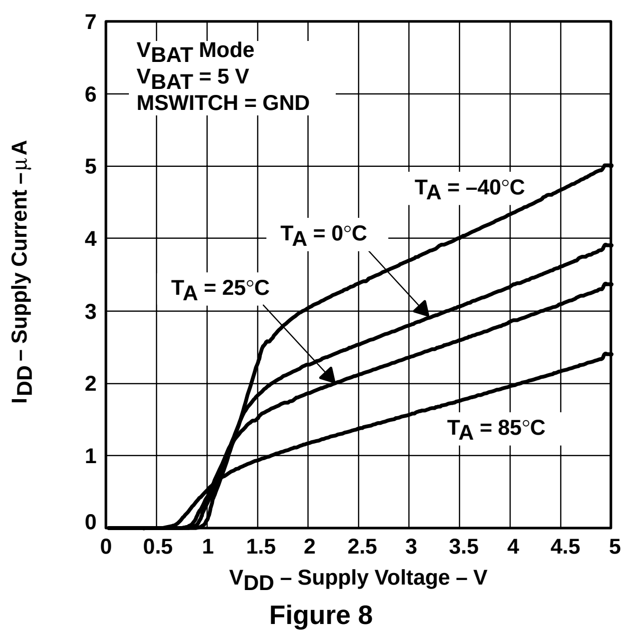


Figure 8

TYPICAL CHARACTERISTICS

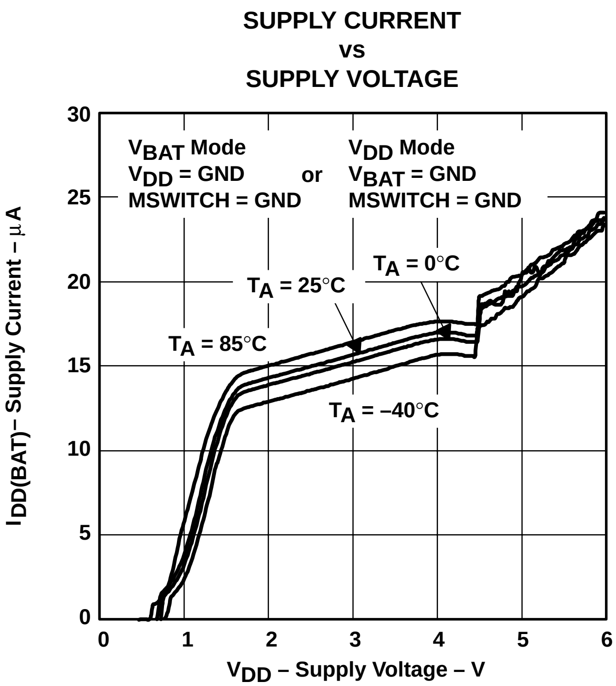


Figure 9

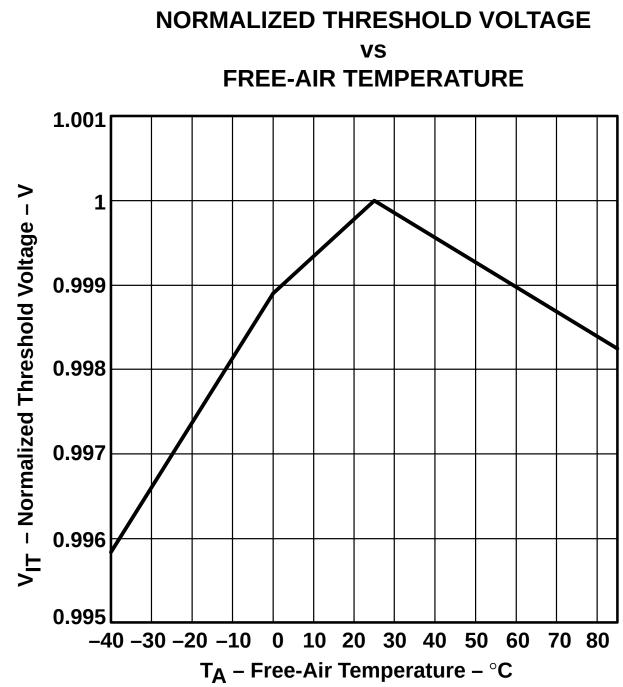


Figure 10

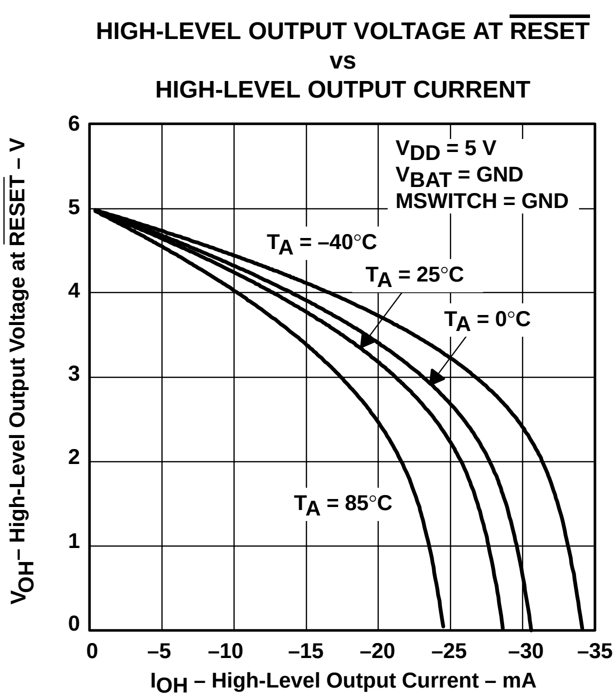


Figure 11

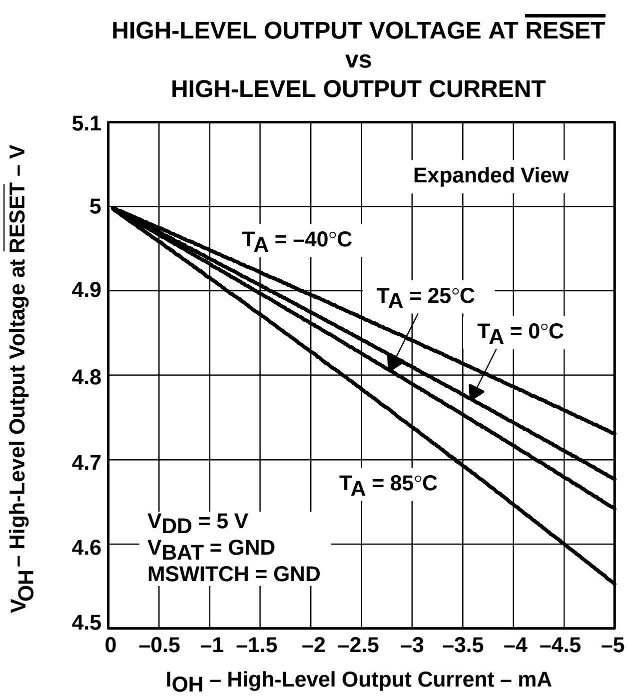


Figure 12

TYPICAL CHARACTERISTICS

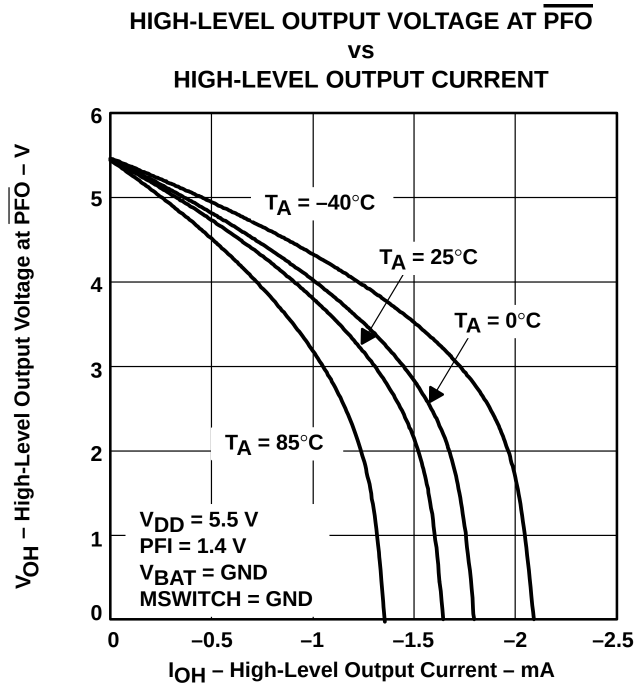


Figure 13

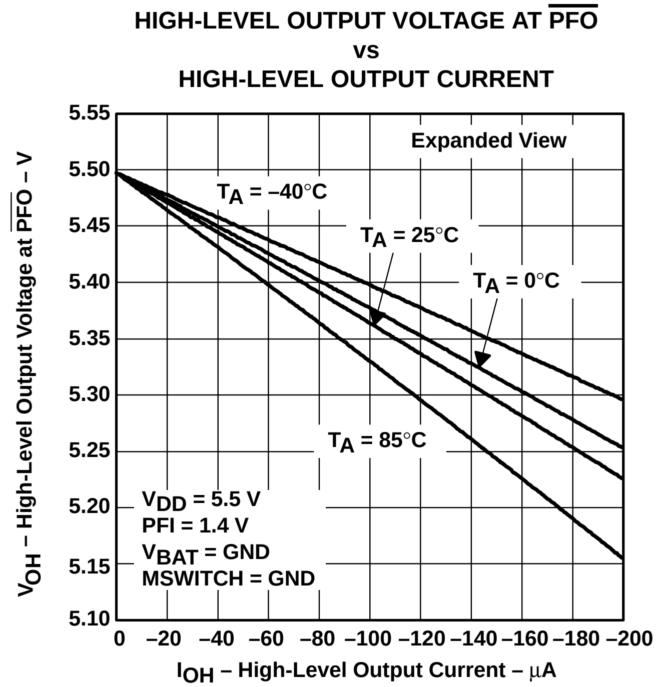


Figure 14

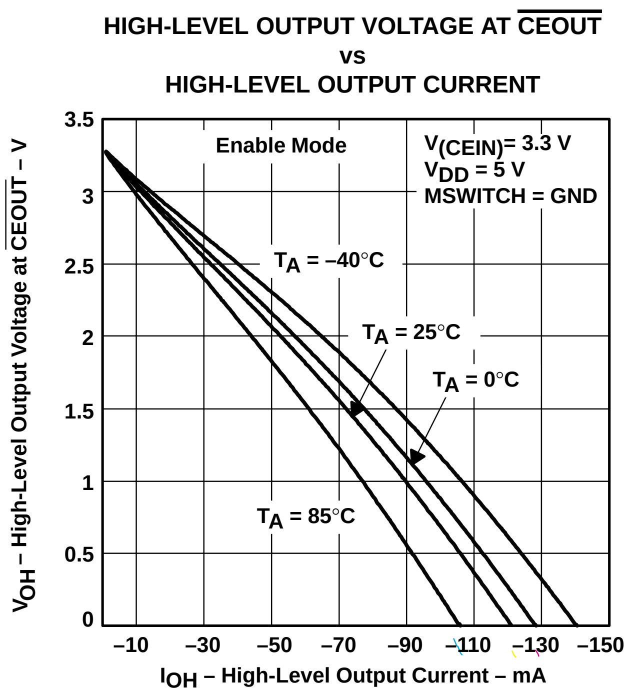


Figure 15

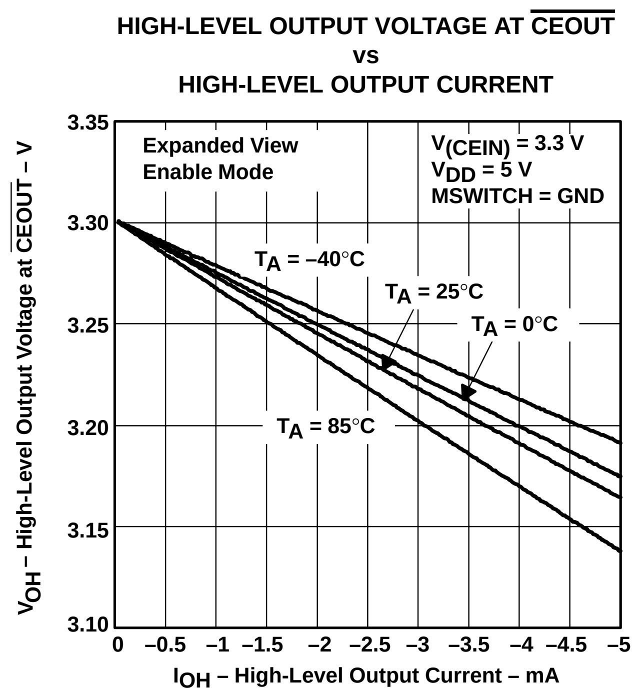


Figure 16

TYPICAL CHARACTERISTICS

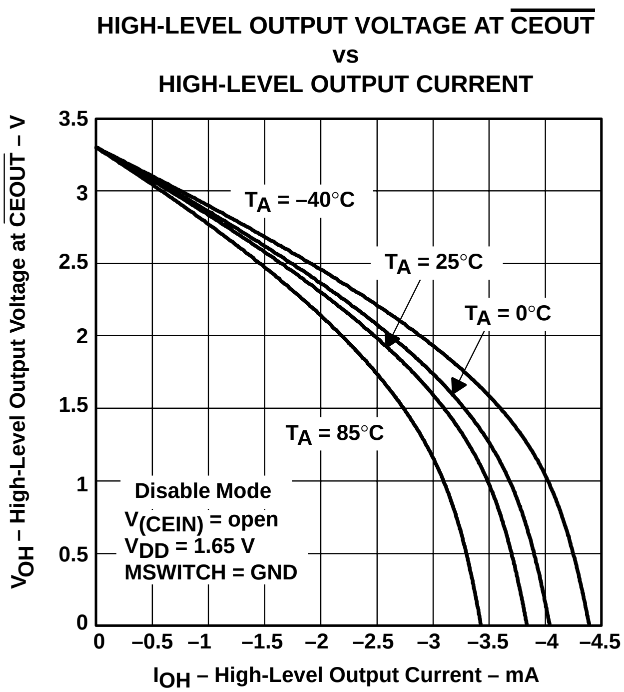


Figure 17

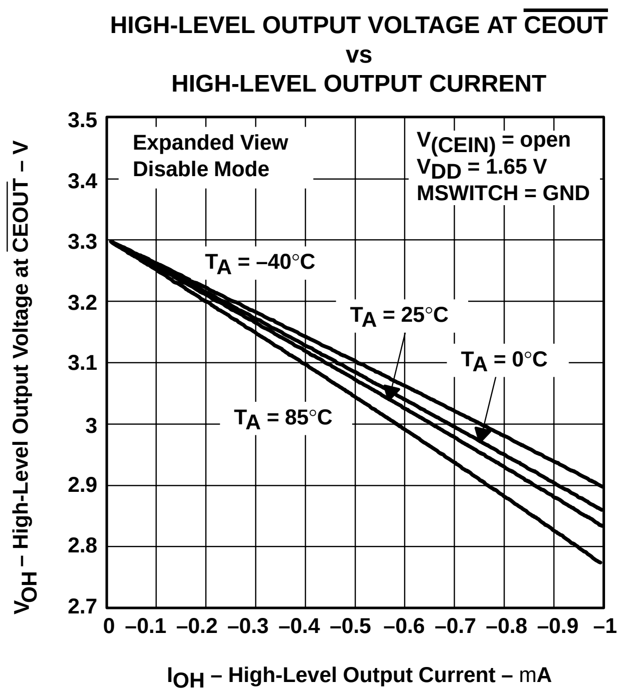


Figure 18

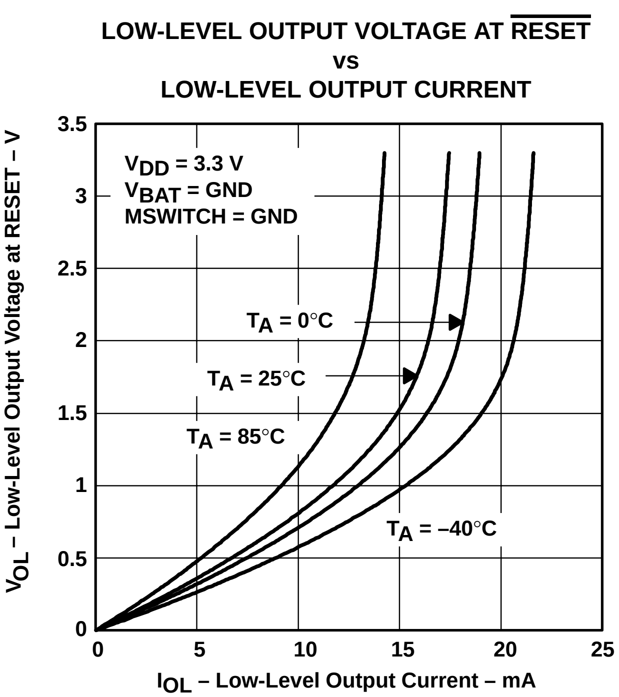


Figure 19

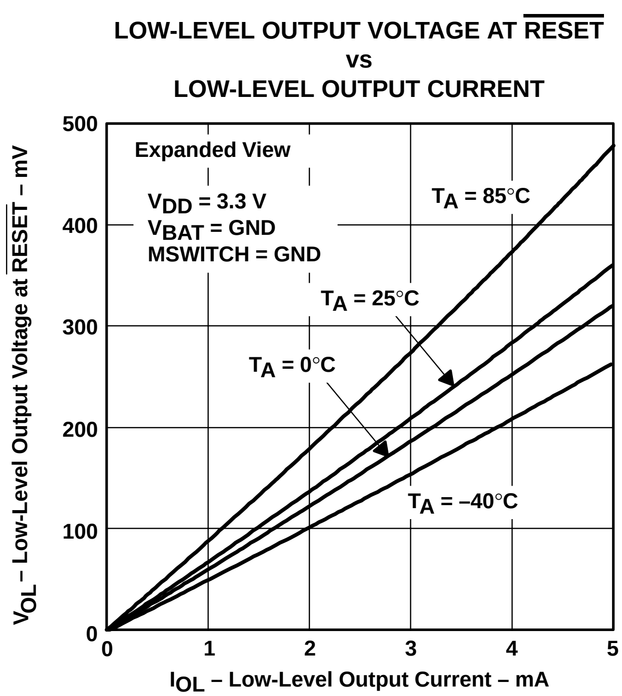


Figure 20

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE AT $\overline{CEOUT}$ vs LOW-LEVEL OUTPUT CURRENT

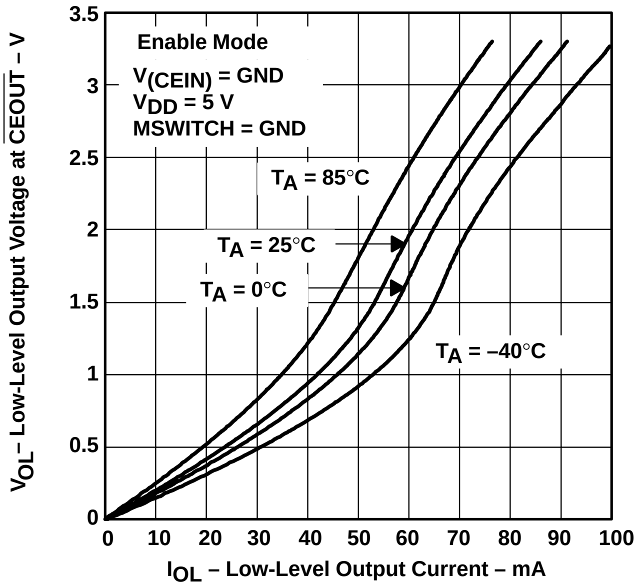


Figure 21

LOW-LEVEL OUTPUT VOLTAGE AT $\overline{CEOUT}$ vs LOW-LEVEL OUTPUT CURRENT

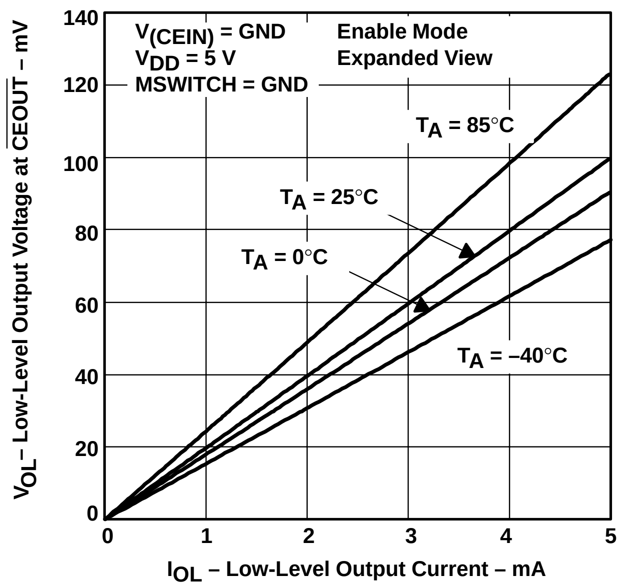


Figure 22

LOW-LEVEL OUTPUT VOLTAGE AT BATTON vs LOW-LEVEL OUTPUT CURRENT

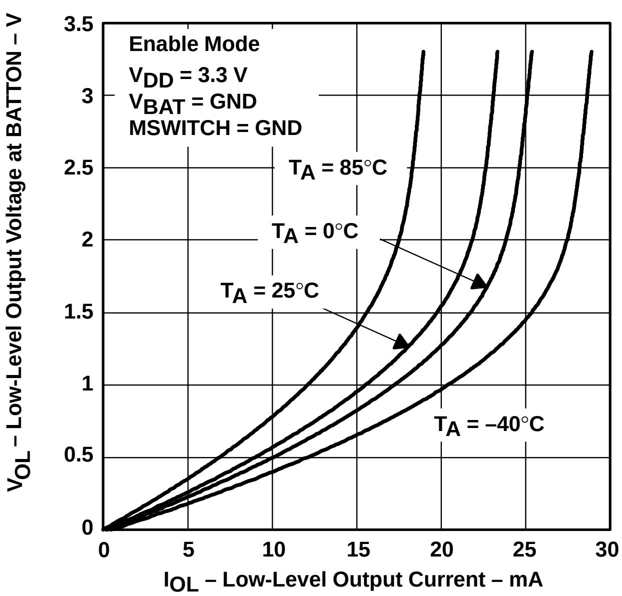


Figure 23

LOW-LEVEL OUTPUT VOLTAGE AT BATTON vs LOW-LEVEL OUTPUT CURRENT

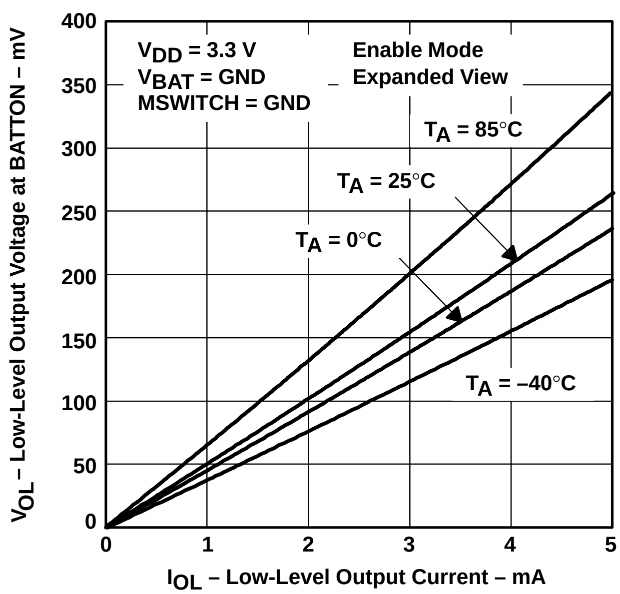


Figure 24

TYPICAL CHARACTERISTICS

TPS3600D50
MINIMUM PULSE DURATION AT V_{DD}
vs
THRESHOLD OVERDRIVE AT V_{DD}

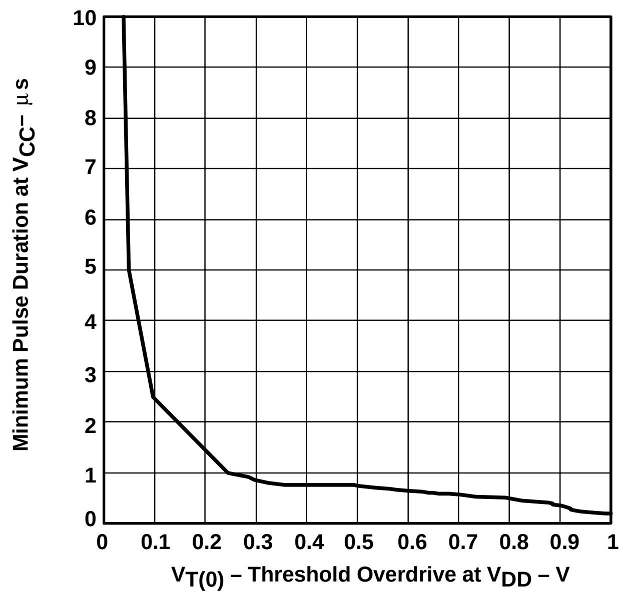


Figure 25

TPS3600D50
MINIMUM PULSE DURATION AT PFI
vs
THRESHOLD OVERDRIVE AT PFI

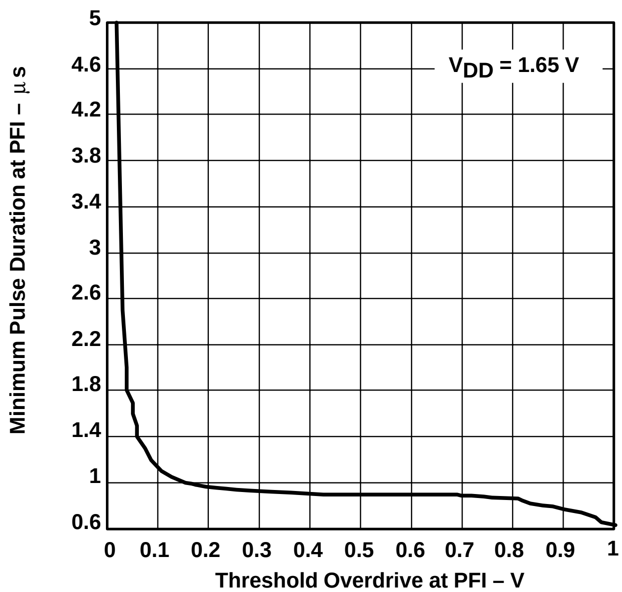
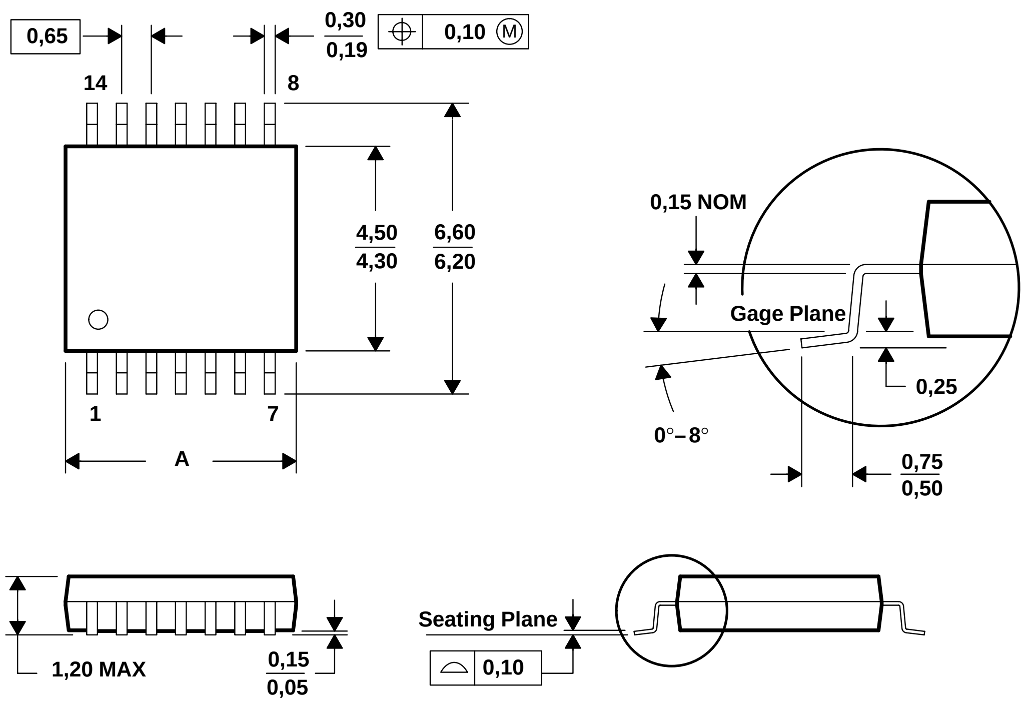


Figure 26

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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