1 Digital Media System-on-Chip (DMSoC)

1.1 Features

- **High-Performance Digital Media SoC**
  - **594-MHz C64x+™ Clock Rate**
  - **297-MHz ARM926EJ-S™ Clock Rate**
  - **Eight 32-Bit C64x+ Instructions/Cycle**
  - **4752 C64x+ MIPS**
  - **Fully Software-Compatible With C64x / ARM9™**
- **Advanced Very-Long-Instruction-Word (VLIW) TMS320C64x+™ DSP Core**
  - **Eight Highly Independent Functional Units**
    - **Six ALUs (32-/40-Bit), Each Supports Single 32-Bit, Dual 16-Bit, or Quad 8-Bit Arithmetic per Clock Cycle**
    - **Two Multipliers Support Four 16 x 16-Bit Multiplies (32-Bit Results) per Clock Cycle or Eight 8 x 8-Bit Multiplies (16-Bit Results) per Clock Cycle**
  - **Load-Store Architecture With Non-Aligned Support**
  - **64 32-Bit General-Purpose Registers**
  - **Instruction Packing Reduces Code Size**
  - **All Instructions Conditional**
  - **Additional C64x+™ Enhancements**
    - **Protected Mode Operation**
    - **Exceptions Support for Error Detection and Program Redirection**
    - **Hardware Support for Modulo Loop Operation**
- **C64x+ Instruction Set Features**
  - **Byte-Addressable (8-/16-/32-/64-Bit Data)**
  - **8-Bit Overflow Protection**
  - **Bit-Field Extract, Set, Clear**
  - **Normalization, Saturation, Bit-Counting**
  - **Compact 16-Bit Instructions**
  - **Additional Instructions to Support Complex Multiplies**
- **C64x+ L1/L2 Memory Architecture**
  - **32K-Byte L1P Program RAM/Cache (Direct Mapped)**
  - **80K-Byte L1D Data RAM/Cache (2-Way Set-Associative)**
  - **64K-Byte L2 Unified Mapped RAM/Cache (Flexible RAM/Cache Allocation)**
- **ARM926EJ-S (MPU) Core**
  - **Support for 32-Bit and 16-Bit (Thumb® Mode) Instruction Sets**
  - **DSP Instruction Extensions and Single Cycle MAC**
  - **ARM® Jazelle® Technology**
  - **EmbeddedICE-RT™ Logic for Real-Time Debug**
- **ARM9 Memory Architecture**
  - **16K-Byte Instruction Cache**
  - **8K-Byte Data Cache**
  - **16K-Byte RAM**
  - **16K-Byte ROM**
- **Embedded Trace Buffer™ (ETB11™) With 4KB Memory for ARM9 Debug**
- **Endianness: Little Endian for ARM and DSP**
- **Video Processing Subsystem**
  - **Front End Provides:**
    - **CCD and CMOS Imager Interface**
    - **BT.601/BT.656 Digital YCbCr 4:2:2 (8-/16-Bit) Interface**
    - **Preview Engine for Real-Time Image Processing**
    - **Glueless Interface to Common Video Decoders**
    - **Histogram Module**
    - **Auto-Exposure, Auto-White Balance and Auto-Focus Module**
    - **Resize Engine**
      - **Resize Images From 1/4x to 4x**
      - **Separate Horizontal/Vertical Control**
  - **Back End Provides:**
    - **Hardware On-Screen Display (OSD)**
    - **Four 54-MHz DACs for a Combination of**
      - **Composite NTSC/PAL Video**
      - **Luma/Chroma Separate Video (S-video)**
      - **Component (YPbPr or RGB) Video (Progressive)**
    - **Digital Output**
      - **8-/16-bit YUV or up to 24-Bit RGB**
      - **HD Resolution**
      - **Up to 2 Video Windows**

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- **External Memory Interfaces (EMIFs)**
  - **32-Bit DDR2 SDRAM Memory Controller With 256M-Byte Address Space (1.8-V I/O)**
  - **Asynchronous16-Bit Wide EMIF (EMIFA) With 128M-Byte Address Reach**
    - **Flash Memory Interfaces**
      - **NOR (8-/16-Bit-Wide Data)**
      - **NAND (8-/16-Bit-Wide Data)**
- **Flash Card Interfaces**
  - **Multimedia Card (MMC)/Secure Digital (SD)**
  - **CompactFlash Controller With True IDE Mode**
  - **SmartMedia**
- **Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)**
- **Two 64-Bit General-Purpose Timers (Each Configurable as Two 32-Bit Timers)**
- **One 64-Bit Watch Dog Timer**
- **Three UARTs (One with RTS and CTS Flow Control)**
- **One Serial Port Interface (SPI) With Two Chip-Selects**
- **Master/Slave Inter-Integrated Circuit (I^2C Bus™)**
- **Audio Serial Port (ASP)**
  - **I2S**
  - **AC97 Audio Codec Interface**
  - **Standard Voice Codec Interface (AIC12)**
- **10/100 Mb/s Ethernet MAC (EMAC)**
  - **IEEE 802.3 Compliant**
  - **Media Independent Interface (MII)**
- **VLYNQ™ Interface (FPGA Interface)**
- **USB Port With Integrated 2.0 PHY**
  - **USB 2.0 High-/Full-Speed (480-Mbps) Client**
  - **USB 2.0 High-/Full-/Low-Speed Host (Mini-Host, Supporting One External Device)**
- **Three Pulse Width Modulator (PWM) Outputs**
- **On-Chip ARM ROM Bootloader (RBL) to Boot From NAND Flash or UART**
- **ATA/ATAPI I/F (ATA/ATAPI-5 Specification)**
- **Individual Power-Saving Modes for ARM/DSP**
- **Flexible PLL Clock Generators**
- **IEEE-1149.1 (JTAG) Boundary-Scan-Compatible**
- **Up to 71 General-Purpose I/O (GPIO) Pins (Multiplexed With Other Device Functions)**
- **361-Pin Pb-Free BGA Package (ZWT Suffix), 0.8-mm Ball Pitch**
- **0.09-µm/6-Level Cu Metal Process (CMOS)**
- **3.3-V and 1.8-V I/O, 1.2-V Internal**
- **Applications:**
  - **Digital Media**
  - **Networked Media Encode/Decode**
  - **Video Imaging**

1.2 Description

The TMS320DM6446 (also referenced as DM6446) leverages TI’s Davinci technology to meet the networked media encode and decode application processing needs of next-generation embedded devices.

The DM6446 enables OEMs and ODMs to quickly bring to market devices featuring robust operating systems support, rich user interfaces, high processing performance, and long battery life through the maximum flexibility of a fully integrated mixed processor solution.

The dual-core architecture of the DM6446 provides benefits of both DSP and Reduced Instruction Set Computer (RISC) technologies, incorporating a high-performance TMS320C64x+ DSP core and an ARM926EJ-S MPU core.

The ARM926EJ-S is a 32-bit RISC processor core that performs 32-bit or 16-bit instructions and processes 32-bit, 16-bit, or 8-bit data. The core uses pipelining so that all parts of the processor and memory system can operate continuously.

The ARM core incorporates:

- A coprocessor 15 (CP15) and protection module
- Data and program Memory Management Units (MMUs) with table look-aside buffers.
- Separate 16K-byte instruction and 8K-byte data caches. Both are four-way associative with virtual index virtual tag (VIVT).

The TMS320C64x+™ DSPs are the highest-performance fixed-point DSP generation in the

TMS320C6000™ DSP platform. It is based on an enhanced version of the second-generation high-performance, advanced very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making these DSP cores an excellent choice for digital media applications. The C64x is a code-compatible member of the C6000™ DSP platform. The TMS320C64x+ DSP is an enhancement of the C64x+ DSP with added functionality and an expanded instruction set.

Any reference to the C64x DSP or C64x CPU also applies, unless otherwise noted, to the C64x+ DSP and C64x+ CPU, respectively.

With performance of up to 4752 million instructions per second (MIPS) at a clock rate of 594 MHz, the C64x+ core offers solutions to high-performance DSP programming challenges. The DSP core possesses the operational flexibility of high-speed controllers and the numerical capability of array processors. The C64x+ DSP core processor has 64 general-purpose registers of 32-bit word length and eight highly independent functional units—two multipliers for a 32-bit result and six arithmetic logic units (ALUs). The eight functional units include instructions to accelerate the performance in video and imaging applications. The DSP core can produce four 16-bit multiply-accumulates (MACs) per cycle for a total of 2376 million MACs per second (MMACS), or eight 8-bit MACs per cycle for a total of 4752 MMACS. For more details on the C64x+ DSP, see the *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (literature number SPRU732).

The DM6446 also has application-specific hardware logic, on-chip memory, and additional on-chip peripherals similar to the other C6000 DSP platform devices. The DM6446 core uses a two-level cache-based architecture. The Level 1 program cache (L1P) is a 256K-bit direct mapped cache and the Level 1 data cache (L1D) is a 640K-bit 2-way set-associative cache. The Level 2 memory/cache (L2) consists of an 512K-bit memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or combinations of the two.

The peripheral set includes: 2 configurable video ports; a 10/100 Mb/s Ethernet MAC (EMAC) with a Management Data Input/Output (MDIO) module; an inter-integrated circuit (I2C) Bus interface; one audio serial port (ASP); 2 64-bit general-purpose timers each configurable as 2 independent 32-bit timers; 1 64-bit watchdog timer; up to 71-pins of general-purpose input/output (GPIO) with programmable interrupt/event generation modes, multiplexed with other peripherals; 3 UARTs with hardware handshaking support on 1 UART; 3 pulse width modulator (PWM) peripherals; and 2 external memory interfaces: an asynchronous external memory interface (EMIFA) for slower memories/peripherals, and a higher speed synchronous memory interface for DDR2.

The DM6446 device includes a Video Processing Subsystem (VPSS) with two configurable video/imaging peripherals: 1 Video Processing Front-End (VPFE) input used for video capture, 1 Video Processing Back-End (VPBE) output with imaging co-processor (VICP) used for display.

The Video Processing Front-End (VPFE) is comprised of a CCD Controller (CCDC), a Preview Engine (Previewer), Histogram Module, Auto-Exposure/White Balance/Focus Module (H3A), and Resizer. The CCDC is capable of interfacing to common video decoders, CMOS sensors, and Charge Coupled Devices (CCDs). The Previewer is a real-time image processing engine that takes raw imager data from a CMOS sensor or CCD and converts from an RGB Bayer Pattern to YUV422. The Histogram and H3A modules provide statistical information on the raw color data for use by the DM6446. The Resizer accepts image data for separate horizontal and vertical resizing from 1/4x to 4x in increments of 256/N, where N is between 64 and 1024.

The Video Processing Back-End (VPBE) is comprised of an On-Screen Display Engine (OSD) and a Video Encoder (VENC). The OSD engine is capable of handling 2 separate video windows and 2 separate OSD windows. Other configurations include 2 video windows, 1 OSD window, and 1 attribute window allowing up to 8 levels of alpha blending. The VENC provides four analog DACs that run at 54 MHz, providing a means for composite NTSC/PAL video, S-Video, and/or Component video output. The VENC also provides up to 24 bits of digital output to interface to RGB888 devices. The digital output is capable of 8/16-bit BT.656 output and/or CCIR.601 with separate horizontal and vertical syncs.

The Ethernet Media Access Controller (EMAC) provides an efficient interface between the DM644X MPU core processor and the network. The DM6446 EMAC support both 10Base-T and 100Base-TX, or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex mode, with hardware flow control and quality of service (QOS) support.

The Management Data Input/Output (MDIO) module continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system. Once a PHY candidate has been selected by the MPU, the MDIO module transparently monitors its link state by reading the PHY status register. Link change events are stored in the MDIO module and can optionally interrupt the MPU, allowing the MPU to poll the link status of the device without continuously performing costly MDIO accesses.

The I2C, SPI, USB2.0, and VLYNQ ports allow DM6446 to easily control peripheral devices and/or communicate with host processors.

The DM6446 also includes a Video/Imaging Co-processor (VICP) to offload many video and imaging processing tasks from the DSP core, making more DSP MIPS available for common video and imaging algorithms. For more information on the VICP enhanced codecs, such as H.264 and MPEG4, please contact your nearest TI sales representative.

The rich peripheral set provides the ability to control external peripheral devices and communicate with external processors. For details on each of the peripherals, see the related sections later in this document and the associated peripheral reference guides.

The DM6446 has a complete set of development tools for both the ARM and DSP. These include C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a Windows™ debugger interface for visibility into source code execution.

1.3 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the device.

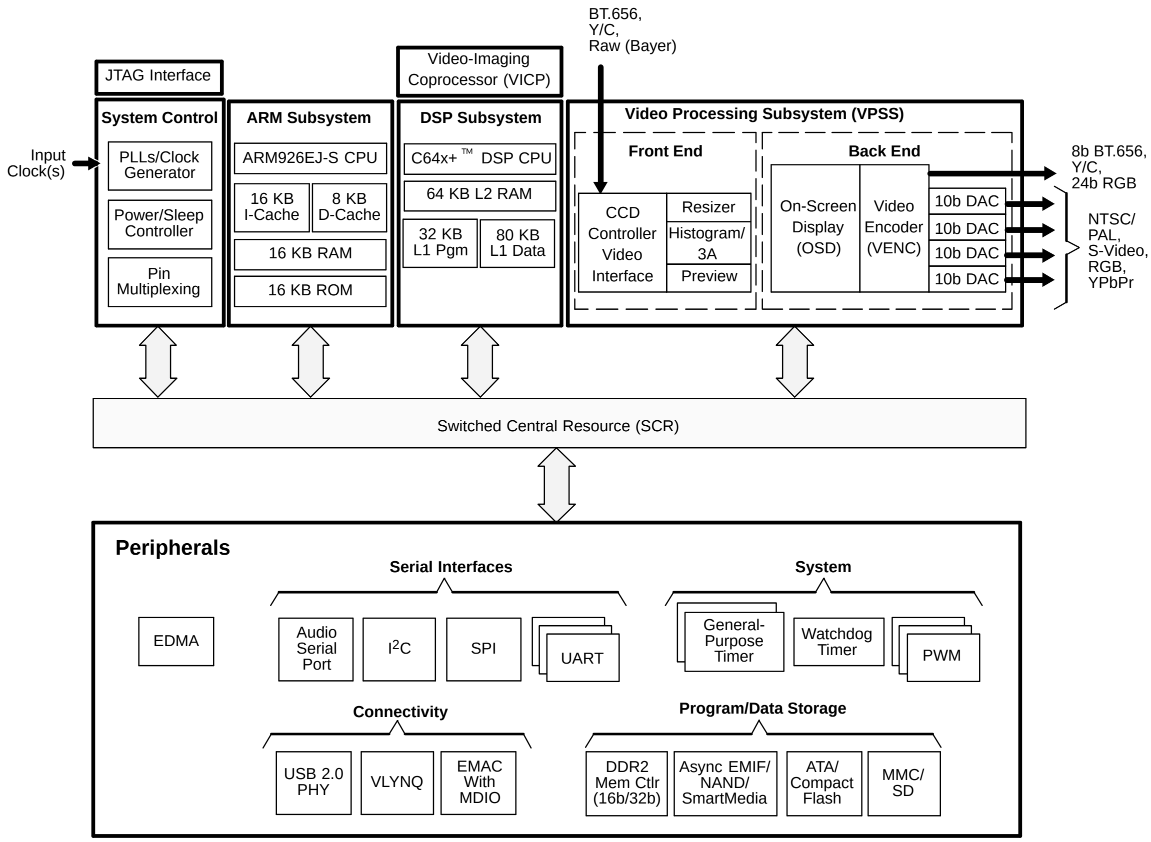

Figure 1-1. TMS320DM6446 Functional Block Diagram

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Contents

2 Device Overview

2.1 Device Characteristics

Table 2-1 provides an overview of the TMS320DM6446 SoC. The table shows significant features of the device, including the capacity of on-chip RAM, peripherals, internal peripheral bus frequency relative to the C64x+ DSP, and the package type with pin count.

Table 2-1. Characteristics of the Processor

HARDWARE FEATURES(1)			DM6446
Peripherals Not all peripherals pins are available at the same time (For more detail, see the Device Configuration section).	DDR2 Memory Controller		DDR2 (16/32-bit bus width)
	Asynchronous EMIF (EMIFA) (speed PLL1/6)		Asynchronous (8/16-bit bus width) RAM, Flash (NOR, NAND)
	Flash Cards (speed PLL1/6)		CF MMC/SD SmartMedia/xD
	EDMA (speed PLL1/3)		64 independent channels 8 QDMA channels
	Timers (speed PLL1/17 [Normal Mode]) (speed PLL1/22 [Turbo Mode])		2 64-Bit General Purpose (each configurable as 2 separate 32-bit timers) 1 64-Bit Watch Dog
	UART (speed PLL1/17 [Normal Mode]) (speed PLL1/22 [Turbo Mode])		3 (one with RTS and CTS flow control)
	SPI (speed PLL1/6)		1 (supports 2 slave devices)
	I^2C (speed PLL1/17 [Normal Mode]) (speed PLL1/22 [Turbo Mode])		1 (Master/Slave)
	Audio Serial Port [ASP] (speed PLL1/6)		1
	10/100 Ethernet MAC with Management Data Input/Output (speed PLL1/6)		1
	VLYNQ (speed PLL1/6)		1
	General-Purpose Input/Output Port (speed PLL1/6)		Up to 71
	PWM (speed PLL1/17 [Normal Mode]) (speed PLL1/22 [Turbo Mode])		3 outputs
	ATA/CF (speed PLL1/6)		1 (ATA/ATAPI-5)
	Configurable Video Ports (speed PLL1/6)		1 Input (VPFE) 1 Output (VPBE)
	USB 2.0 (speed PLL1/6)		High Speed Device High Speed Host
On-Chip Memory	Size (Bytes)		160KB RAM, 16KB ROM
	Organization		DSP [32KB L1 Program (L1P)/Cache (up to 32KB), 80KB L1 Data (L1D)/Cache (up to 32KB), 64KB Unified Mapped RAM/Cache (L2), MPU [16KB I-cache, 8KB D-cache, 16KB RAM, 16KB ROM]
CPU ID + CPU Rev ID	Control Status Register (CSR.[31:16])		TBD
JTAG BSDL_ID	JTAGID register (address location: 0x01C4 0028)		0x0B70 002F
CPU Frequency	MHz	DM6446 - 594	DSP 594 MHz
			MPU 297 MHz
Cycle Time	ns	DM6446 - 594	DSP 1.68 ns
			MPU 3.37 ns
Voltage	Core (V)		1.2 V (-594)
	I/O (V)		1.8 V, 3.3 V
PLL Options	CLKIN frequency multiplier (27 MHz reference)		x1 (Bypass), x22 (-594)
BGA Package	16 x 16 mm		357-Pin BGA (ZWT)
Process Technology	µm		0.09 µm

(1) Speeds noted may not indicate peripheral operating speed, but rather peripheral state machine clocking speed.

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Table 2-1. Characteristics of the Processor (continued)

HARDWARE FEATURES(1)		DM6446
Product Status(2)	Product Preview (PP), Advance Information (AI), or Production Data (PD)	PP

(2) PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice .

2.2 Device Compatibility

The ARM926EJ-S RISC MPU is compatible with other ARM9 MPUs from ARM Holdings plc.

The C64X+ DSP core is code-compatible with the C6000™ DSP platform and supports features of the C64X DSP family.

2.3 ARM Subsystem

The ARM Subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the DSP Subsystem, the VPSS Subsystem, and a majority of the peripherals and external memories.

The ARM Subsystem includes the following features:

- ARM926EJ-S RISC processor
- ARMv5TEJ (32/16-bit) instruction set
- Little endian
- Co-Processor 15 (CP15)
- MMU
- 16KB Instruction cache
- 8KB Data cache
- Write Buffer
- 16KB Internal RAM (32-bit wide access)
- 16KB Internal ROM (ARM bootloader for non-EMIFA boot options)
- Embedded Trace Module and Embedded Trace Buffer (ETM/ETB)
- ARM Interrupt controller
- PLL Controller
- Power and Sleep Controller (PSC)
- System Module

2.3.1 ARM926EJ-S RISC MPU

The ARM Subsystem integrates the ARM926EJ-S processor. The ARM926EJ-S processor is a member of ARM9 family of general-purpose microprocessors. This processor is targeted at multi-tasking applications where full memory management, high performance, low die size, and low power are all important. The ARM926EJ-S processor supports the 32-bit ARM and 16 bit THUMB instruction sets, enabling the user to trade off between high performance and high code density. Specifically, the ARM926EJ-S processor supports the ARMv5TEJ instruction set, which includes features for efficient execution of Java byte codes, providing Java performance similar to Just in Time (JIT) Java interpreter, but without associated code overhead.

The ARM926EJ-S processor supports the ARM debug architecture and includes logic to assist in both hardware and software debug. The ARM926EJ-S processor has a Harvard architecture and provides a complete high performance subsystem, including:

- ARM926EJ -S integer core
- CP15 system control coprocessor

- Memory Management Unit (MMU)
- Separate instruction and data Caches
- Write buffer
- Separate instruction and data Tightly-Coupled Memories (TCMs) [internal RAM] interfaces
- Separate instruction and data AHB bus interfaces
- Embedded Trace Module and Embedded Trace Buffer (ETM/ETB)

For more complete details on the ARM9, refer to the ARM926EJ-S Technical Reference Manual, available at http://www.arm.com

2.3.2 CP15

The ARM926EJ-S system control coprocessor (CP15) is used to configure and control instruction and data caches, Tightly-Coupled Memories (TCMs), Memory Management Unit (MMU), and other ARM subsystem functions. The CP15 registers are programmed using the MRC and MCR ARM instructions, when the ARM in a privileged mode such as supervisor or system mode.

2.3.3 MMU

The ARM926EJ-S MMU provides virtual memory features required by operating systems such as Linux, WindowCE, ultron, ThreadX, etc. A single set of two level page tables stored in main memory is used to control the address translation, permission checks and memory region attributes for both data and instruction accesses. The MMU uses a single unified Translation Lookaside Buffer (TLB) to cache the information held in the page tables. The MMU features are:

- Standard ARM architecture v4 and v5 MMU mapping sizes, domains and access protection scheme.
- Mapping sizes are:
  – 1MB (sections)
  – 64KB (large pages)
  – 4KB (small pages)
  – 1KB (tiny pages)
- Access permissions for large pages and small pages can be specified separately for each quarter of the page (subpage permissions)
- Hardware page table walks
- Invalidate entire TLB, using CP15 register 8
- Invalidate TLB entry, selected by MVA, using CP15 register 8
- Lockdown of TLB entries, using CP15 register 10

2.3.4 Caches and Write Buffer

The size of the Instruction Cache is 16KB, Data cache is 8KB. Additionally, the Caches have the following features:

- Virtual index, virtual tag, and addressed using the Modified Virtual Address (MVA)
- Four-way set associative, with a cache line length of eight words per line (32-bytes per line) and with two dirty bits in the Dcache
- Dcache supports write-through and write-back (or copy back) cache operation, selected by memory region using the C and B bits in the MMU translation tables.
- Critical-word first cache refilling
- Cache lockdown registers enable control over which cache ways are used for allocation on a line fill, providing a mechanism for both lockdown, and controlling cache corruption
- Dcache stores the Physical Address TAG (PA TAG) corresponding to each Dcache entry in the TAG RAM for use during the cache line write-backs, in addition to the Virtual Address TAG stored in the TAG RAM. This means that the MMU is not involved in Dcache write-back operations, removing the possibility of TLB misses related to the write-back address.

- Cache maintenance operations provide efficient invalidation of, the entire Dcache or Icache, regions of the Dcache or Icache, and regions of virtual memory.

The write buffer is used for all writes to a noncachable bufferable region, write-through region and write misses to a write-back region. A separate buffer is incorporated in the Dcache for holding write-back for cache line evictions or cleaning of dirty cache lines. The main write buffer has 16-word data buffer and a four-address buffer. The Dcache write-back has eight data word entries and a single address entry.

2.3.5 Tightly Coupled Memory (TCM)

ARM internal RAM is provided for storing real-time and performance-critical code/data and the Interrupt Vector table. ARM internal ROM enables non-EMIFA boot options, such as NAND and UART. The RAM and ROM memories interfaced to the ARM926EJ-S via the tightly coupled memory interface that provides for separate instruction and data bus connections. Since the ARM TCM does not allow instructions on the D-TCM bus or data on the I-TCM bus, an arbiter is included so that both data and instructions can be stored in the internal RAM/ROM. The arbiter also allows accesses to the RAM/ROM from extra-ARM sources (e.g., EDMA or other masters). The ARM926EJ-S has built-in DMA support for direct accesses to the ARM internal memory from a non-ARM master. Because of the time-critical nature of the TCM link to the ARM internal memory, all accesses from non-ARM devices are treated as DMA transfers.

Instruction and Data accesses are differentiated via accessing different memory map regions, with the instruction region from 0x0000 through 0x7FFF and data from 0x8000 through 0xFFFF. Placing the instruction region at 0x0000 is necesssary to allow the ARM Interrupt Vector table to be placed at 0x0000, as required by the ARM architecture. The internal 16-KB RAM is split into two physical banks of 8KB each, which allows simultaneous instruction and data accesses to be accomplished if the code and data are in separate banks.

2.3.6 Advanced High-performance Bus (AHB)

The ARM Subsystem uses the AHB port of the ARM926EJ-S to connect the ARM to the Config bus and the external memories. Arbiters are employed to arbitrate access to the separate D-AHB and I-AHB by the Config Bus and the external memories bus.

2.3.7 Embedded Trace Macrocell (ETM) and Embedded Trace Buffer (ETB)

To support real-time trace, the ARM926EJ-S processor provides an interface to enable connection of an Embedded Trace Macrocell (ETM). The ARM926ES-J Subsystem in DM644X also includes the Embedded Trace Buffer (ETB). The ETM consists of two parts:

- Trace Port provides real-time trace capability for the ARM9.
- Triggering facilities provide trigger resources, which include address and data comparators, counter, and sequencers.

The DM644X trace port is not pinned out and is instead only connected to the Embedded Trace Buffer. The ETB has a 4KB buffer memory. ETB enabled debug tools are required to read/interpret the captured trace data.

2.3.8 ARM Memory Mapping

The ARM memory map is shown in the Memory Map section of this document. The ARM has access to memories shown in the following sections.

2.3.8.1 ARM Internal Memories

The ARM has access to the following ARM internal memories:

- 16KB ARM Internal RAM on TCM interface, logically separated into two 8KB pages to allow simulatenous access on any given cycle if there are separate acecsses for code (I-TCM bus) and data (D-TCM) to the different memory regions.
- 16KB ARM Internal ROM

2.3.8.2 External Memories

The ARM has access to the following External memories:

- DDR2 Synchronous DRAM
- Asynchronous EMIF / NOR Flash / NAND Flash
- ATA/CF
- Flash card devices:
  - MMC/SD
  - xD
  - SmartMedia

2.3.8.3 DSP Memories

The ARM has access to the following DSP memories:

- L2 RAM
- L1P RAM
- L1D RAM

2.3.8.4 VICP Registers and Memories

The ARM has access to the registers and memories of the Video/Imaging Co-Processor (VICP) Subsystem. The VICP Subsystem consists of the Sequencer, IMX, and VLCD, and the memories associated with these modules. For complete details on the VICP Subsystem, refer to the Documentation Support Section of this document for the VICP Subsystem Guide.

2.3.8.5 ARM-DSP Integration

DM6446 ARM and DSP integration features are as follows:

- DSP visibility from ARM’s memory map, see the Memory Map section for details
- Boot Modes for DSP - see the Device Configurations section for details
- ARM control of DSP boot / reset - see the Device Configurations section for details
- ARM control of DSP isolation and powerdown / powerup - see the Device Configurations section
- ARM & DSP Interrupts - see the Interrupts section

2.3.9 Peripherals

The ARM9 has access to all of the peripherals on the DM6446 device with the exception of the VICP.

2.3.10 PLL Controller (PLLC)

The ARM Subsystem includes the PLL Controller. The PLL Controller contains a set of registers for configuring DM6446’s two internal PLLs (PLL1 and PLL2). The PLL Controller provides the following configuration and control:

- PLL Bypass Mode
- Set PLL multiplier parameters
- Set PLL divider parameters
- PLL power down
- Oscillator power down

The PLLs are briefly described in this document in the Clocking section. For more detailed information on the PLLs and PLL Controller register descriptions, see the Documentation Support section of this document for the ARM Subsystem Guide .

2.3.11 Power and Sleep Controller (PSC)

The ARM Subsystem includes the Power and Sleep Controller (PSC). Through register settings accessible by the ARM9, the PSC provides two levels of power savings: peripheral/module clock gating and power domain shut-off. Brief details on the PSC are given in the Power Supply section. For more detailed information and complete register descriptions for the PSC, see the Documentation Support section of this document for the ARM Subsystem Guide.

2.3.12 ARM Interrupt Controller (AINTC)

The ARM Interrupt Controller (AINTC) accepts device interrupts and maps them to either the ARM's IRQ (interrupt request) or FIQ (fast interrupt request). The ARM Interrupt Controller is briefly described in this document in the Interrupts section. For detailed information on the ARM Interrupt Controller, see the Documentation Support section of this document for the ARM Subsystem Guide.

2.3.13 System Module

The ARM Subsystem includes the System module. The System module consists of a set of registers for configuring and controlling a variety of system functions. For details and register descriptions for the System module, see the Device Configurations section and the Documentation Support section of this document for the ARM Subsystem Guide.

2.3.14 Power Management

DM6446 has several means of managing power consumption. There is extensive use of clock gating, which reduces the power used by global device clocks and individual peripheral clocks. The DSP and VICP power can be disabled through register settings. Voltage/Frequency scaling can be used to allow the user to lower the core power supply voltage if the frequency needs for a particular application are lower. Clock management can be utilized to reduce clock frequencies in order to reduce switching power. For more details on power management techniques, see the Device Configurations and Peripheral sections of this document and the Documentation Support section of this document for the ARM Subsystem Guide.

DM6446 gives the programmer full flexibility to use any and all of the previously mentioned capabilities to customize an optimal power management strategy. Several typical power management scenarios are described in the following sections.

2.3.14.1 Standby Power Mode

This mode consumes the lowest power, with the minimum set of modules kept alive that are required to wake up the chip to a higher power mode. DSP and coprocessor subsystems are not powered. The rest of the chip is powered and clocks are suspended, except for GPIO (interrupts), UARTs, I2C (in slave mode), and the PWM peripheral. PLLs are operating in bypass mode. 27-MHz clock is the only clock available to the system. DDR2 clock is suspended and the DDR2 Memory Controller is put into self-refresh mode.

2.3.14.2 Low-Power Mode

This mode is for the ARM to sustain some basic control functions. DSP and coprocessor subsystems are not powered. The rest of the chip is powered, but most clocks are suspended, except for ARM, GPIO, UARTs, SPI, I2C, PWMs, and Timers. PLLs are operating in bypass mode. 27-MHz clock is the only clock available to the system. ARM runs at 13.5 MHz, and handles all peripherals by direct access. DDR2 clock is suspended and DDR2 Memory Controller is put into self-refresh mode. ARM will not have access to DDR2 and its caches are either frozen or inaccessible.

2.3.14.3 Active Power Mode

The entire chip is powered. All modules operate at nominal clock frequency. Unused peripherals have their clocks suspended. Active peripherals have their clocks suspended when unneeded.

2.4 DSP Subsystem

The DSP Subsystem includes the following features:

- C64X+ DSP CPU
- 32KB L1 Program (L1P)/Cache (up to 32KB)
- 80KB L1 Data (L1D)/Cache (up to 32KB)
- 64KB Unified Mapped RAM/Cache (L2)
- Little endian

2.4.1 C64X+ DSP CPU Description

The C64x+ Central Processing Unit (CPU) consists of eight functional units, two register files, and two data paths as shown in Figure 2-1. The two general-purpose register files (A and B) each contain 32 32-bit registers for a total of 64 registers. The general-purpose registers can be used for data or can be data address pointers. The data types supported include packed 8-bit data, packed 16-bit data, 32-bit data, 40-bit data, and 64-bit data. Values larger than 32 bits, such as 40-bit-long or 64-bit-long values are stored in register pairs, with the 32 LSBs of data placed in an even register and the remaining 8 or 32 MSBs in the next upper register (which is always an odd-numbered register).

The eight functional units (.M1, .L1, .D1, .S1, .M2, .L2, .D2, and .S2) are each capable of executing one instruction every clock cycle. The .M functional units perform all multiply operations. The .S and .L units perform a general set of arithmetic, logical, and branch functions. The .D units primarily load data from memory to the register file and store results from the register file into memory.

The C64x+ CPU extends the performance of the C64x core through enhancements and new features.

Each C64x+ .M unit can perform one of the following each clock cycle: one 32 x 32 bit multiply, one 16 x 32 bit multiply, two 16 x 16 bit multiplies, two 16 x 32 bit multiplies, two 16 x 16 bit multiplies with add/subtract capabilities, four 8 x 8 bit multiplies, four 8 x 8 bit multiplies with add operations, and four 16 x 16 multiplies with add/subtract capabilites (including a complex multiply). There is also support for Galois field mutiplication for 8-bit and 32-bit data. Many communications algorithms such as FFTs and modems require complex multiplication. The complex multiply (CMPY) instruction takes for 16-bit inputs and produces a 32-bit real and a 32-bit imaginary output. There are also complex multiplies with rounding capability that produces one 32-bit packed output that contain 16-bit real and 16-bit imaginary values. The 32 x 32 bit multiply instructions provide the extended precision necessary for audio and other high-precision algorithms on a variety of signed and unsigned 32-bit data types.

The .L or (Arithmetic Logic Unit) now incorporates the ability to do parallel add/subtract operations on a pair of common inputs. Versions of this instruction exist to work on 32-bit data or on pairs of 16-bit data performing dual 16-bit add and subtracts in parallel. There are also saturated forms of these instructions.

The C64x+ core enhances the .S unit in several ways. In the C64x core, dual 16-bit MIN2 and MAX2 comparisons were only available on the .L units. On the C64x+ core they are also available on the .S unit which increases the performance of algorithms that do searching and sorting. Finally, to increase data packing and unpacking throughput, the .S unit allows sustained high performance for the quad 8-bit/16-bit and dual 16-bit instructions. Unpack instructions prepare 8-bit data for parallel 16-bit operations. Pack instructions return parallel results to output precision including saturation support.

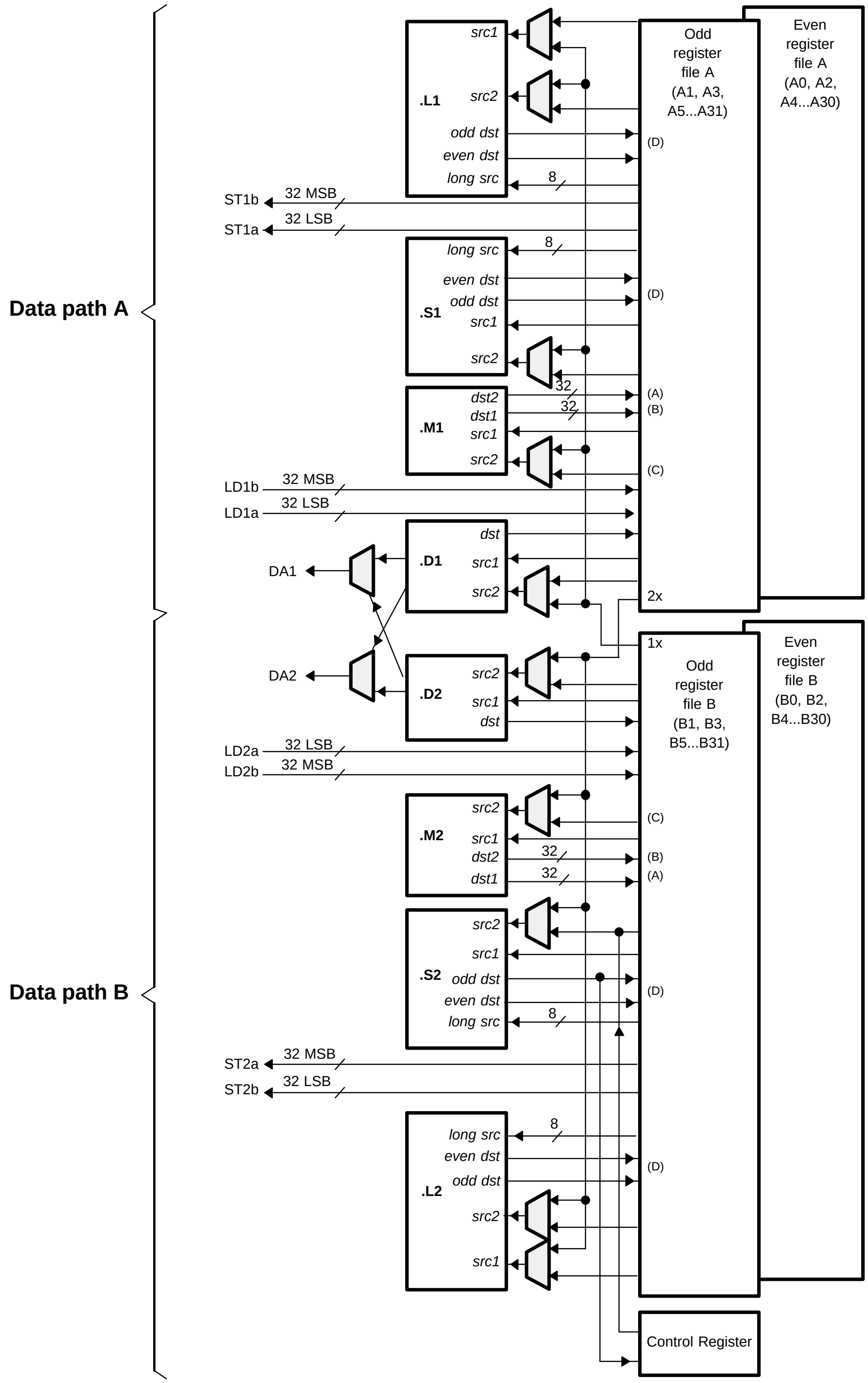
Other new features include:

- **SPLOOP** - A small instruction buffer in the CPU that aids in creation of software pipelining loops where multiple iterations of a loop are executed in parallel. The SPLOOP buffer reduces the code size associated with software pipelining. Futhermore, loops in the SPLOOP buffer are fully interruptible.
- **Compact Instructions** - The native instruction size for the C6000 devices is 32 bits. Many common instructions such as MPY, AND, OR, ADD, and SUB can be expressed as 16 bits if the C64x+ compiler can restrict the code to use certain registers in the register file. This compression is performed by the code generation tools.

- **Instruction Set Enhancement** - As noted above, there are new instructions such as 32-bit multiplications, complex multiplications, packing, sorting, bit manipulation, and 32-bit Galois field multiplication.
- **Exceptions Handling** - Intended to aid the programmer in isolating bugs. The C64x+ CPU is able to detect and respond to exceptions, both from internally detected sources (such as illegal op-codes) and from system events (such as a watchdog time expiration).
- **Privilege** - Defines user and supervisor modes of operation, allowing the operating system to give a basic level of protection to sensitive resources. Local memory is divided into multiple pages, each with read, write, and execute permissions.
- **Time-Stamp Counter** - Primarily targeted for Real-Time Operating System (RTOS) robustness, a free-running time-stamp counter is implemented in the CPU which is ***not*** sensitive to system stalls.

For more details on the C64x+ CPU and its enhancements over the C64x architecture, see the following documents:

- *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (literature number SPRU732)
- *TMS320C64x Technical Overview* (literature number SPRU395)



A. On .M unit, *dst2* is 32 MSB.
B. On .M unit, *dst1* is 32 LSB.
C. On C64x CPU .M unit, *src2* is 32 bits; on C64x+ CPU .M unit, *src2* is 64 bits.
D. On .L and .S units, *odd dst* connects to odd register files and *even dst* connects to even register files.

Figure 2-1. TMS320C64x+™ CPU (DSP Core) Data Paths

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2.4.1.1 C64X+ CPU Cache Registers

Table 2-2 shows a memory map of the C64x+ CPU cache Registers for the device.

Table 2-2. C64x+ Cache Registers

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x0184 0000	L2CFG	L2 Cache configuration register
0x0184 0020	L1PCFG	L1P Size Cache configuration register
0x0184 0024	L1PCC	L1P Freeze Mode Cache configuration register
0x0184 0040	L1DCFG	L1D Size Cache configuration register
0x0184 0044	L1DCC	L1D Freeze Mode Cache configuration register
0x0184 0048 - 0x0184 0FFC	-	Reserved
0x0184 1000	EDMAWEIGHT	L2 EDMA access control register
0x0184 1004 - 0x0184 1FFC	-	Reserved
0x0184 2000	L2ALLOC0	L2 allocation register 0
0x0184 2004	L2ALLOC1	L2 allocation register 1
0x0184 2008	L2ALLOC2	L2 allocation register 2
0x0184 200C	L2ALLOC3	L2 allocation register 3
0x0184 2010 - 0x0184 3FFF	-	Reserved
0x0184 4000	L2WBAR	L2 writeback base address register
0x0184 4004	L2WWC	L2 writeback word count register
0x0184 4010	L2WIBAR	L2 writeback invalidate base address register
0x0184 4014	L2WIWC	L2 writeback invalidate word count register
0x0184 4018	L2IBAR	L2 invalidate base address register
0x0184 401C	L2IWC	L2 invalidate word count register
0x0184 4020	L1PIBAR	L1P invalidate base address register
0x0184 4024	L1PIWC	L1P invalidate word count register
0x0184 4030	L1DWIBAR	L1D writeback invalidate base address register
0x0184 4034	L1DWIWC	L1D writeback invalidate word count register
0x0184 4038	-	Reserved
0x0184 4040	L1DWBAR	L1D Block Writeback
0x0184 4044	L1DWWC	L1D Block Writeback
0x0184 4048	L1DIBAR	L1D invalidate base address register
0x0184 404C	L1DIWC	L1D invalidate word count register
0x0184 4050 - 0x0184 4FFF	-	Reserved
0x0184 5000	L2WB	L2 writeback all register
0x0184 5004	L2WBINV	L2 writeback invalidate all register
0x0184 5008	L2INV	L2 Global Invalidate without writeback
0x0184 500C - 0x0184 5027	-	Reserved
0x0184 5028	L1PINV	L1P Global Invalidate
0x0184 502C - 0x0184 5039	-	Reserved
0x0184 5040	L1DWB	L1D Global Writeback
0x0184 5044	L1DWBINV	L1D Global Writeback with Invalidate
0x0184 5048	L1DINV	L1D Global Invalidate without writeback
0x0184 8000 - 0x0184 8004	MAR0 - MAR1	Reserved 0x0000 0000 - 0x01FF FFFF
0x0184 8008 - 0x0184 8024	MAR2 - MAR9	Memory Attribute Registers for EMIFA 0x0200 0000 - 0x09FF FFFF
0x0184 8028 - 0x0184 802C	MAR10 - MAR11	Reserved 0x0A00 0000 - 0x0BFF FFFF
0x0184 8030 - 0x0184 803C	MAR12 - MAR15	Memory Attribute Registers for VLYNQ 0x0C00 0000 - 0x0FFF FFFF
0x0184 8040 - 0x0184 8104	MAR16 - MAR65	Reserved 0x1000 0000 - 0x41FF FFFF

Table 2-2. C64x+ Cache Registers (continued)

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x0184 8108 - 0x0184 813C	MAR66 - MAR79	Memory Attribute Registers for EMIFA/VLYNQ Shadow 0x4200 0000 - 0x4FFF FFFF
0x0184 8140	MAR80 - MAR127	Reserved 0x5000 0000 - 0x7FFF FFFF
0x0184 8200 - 0x0184 823C	MAR128 - MAR143	Memory Attribute Registers for DDR2 0x8000 0000 - 0x8FFF FFFF
0x0184 8240 - 0x0184 83FC	MAR144 - MAR255	Reserved 0x9000 0000 - 0xFFFF FFFF

2.4.2 DSP Memory Mapping

The DSP memory map is shown in Section 2.5. Configuration of the control registers for DDR2, EMIFA, and ARM Internal RAM is supported by the ARM. The DSP has access to memories shown in the following sections.

2.4.2.1 ARM Internal Memories

The DSP has access to the 16KB ARM Internal RAM on the ARM D-TCM interface (i.e., data only).

2.4.2.2 External Memories

The DSP has access to the following External memories:

- DDR2 Synchronous DRAM
- Asynchronous EMIF / NOR Flash

2.4.2.3 DSP Internal Memories

The DSP has access to the following DSP memories:

- L2 RAM
- L1P RAM
- L1D RAM

2.4.2.4 VICP Registers and Memories

The DSP has access to the registers and memories of the VICP Subsystem. The VICP Subsystem consists of the Sequencer, IMX, and VLCD, and the memories associated with these modules.

The VICP register descriptions are shown in the Table 2-3 - Table 2-6.

For complete details on the VICP Subsystem, refer to the VICP Subsystem Guide.

Table 2-3. Imaging Coprocessors (VICP) Register Descriptions

Address	Register	Description
0x01CC 0400	CLKC	Clock Controller
0x01CC 0404	RSV	Reserved
0x01CC 0998	BUFSW	Buffer Switch
0x01CC 0A08	RSV	Reserved
0x01CC 1698	INTC_GEN	Interrupt Generation
0x01CC 1702	INTC_CFG	Sequencer Interrupt Controller Configuration
0x01CC 1712	INTC_STAT	Sequencer Interrupt or Sync State
0x01CC 1716	INTC_MSK	Sequencer Synclinterrupt Mask
0x01CC 1720	INTC_ARMCFG	ARM-to-Sequencer Interrupt Configuration
0x01CC 1730	INTC_DSPCFG	DSP-to-Sequencer Interrupt Configuration
0x01CC 1734	INTC_SDMACFG	System DMA-to-Sequencer Interrupt Configuration
0x01CC 1744	INTC_LDMACFG	Local DMA-to-Sequencer Interrupt Configuration
0x01CC 1748	INTC_IMXCFG	iMX-to-Sequencer Interrupt Configuration
0x01CC 1752	INTC_VLCDCFG	VLCD-to-Sequencer Interrupt Configuration

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Table 2-3. Imaging Coprocessors (VICP) Register Descriptions (continued)

Address	Register	Description
0x01CC 1762	RSV	Reserved
0x01CC 1766	RSV	Reserved
0x01CC 1776	INTC_DBGC	Sequencer Debug Control
0x01CC 1780	INTC_HWBPA	Sequencer Hardware Breakpoint Address
0x01CC 1784	INTC_BPST	Sequencer Breakpoint Status
0x01CC 1794	INTC_TMR	Sequencer Performance Timer
0x01CC 1798	INTC_AERR	Memory Access Error Status
0x01CC 1808	RSV	Reserved
0x01CC 1C96	LDMA_ADR	Local DMA Address
0x01CC 1D06	LDMA_CTRL	Local DMA Control
0x01CC 1D10	RSV	Reserved
0x01CC 4532	CFG_DMA	System CFG Bus DMA Setup
0x01CC 4536	CFG_RADDR	System CFG Bus Read Address
0x01CC 4546	CFG_WADDR	Systen CFG Bus Write Address
0x01CC 4550	CFG_RDATA	CFG bus Request Read Data
0x01CC 4560	CFG_WDATA	CFG bus Request Write Data

Table 2-4. Imaging Accelerator (IMX) Register Descriptions

Address	Acronym	Register Description
0x01CC 0900	EMU	IMX EMU Register
0x01CC 0904	START	IMX Start Register
0x01CC 0908	INTR_EN	IMX INTR Enable Register
0x01CC 0918	BUSY	IMX Busy Register
0x01CC 0922	CMDPTR	IMX Command Pointer
0x01CC 0932	ABORT	IMX Abort Register
0x01CC 0933 - 0x01CC 09FF	Reserved	Reserved

Table 2-5. Imaging Coprocessor Variable Length Coder/Decoder Register Descriptions (VLCD)

Address	Register	Description
0x01CC 0A00	START	VLCD Start Register
0x01CC 0A02	MODE	VLCD Mode Register
0x01CC 0A04	QIN_ADDR	Quantization Input Address Register
0x01CC 0A06	QOUT_ADDR	Quantization Output Address Register
0x01CC 0A08	IQIN_ADDR	Inverse Quantization Input Address Register
0x01CC 0A16	IQOUT_ADDR	Inverse Quantization Output Address Register
0x01CC 0A18	VLCDIN_ADDR	VLCD Input Address
0x01CC 0A20	VLCDOUT_ADDR	VLCD Output Address
0x01CC 0A22	DC_PRED0	Quantization DC Predictor 0 Register
0x01CC 0A24	DC_PRED1	Quantization DC Predictor 1 Register
0x01CC 0A32	DC_PRED2	Quantization DC Predictor 2 Register
0x01CC 0A34	DC_PRED3	Quantization DC Predictor 3 Register
0x01CC 0A36	DC_PRED4	Quantization DC Predictor 4 Register
0x01CC 0A38	DC_PRED5	Quantization DC Predictor 5 Register
0x01CC 0A40	IDC_PRED0	Inverse Quantization DC Predictor 0 Register
0x01CC 0A48	IDC_PRED1	Inverse Quantization DC Predictor 1 Register

Table 2-5. Imaging Coprocessor Variable Length Coder/Decoder Register Descriptions (VLCD) (continued)

Address	Register	Description
0x01CC 0A50	IDC_PRED2	Inverse Quantization DC Predictor 2 Register
0x01CC 0A52	IDC_PRED3	Inverse Quantization DC Predictor 3 Register
0x01CC 0A54	IDC_PRED4	Inverse Quantization DC Predictor 4 Register
0x01CC 0A56	IDC_PRED5	Inverse Quantization DC Predictor 5 Register
0x01CC 0A64	MPEG_INVQ	MPEG Inverse Quantization Scale Register
0x01CC 0A66	MPEG_Q	MPEG Quantization Scale Register
0x01CC 0A68	MPEG_DELTA_Q	MPEG Quantization Delta Register
0x01CC 0A70	MPEG_DELTA_IQ	MPEG Inverse Quantization Delta Register
0x01CC 0A72	MPEG_THRED	MPEG Thred Register
0x01CC 0A80	MPEG_CBP	MPEG Coded Block Pattern Register
0x01CC 0A82	LUMA_VECTOR	LUMA Bit Vector Register
0x01CC 0A84	HUFFTAB_DCY	Huffman DC Y Table Base Address Register
0x01CC 0A86	HUFFTAB_DCUV	Huffman DC UV Table Base Address Register
0x01CC 0A88	HUFFTAB_AC0	Huffman AC0 Table Base Address Register
0x01CC 0A96	HUFFTAB_AC1	Huffman AC1 Table Base Address Register
0x01CC 0A98	OFLEV_MAXOTAB	MPEG Max 0 Level Table Base Address Register
0x01CC 0A00	OFLEV_MAX1TAB	MPEG Max 1 Level Table Base Address Register
0x01CC 0A02	CTLTAB_DCY	DC Y Control Lookup Table Base Address Register
0x01CC 0B04	CTLTAB_DCUV	DC UV Control Lookup Table Base Address Register
0x01CC 0B12	CTLTAB_AC0	AC0 Control Lookup Table Base Address Register
0x01CC 0B14	CTLTAB_AC1	AC1 Control Lookup Table Base Address Register
0x01CC 0B16	OFFSET_DCY	DC Y Symbol Lookup Table Address Offset Register
0x01CC 0B18	OFFSET_DCUV	DC UV Symbol Lookup Table Address Offset Register
0x01CC 0B20	OFFSET_AC0	AC0 Symbol Lookup Table Address Offset Register
0x01CC 0B28	OFFSET_AC1	AC1 Symbol Lookup Table Address Offset Register
0x01CC 0B30	SYMTAB_DCY	DC Y Symbol Lookup Table Base Address Register
0x01CC 0B32	SYMTAB_DCUV	DC UV Symbol Lookup Table Base Address Register
0x01CC 0B34	SYMTAB_AC0	AC0 Symbol Lookup Table Base Address Register
0x01CC 0B36	SYMTAB_AC1	AC1 Symbol Lookup Table Base Address Register
0x01CC 0B44	CTL	VLD Control Register
0x01CC 0B46	VLD_NRBIT_DC	DC Number of Bits Register
0x01CC 0B48	VLD_NRBIT_AC	AC Number of Bits Register
0x01CC 0B50	BITS_BPTR	Bits Pointer Register
0x01CC 0B52	BITS_WORD	Bits Word Register
0x01CC 0C56	BYTE_ALIGN	Byte Align Register
0x01CC 0C58	HEAD_ADDR	Header Address Register
0x01CC 0C60	HEAD_NUM	Number of Header Data Register
0x01CC 0C62	QIQ_CONFIG0	QIQ Configuration Register #0
0x01CC 0C64	QIQ_CONFIG1	QIQ Configuration Register #1
0x01CC 0C72	QIQ_CONFIG2	QIQ Configuration Register #2
0x01CC 0C74	QIQ_CONFIG3	QIQ Configuration Register #3
0x01CC 0C76	QIQ_CONFIG4	QIQ Configuration Register #4
0x01CC 0C78	QIQ_CONFIG5	QIQ Configuration Register #5
0x01CC 0C80	VLD_ERRCTL	VLD Error Control Register
0x01CC 0C88	VLD_ERRSTAT	VLD Error Status Register
0x01CC 0C90	RING_START	Ring Buffer Start Address Register

Table 2-5. Imaging Coprocessor Variable Length Coder/Decoder Register Descriptions (VLCD) (continued)

Address	Register	Description
0x01CC 0C92	RING_END	Ring Buffer End Address Register
0x01CC 0C94	CLKCTRL	VLD Prefix Register - DC
0x01CC 0C96	VLD_PREFIX_DC	VLD Prefix Register - DC
0x01CC 0D04	VLD_PREFIX_AC	VLD Prefix Register - AC
0x01CC 0D06	WMV9_CFG	WMV9 Configuration
0x01CC 0D08	FIRST_FRAME	First Frame
0x01CC 0D10	H264_MODE	H.264 Mode
0x01CC 0D12	NRBITS_THRED	First Frame

Table 2-6. Imaging Coprocessor Sequencer Register Descriptions (SEQ)

Address	Acronym	Description
0x01CC 0B00	Reserved	Reserved
0x01CC 0B04	CTRL	Sequencer Control Register
0x01CC 0B08	BOOT	Sequencer Boot Address Register
0x01CC 0B18	AREG	A Register of Sequencer (debug)
0x01CC 0B22	BREG	B Register of Sequencer (debug)
0x01CC 0B36	CREG	C Register of Sequencer (debug)
0x01CC 0B40	PREG	P1 Register of Sequencer (debug)
0x01CC 0B40	P2REG	P2 Register of Sequencer (debug)
0x01CC 0B50	PCREG	PC Register of Sequencer (debug)
0x01CC 0B54	STATUS	Status Register of Sequencer (debug)
0x01CC 0B58 - 0x01CC 0BFF	Reserved	Reserved

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2.4.3 Peripherals

The DSP has controllability for the following peripherals:

- VICP
- EDMA
- ASP
- 2 Timers (Timer 0 and Timer1) that can each be configured as 1 64-bit or 2 32-bit timers

2.4.4 DSP Interrupt Controller

The DSP Interrupt Controller accepts device interrupts and appropriately maps them to the DSP's available interrupts. The DSP Interrupt Controller is briefly described in this document in the Interrupts section. For more detailed on the DSP Interrupt Controller, see the Documentation Support section of this document for the C64x+ CPU User's Guide.

2.5 Memory Map Summary

Table 2-7 shows the memory map address ranges of the device. Table 2-8 depicts the expanded map of the Configuration Space (0x0180 0000 through 0x0FFF FFFF). The device has multiple on-chip memories associated with its two processors and various subsystems. To help simplify software development a unified memory map is used where possible to maintain a consistent view of device resources across all bus masters.

Table 2-7. Memory Map Summary

START ADDRESS	END ADDRESS	SIZE (Bytes)	ARM	C64x+	EDMA/ PERIPHERAL	VPSS
0x0000 0000	0x0000 1FFF	8K	ARM RAM0 (Instruction)	Reserved	Reserved	Reserved
0x0000 2000	0x0000 3FFF	8K	ARM RAM1 (Instruction)	Reserved	Reserved	Reserved
0x0000 4000	0x0000 7FFF	16K	ARM ROM (Instruction)	Reserved	Reserved	Reserved
0x0000 8000	0x0000 9FFF	8K	ARM RAM0 (Data)	Reserved	ARM RAM0	Reserved
0x0000 A000	0x0000 BFFF	8K	ARM RAM1 (Data)	Reserved	ARM RAM1	Reserved
0x0000 C000	0x0000 FFFF	16K	ARM ROM (Data)	Reserved	ARM ROM	Reserved
0x0001 0000	0x000F FFFF	960K	Reserved	Reserved	Reserved	Reserved
0x0010 0000	0x001F FFFF	1M	Reserved	VICP	Reserved	Reserved
0x0020 0000	0x007F FFFF	6M	Reserved	Reserved	Reserved	Reserved
0x0080 0000	0x0080 FFFF	64K	Reserved	L2 RAM/Cache	Reserved	Reserved
0x0081 0000	0x00DF FFFF	6080K	Reserved	Reserved	Reserved	Reserved
0x00E0 0000	0x00E0 3FFF	16K	Reserved	Reserved	Reserved	Reserved
0x00E0 4000	0x00E0 7FFF	16K	Reserved	Reserved	Reserved	Reserved
0x00E0 8000	0x00E0 FFFF	32K	Reserved	L1P Cache	Reserved	Reserved
0x00E1 0000	0x00F0 3FFF	976K	Reserved	Reserved	Reserved	Reserved
0x00F0 4000	0x00F0 FFFF	48K	Reserved	L1D RAM	Reserved	Reserved
0x00F1 0000	0x00F1 7FFF	32K	Reserved	L1D Cache	Reserved	Reserved
0x00F1 8000	0x017F FFFF	9120K	Reserved	Reserved	Reserved	Reserved
0x0180 0000	0x01BB FFFF	3840K	Reserved	CFG Space	Reserved	Reserved
0x01BC 0000	0x01BC 0FFF	4K	ARM ETB Memory	CFG Space	Reserved	Reserved
0x01BC 1000	0x01BC 17FF	2K	ARM ETB Registers	CFG Space	Reserved	Reserved
0x01BC 1800	0x01BC 18FF	256	ARM IceCrusher	CFG Space	Reserved	Reserved
0x01BC 1900	0x01BC FFFF	59136	Reserved	CFG Space	Reserved	Reserved
0x01BD 0000	0x01BF FFFF	192K	Reserved	CFG Space	Reserved	Reserved
0x01C0 0000	0x01FF FFFF	4M	CFG Bus Peripherals	CFG Bus Peripherals	CFG Bus Peripherals	Reserved
0x0200 0000	0x09FF FFFF	128M	EMIFA (Code and Data)	EMIFA (Data)	EMIFA (Data)	Reserved
0x0A00 0000	0x0BFF FFFF	32M	Reserved	Reserved	Reserved	Reserved
0x0C00 0000	0x0FFF FFFF	64M	VLYNQ (Remote)	Reserved	VLYNQ (Remote)	Reserved
0x1000 0000	0x1000 7FFF	32K	Reserved	Reserved	Reserved	Reserved
0x1000 8000	0x1000 9FFF	8K	Reserved	ARM RAM0	ARM RAM0	Reserved
0x1000 A000	0x1000 BFFF	8K	Reserved	ARM RAM1	ARM RAM1	Reserved
0x1000 C000	0x1000 FFFF	16K	Reserved	ARM ROM	ARM ROM	Reserved
0x1001 0000	0x110F FFFF	17344K	Reserved	Reserved	Reserved	Reserved
0x1110 0000	0x111F FFFF	1M	VICP	VICP	VICP	Reserved
0x1120 0000	0x117F FFFF	6M	Reserved	Reserved	Reserved	Reserved
0x1180 0000	0x1180 FFFF	64K	L2 RAM/Cache	L2 RAM/Cache	L2 RAM/Cache	Reserved
0x1181 0000	0x11DF FFFF	6080K	Reserved	Reserved	Reserved	Reserved
0x11E0 0000	0x11E0 3FFF	16K	Reserved	Reserved	Reserved	Reserved
0x11E0 4000	0x11E0 7FFF	16K	Reserved	Reserved	Reserved	Reserved
0x11E0 8000	0x11E0 FFFF	32K	L1P Cache	L1P Cache	L1P Cache	Reserved
0x11E1 0000	0x11F0 3FFF	976K	Reserved	Reserved	Reserved	Reserved
0x11F0 4000	0x11F0 FFFF	48K	L1D RAM	L1D RAM	L1D RAM	Reserved
0x11F1 0000	0x11F1 7FFF	32K	L1D RAM/Cache	L1D RAM/Cache	L1D RAM/Cache	Reserved
0x11F1 8000	0x1FFF FFFF	241M-32K	Reserved	Reserved	Reserved	Reserved

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Memory Map Summary (continued)

START ADDRESS	END ADDRESS	SIZE (Bytes)	ARM	C64x+	EDMA/ PERIPHERAL	VPSS
0x2000 0000	0x2000 7FFF	32K	DDR2 Control Regs	DDR2 Control Regs	DDR2 Control Regs	Reserved
0x2000 8000	0x41FF FFFF	544M-32k	Reserved	Reserved	Reserved	Reserved
0x4200 0000(1)	0x4FFF FFFF	224M	Reserved	EMIFA/VLYNQ Shadow	EMIFA/VLYNQ Shadow	Reserved
0x5000 0000	0x7FFF FFFF	768M	Reserved	Reserved	Reserved	Reserved
0x8000 0000	0x8FFF FFFF	256M	DDR2	DDR2	DDR2	DDR2
0x9000 0000	0xFFFF FFFF	1792M	Reserved	Reserved	Reserved	Reserved

(1) EMIFA shadow memory started a 0x4200 0000 is physically the same memory as location 0x0200 0000. Memory range 0x200 0000 through 0x09FF FFFF should only be used by C64x+ for data accesses. Memory range 0x4200 0000 through 0x4FFF FFFF can be used by C64x+ for both code execution and data accesses.

Table 2-8. Configuration Memory Map Summary

START ADDRESS	END ADDRESS	SIZE (Bytes)	ARM/EDMA/SEQUENCER	C64x+
0x0180 0000	0x0180 FFFF	64K	Reserved	C64x+ Interrupt Controller
0x0181 0000	0x0181 0FFF	4K	Reserved	C64x+ Powerdown Controller
0x0181 1000	0x0181 1FFF	4K	Reserved	C64x+ Security ID
0x0181 2000	0x0181 2FFF	4K	Reserved	C64x+ Revision ID
0x0182 0000	0x0182 FFFF	64K	Reserved	C64x+ EMC
0x0183 0000	0x0183 FFFF	64K	Reserved	Reserved
0x0184 0000	0x0184 FFFF	64K	Reserved	C64x+ Memory System
0x0185 0000	0x0187 FFFF	192K	Reserved	Reserved
0x0188 0000	0x01BB FFFF	3328K	Reserved	Reserved
0x01BC 0000	0x01BC 00FF	256	Reserved	AET Registers
0x01BC 0100	0x01BC 01FF	256	Reserved	Pin Manager and Trace
0x01BC 0400	0x01BC 042F	48	Reserved	Reserved
0x01BC 0430	0x01BC 044F	208	Reserved	Reserved
0x01BC 0500	0x01BC FFFF	64255	Reserved	Reserved
0x01BD 0000	0x01BF FFFF	192K	Reserved	Reserved
0x01C0 0000	0x01C0 FFFF	64K	EDMA CC	EDMA CC
0x01C1 0000	0x01C1 03FF	1K	EDMA TC0	EDMA TC0
0x01C1 0400	0x01C1 07FF	1K	EDMA TC1	EDMA TC1
0x01C1 8800	0x01C1 9FFF	6K	Reserved	Reserved
0x01C1 A000	0x01C1 FFFF	24K	Reserved	Reserved
0x01C2 0000	0x01C2 03FF	1K	UART0	Reserved
0x01C2 0400	0x01C2 07FF	1K	UART1	Reserved
0x01C2 0800	0x01C2 0BFF	1K	UART2	Reserved
0x01C2 0C00	0x01C2 0FFF	1K	Reserved	Reserved
0x01C2 1000	0x01C2 13FF	1K	I2C	Reserved
0x01C2 1400	0x01C2 17FF	1K	Timer0	Timer0
0x01C2 1800	0x01C2 1BFF	1K	Timer1	Timer1
0x01C2 1C00	0x01C2 1FFF	1K	Timer2 (WatchDog)	Reserved
0x01C2 2000	0x01C2 23FF	1K	PWM0	Reserved
0x01C2 2400	0x01C2 27FF	1K	PWM1	Reserved
0x01C2 2800	0x01C2 2BFF	1K	PWM2	Reserved
0x01C2 2C00	0x01C3 FFFF	117K	Reserved	Reserved

Configuration Memory Map Summary (continued)

START ADDRESS	END ADDRESS	SIZE (Bytes)	ARM/EDMA/SEQUENCER	C64x+
0x01C4 0000	0x01C4 07FF	2K	System Module	System Module
0x01C4 0800	0x01C4 0BFF	1K	PLL Controller 1	Reserved
0x01C4 0C00	0x01C4 0FFF	1K	PLL Controller 2	Reserved
0x01C4 1000	0x01C4 1FFF	4K	Power and Sleep Controller	Power and Sleep Controller
0x01C4 2000	0x01C4 202F	48	Reserved	Reserved
0x01C4 2030	0x01C4 2033	4	DDR2 VTP Reg	DDR2 VTP Reg
0x01C4 2034	0x01C4 23FF	1K - 52	Reserved	Reserved
0x01C4 2400	0x01C4 7FFF	23K	Reserved	Reserved
0x01C4 8000	0x01C4 83FF	1K	ARM Interrupt Controller	Reserved
0x01C4 8400	0x01C5 FFFF	95K	Reserved	Reserved
0x01C6 0000	0x01C6 3FFF	16K	Reserved	Reserved
0x01C6 4000	0x01C6 5FFF	8K	USB2.0 Regs / RAM	Reserved
0x01C6 6000	0x01C6 67FF	2K	ATA/CF	Reserved
0x01C6 6800	0x01C6 6FFF	2K	SPI	Reserved
0x01C6 7000	0x01C6 77FF	2K	GPIO	Reserved
0x01C6 7800	0x01C6 7FFF	2K	Reserved	Reserved
0x01C6 8000	0x01C6 FFFF	32K	Reserved	Reserved
0x01C7 0000	0x01C7 3FFF	16K	VPSS Regs	Reserved
0x01C7 4000	0x01C7 FFFF	48K	Reserved	Reserved
0x01C8 0000	0x01C8 0FFF	4K	EMAC Control Regs	Reserved
0x01C8 1000	0x01C8 1FFF	4K	EMAC Control Module Regs	Reserved
0x01C8 2000	0x01C8 3FFF	8K	EMAC Contol Module RAM	Reserved
0x01C8 4000	0x01C8 47FF	2K	MDIO Control Regs	Reserved
0x01C8 4800	0x01C8 4FFF	2K	Reserved	Reserved
0x01C8 5000	0x01CB FFFF	236K	Reserved	Reserved
0x01CC 0000	0x01CD FFFF	128K	Image Coprocessor	Image Coprocessor
0x01CE 0000	0x01CF FFFF	128K	Reserved	Reserved
0x01D0 0000	0x01DF FFFF	1M	Reserved	Reserved
0x01E0 0000	0x01E0 0FFF	4K	EMIFA Control	Reserved
0x01E0 1000	0x01E0 1FFF	4K	VLYNQ Control Regs	Reserved
0x01E0 2000	0x01E0 3FFF	8K	ASP	ASP
0x01E0 4000	0x01E0 FFFF	48K	Reserved	Reserved
0x01E1 0000	0x01E1 FFFF	64K	MMC/SD	Reserved
0x01E2 0000	0x01E3 FFFF	128K	Reserved	Reserved
0x01E4 0000	0x01FF FFFF	1792K	Reserved	Reserved
0x0200 0000	0x03FF FFFF	32M	EMIFA Data (CE0)	EMIFA Data (CE0)
0x0400 0000	0x05FF FFFF	32M	EMIFA Data (CE1)	EMIFA Data (CE1)
0x0600 0000	0x07FF FFFF	32M	EMIFA Data (CE2)	EMIFA Data (CE2)
0x0800 0000	0x09FF FFFF	32M	EMIFA Data (CE3)	EMIFA Data (CE3)
0x0A00 0000	0x0BFF FFFF	32M	Reserved	Reserved
0x0C00 0000	0x0FFF FFFF	64M	VLYNQ (Remote)	Reserved

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2.6 Pin Assignments

Extensive use of pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using a combination of hardware configuration at device reset and software programmable register settings.

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2.6.1 Pin Map (Bottom View)

Figure 2-2 through Figure 2-5 show the bottom view of the package pin assignments in four quadrants (A, B, C, and D).

	1	2	3	4	5	6	7	8	9	10	
W	RSV3	DDR_D[4]	DDR_D[7]	DDR_D[9]	DDR_D[12]	DDR_D[14]	DDR_CLK0	$\overline{\text{DDR\_CLK0}}$	DDR_A[12]	DDR_A[11]	W
V	DDR_D[2]	DDR_D[3]	DDR_D[6]	DDR_D[8]	DDR_D[11]	DDR_D[13]	DDR_D[15]	DDR_CKE	DDR_BS[1]	DDR_A[8]	V
U	DDR_D[0]	DDR_D[1]	DDR_D[5]	DDR_DQS[0]	DDR_D[10]	DDR_DQS[1]	$\overline{\text{DDR\_RAS}}$	DDR_BS[0]	DDR_BS[2]	DDR_A[10]	U
T	EM_CS5/ GPIO8/ VLYNQ_CLK	EM_CS4/ GPIO9/ VLYNQ_ SCRUN	EM_A[21]/ GPIO10/ VLYNQ_TXD0	DDR_ DQM[0]	DV_{DDR2}	DDR_ DQM[1]	$\overline{\text{DDR\_CAS}}$	$\overline{\text{DDR\_WE}}$	$\overline{\text{DDR\_CS}}$	DDR_VDDDLL	T
R	EM_A[12]/ GPIO19	EM_A[17]/ GPIO14/ VLYNQ_TXD2	EM_A[20]/ GPIO11/ VLYNQ_RXD0	EM_A[19]/ GPIO12/ VLYNQ_TXD1	EM_A[16]/ GPIO15/ VLYNQ_RXD2	V_{SS}	V_{SS}	RSV7	DV_{DDR}	V_{SS}	R
P	EM_A[10]/ GPIO21	EM_A[11]/ GPIO20	EM_A[15]/ GPIO16/ VLYNQ_TXD3	EM_A[14]/ GPIO17/ VLYNQ_RXD3	EM_A[18]/ GPIO13/ VLYNQ_RXD1	DV_{DDR}	V_{SS}	DV_{DDR}	V_{SS}	DV_{DDR}	P
N	EM_A[6]/ GPIO25	EM_A[7]/ GPIO24	EM_A[8]/ GPIO23	EM_A[13]/ GPIO18	DV_{DD18}	V_{SS}	DV_{DDR}	V_{SS}	DV_{DDR}	V_{SS}	N
M	MXO	$PLLV_{DD18}$	APLLREFV	EM_A[9]/ GPIO22	V_{SS}	DV_{DD18}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	M
L	MXI/CLKIN	MXV_{SS}	RSV6	$\overline{\text{RESET}}$	MXV_{DD}	V_{SS}	DV_{DD18}	CV_{DD}	CV_{DD}	CV_{DD}	L
K	CLK_OUT0/ GPIO48	EM_A[3]/ GPIO28	EM_A[5]/ GPIO26	EM_A[4]/ GPIO27	V_{SS}	DV_{DD18}	V_{SS}	CV_{DDDSP}	CV_{DDDSP}	CV_{DD}	K
	1	2	3	4	5	6	7	8	9	10	

Figure 2-2. Pin Map [Quadrant A]

	11	12	13	14	15	16	17	18	19	
W	DDR_A[6]	DDR_A[5]	DDR_A[0]	DDR_D[16]	DDR_D[18]	DDR_D[21]	DDR_D[27]	DDR_D[29]	RSV4	W
V	DDR_A[7]	DDR_A[4]	DDR_A[2]	DDR_D[17]	DDR_D[19]	DDR_D[22]	DDR_D[24]	DDR_D[28]	DDR_D[30]	V
U	DDR_A[9]	DDR_A[3]	DDR_A[1]	DDR_DQS[2]	DDR_D[20]	DDR_DQS[3]	DDR_D[25]	DDR_D[26]	DDR_D[31]	U
T	DDR_ VSSDLL	DDR_ZN	DDR_ZP	DDR_DQM[2]	DDR_REF	DDR_DQM[3]	DDR_D[23]	V_{SSA_1P1V}	DAC_IOUT_D	T
R	DV_{DDR2}	V_{SS}	DV_{DDR2}	V_{SS}	DV_{DDR2}	DAC_RBIAS	DAC_V_{REF}	V_{DDA_1P8V}	DAC_IOUT_C	R
P	V_{SS}	DV_{DDR2}	V_{SS}	DV_{DDR2}	V_{SS}	V_{DDA_1P1V}	V_{SSA_1P8V}	DAC_IOUT_B	DAC_IOUT_A	P
N	DV_{DDR2}	V_{SS}	DV_{DDR2}	V_{SS}	CI3/CCD11	CI4/CCD12/ UART_RTS2	CI5/CCD13/ UART_CTS2	CI6/CCD14/ UART_TXD2	CI7/CCD15/ UART_RXD2	N
M	V_{SS}	CV_{DD}	V_{SS}	DV_{DD18}	CI0/CCD8	CI1/CCD9	CI2/CCD10	HD	PCLK	M
L	CV_{DD}	V_{SS}	DV_{DD18}	V_{SS}	YI4/CCD4	YI5/CCD5	YI6/CCD6	YI7/CCD7	VD	L
K	CV_{DDDSP}	CV_{DD}	V_{SS}	DV_{DD18}	V_{SS}	YI0/CCD0	YI1/CCD1	YI2/CCD2	YI3/CCD3	K
	11	12	13	14	15	16	17	18	19	

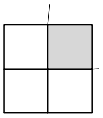

Figure 2-3. Pin Map [Quadrant B]

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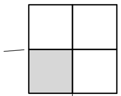
	11	12	13	14	15	16	17	18	19	
J	CV_{DDDSP}	V_{SS}	CV_{DDDSP}	V_{SS}	DV_{DD18}	USB_ID	USB_VBUS	USB_ V_{SSA3P3}	USB_ V_{DDA3P3}	J
H	CV_{DDDSP}	CV_{DDDSP}	V_{SS}	DV_{DD18}	V_{SS}	USB_V_{SS1P8}	USB_V_{DD1P8}	USB_R1	USB_DM	H
G	V_{SS}	V_{SS}	V_{SS}	V_{SS}	DV_{DD18}	USB_ V_{SSREF}	USB_ $V_{SSA1P2LD0}$	USB_ $V_{DDA1P2LD0}$	USB_DP	G
F	DV_{DD33}	DV_{DD33}	DV_{DD33}	DV_{DD18}	CV_{DD}	M24V_{DD}	M24V_{SS}	M24XI	M24XO	F
E	GPIOV33_10/ RXD3	GPIOV33_7/ RXD0	GPIO1/ $\overline{\text{C\_WE}}$	GPIO5/G1	YOUT4/R4/ **AEAW4**	YOUT5/R5	YOUT6/R6	YOUT7/R7	CLK_OUT1/ TIM_IN/ GPIO49	E
D	GPIOV33_12/ RXDV	GPIOV33_4/ TXD1	GPIO2/G0	GPIO38/R1	YOUT0/G5/ **AEAW0**	YOUT1/G6/ **AEAW1**	YOUT2/G7/ **AEAW2**	YOUT3/G8/ **AEAW3**	VCLK	D
C	GPIOV33_8/ RXD1	GPIOV33_6/ TXD3	GPIO0/ LCD_OE	GPIO3/B0/ LCD_FIELD	PWM0/ GPIO45	COUT7/G4	HSYNC	VSYNC	VPBECLK	C
B	GPIOV33_9/ RXD2	GPIOV33_3/ TXD0	GPIOV33_0/ TXEN	GPIO4/R0/ C_FIELD	PWM1/R2/ GPIO46	COUT1/B4/ **BTSEL1**	COUT3/B6/ **DSP_BT**	COUT5/G2	COUT6/G3	B
A	GPIOV33_5/ TXD2	GPIOV33_2/ COL	GPIOV33_1/ TXCLK	GPIO6/B1	PWM2/ B2/GPIO47	COUT0/B3/ **BTSEL0**	COUT2/B5/ **EM_WIDTH**	COUT4/B7	RSV2	A
	11	12	13	14	15	16	17	18	19	

BOLD text denotes a DaVinci device pin function

Figure 2-4. Pin Map [Quadrant C]



	1	2	3	4	5	6	7	8	9	10	
J	EM_A[2]/ (CLE)	EM_A[1]/ (ALE)	EM_BA[0]/ DA0	EM_A[0]/ DA2/ GPIO53	ATA_CS0/ GPIO50	V_{SS}	DV_{DD18}	V_{SS}	CV_{DDDSP}	CV_{DDDSP}	J
H	ATA_CS1/ GPIO51	EM_BA[1]/ DA1/ GPIO52	DMACK/ UART_TXD1	$\overline{\text{EM\_OE}}$/($\overline{\text{RE}}$)/ ($\overline{\text{IORD}}$)/$\overline{\text{DIOR}}$	EM_D14/ DD14	DV_{DD18}	V_{SS}	CV_{DDDSP}	V_{SS}	CV_{DDDSP}	H
G	DMARQ/ UART_RXD1	$\overline{\text{EM\_WE}}$/($\overline{\text{WE}}$)/ ($\overline{\text{IOWR}}$)/$\overline{\text{DIOW}}$	EM_R/$\overline{\text{W}}$/ INTRQ	EM_D11/ DD11	EM_D10/ DD10	V_{SS}	DV_{DD18}	V_{SS}	DV_{DD18}	V_{SS}	G
F	EM_WAIT/ (RDY/$\overline{\text{BSY}}$)/ $\overline{\text{IORDY}}$	EM_D13/ DD13	EM_D8/ DD8	EM_D6/ DD6	EM_D2/ DD2	DV_{DD18}	V_{SS}	DV_{DD18}	V_{SS}	DV_{DD33}	F
E	EM_D15/ DD15	EM_D9/ DD9	EM_D3/ DD3	EM_D4/ DD4	EM_D0/ DD0	TMS	DV_{DD18}	V_{SS}	SD_DATA1	GPIOV33_15/ MDIO	E
D	EM_D12/ DD12	EM_D5/ DD5	EM_D1/ DD1	RSV5	UART_RXD0/ GPIO35	EMU0	$\overline{\text{TRST}}$	SD_DATA0	SD_DATA2	GPIOV33_13/ RXER	D
C	EM_D7/ DD7	$\overline{\text{EM\_CS2}}$	GPIO7	SCL/ GPIO43	UART_TXD0/ GPIO36	EMU1	FSR/ GPIO32	FSX/ GPIO31	SD_DATA3	GPIOV33_14/ CRS	C
B	$\overline{\text{EM\_CS3}}$	SPI_EN1/ HDDIR/ GPIO42	SPI_DI/ GPIO40	SDA/GPIO44	TDO	RTCK	DX/ GPIO33	CLKX/ GPIO29	SD_CMD	GPIOV33_16/ MDCLK	B
A	RSV1	SPI_DO/ GPIO41	SPI_CLK/ GPIO39	SPI_EN0/ GPIO37	TDI	TCK	DR/ GPIO34	CLKR/ GPIO30	SD_CLK	GPIOV33_11/ RXCLK	A
	1	2	3	4	5	6	7	8	9	10	

Figure 2-5. Pin Map [Quadrant D]

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2.6.2 Signal Groups Description

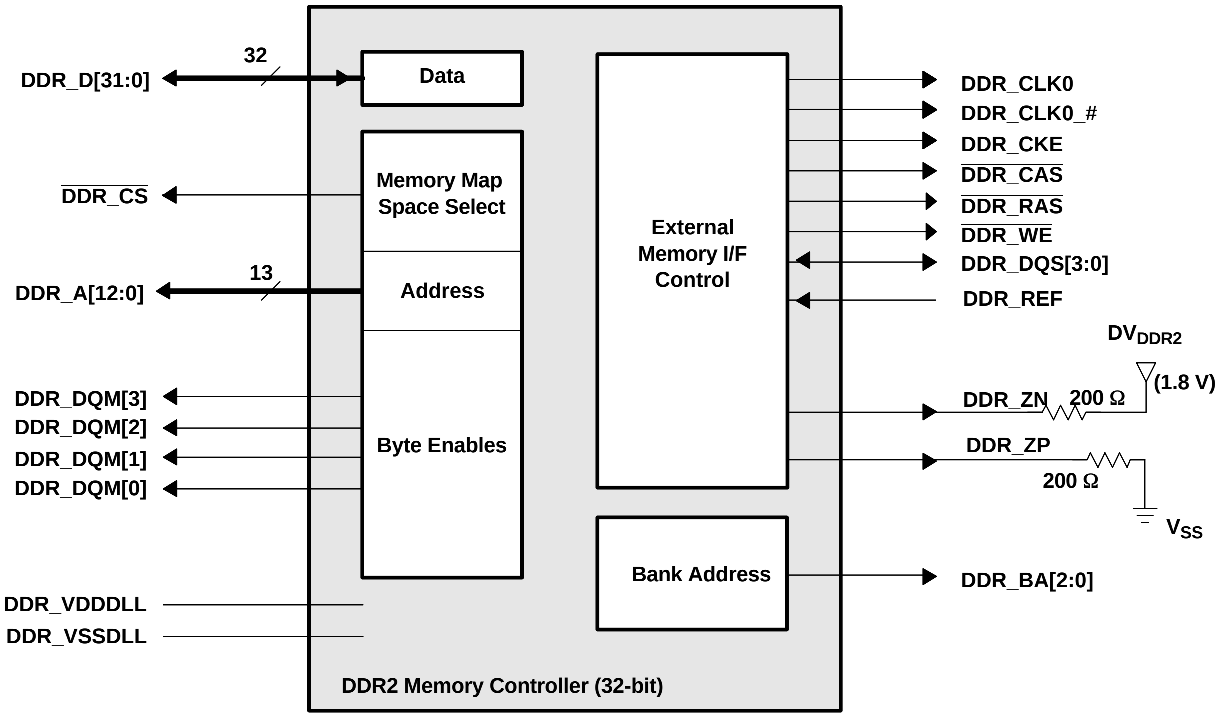

Figure 2-6. DDR2 Memory Controller Signals

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2.7 Terminal Functions

The terminal functions tables (Table 2-9 through Table 2-33) identify the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed/shared pin, and debugging considerations, see the Device Configurations section of this data sheet.

Table 2-9. BOOT Terminal Functions

<table>
<tr><th colspan="2">SIGNAL</th><th rowspan="2">TYPE(1)</th><th rowspan="2">IPD/
IPU(2)</th><th rowspan="2" colspan="3">DESCRIPTION</th></tr>
<tr><th>NAME</th><th>NO.</th></tr>
<tr><td colspan="7">BOOT</td></tr>
<tr><td>COUT0/
B3/
BTSEL0</td><td>A16</td><td>I/O/Z</td><td>IPD</td><td colspan="3">These pins are multiplexed between ARM boot mode and the VPBE. At reset, the boot mode inputs BTSEL0 and BTSEL1 are sampled to determine the ARM boot configuration. See below for the boot modes set by these inputs. See the Bootmode section for more details.
After reset, these are video encoder outputs COUT0 and COUT1, or RGB666/888 Blue output data bits 3 and 4 B3/B4.</td></tr>
<tr><td rowspan="5">COUT1/
B4/
BTSEL1</td><td rowspan="5">B16</td><td rowspan="5">I/O/Z</td><td rowspan="5">IPD</td><td>BTSEL1</td><td>BTSEL0</td><td>ARM Boot Mode</td></tr>
<tr><td>0</td><td>0</td><td>ARM ROM Boot (NAND) [default]</td></tr>
<tr><td>0</td><td>1</td><td>ARM EMIFA Boot (NOR)</td></tr>
<tr><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>ARM ROM Boot (UART)</td></tr>
<tr><td>COUT2/
B5/
EM_WIDTH</td><td>A17</td><td>I/O/Z</td><td>IPD</td><td colspan="3">This pin is multiplexed between EMIFA and the VPBE. At reset, the input state is sampled to set the EMIFA data bus width (EM_WIDTH). For an 8-bit wide EMIFA data bus, EM_WIDTH = 0. For a 16-bit wide EMIFA data bus, EM_WIDTH = 1.
After reset, it is video encoder output COUT2 or RGB666/888 Blue output data bit 5 B5.</td></tr>
<tr><td>COUT3/
B6/
DSP_BT</td><td>B17</td><td>I/O/Z</td><td>IPD</td><td colspan="3">This pin is multiplexed between DSP boot and the VPBE. At reset, the input state is sampled to set the DSP boot source DSP_BT. The DSP is booted by the ARM when DSP_BT=0. The DSP boots from EMIFA when DSP_BT=1.
After reset, it is video encoder output COUT3 or RGB666/888 Blue data bit 6 output B6.</td></tr>
<tr><td>YOUT0/
G5/
AEAW0</td><td>D15</td><td>I/O/Z</td><td>IPD</td><td rowspan="5" colspan="3">These pins are multiplexed between EMIFA and the VPBE. At reset, the input states of AEAW[4:0] are sampled to set the EMIFA address bus width. See the Peripheral Selection at Device Reset section for details.
After reset, these are video encoder outputs YOUT[0:4] or RGB666/888 Red and Green data bit outputs G5, G6, G7, R3, and R4.</td></tr>
<tr><td>YOUT1/
G6/
AEAW1</td><td>D16</td><td>I/O/Z</td><td>IPD</td></tr>
<tr><td>YOUT2/
G7/
AEAW2</td><td>D17</td><td>I/O/Z</td><td>IPD</td></tr>
<tr><td>YOUT3/
R3/
AEAW3</td><td>D18</td><td>I/O/Z</td><td>IPD</td></tr>
<tr><td>YOUT4/
R4/
AEAW4</td><td>E15</td><td>I/O/Z</td><td>IPD</td></tr>
</table>

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-10. Oscillator/PLL Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
OSCILLATOR, PLL				
MXI/ CLKIN	L1	I		Crystal input MXI for MX oscillator (system oscillator, typically 27 MHz). If the internal oscillator is bypassed, this is the external oscillator clock input.
MXO	M1	O		Crystal output for MX oscillator
MXV_{DD}	L5	S		1.8V power supply for MX oscillator
MXV_{SS}	L2	GND		Ground for MX oscillator
M24XI	F18	I		Crystal input for M24 oscillator (24 MHz for USB)
M24XO	F19	O		Crystal output for M24 oscillator
$M24V_{DD}$	F16	S		1.8V power supply for M24 oscillator
$M24V_{SS}$	F17	GND		Ground for M24 oscillator
$PLLV_{DD18}$	M2	S		1.8 Volt power supply for PLLs (system and USB)
APLLREFV	M3	S		Core voltage reference for PLL logic and bandgap backup

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-11. Clock Generator Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
CLOCK GENERATOR				
CLK_OUT0/ GPIO48	K1	I/O/Z	IPD	This pin is multiplexed between the PLL1 clock generator and GPIO. For the PLL1 clock generator, it is clock output CLK_OUT0. This is configurable for 13.5 MHz or 27 MHz clock outputs. For GPIO, it is GPIO48 [default].
CLK_OUT1/ TIM_IN/ GPIO49	E19	I/O/Z	IPD	This pin is multiplexed between the USB clock generator, timer, and GPIO. For the USB clock generator, it is clock output CLK_OUT1. This is configurable for 12 MHz or 24 MHz clock outputs. For Timer0, it is the timer event capture input TIM_IN. For GPIO, it is GPIO49 [default].

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-12. RESET and JTAG Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
RESET				
$\overline{RESET}$	L4	I	IPU	This is the active low Global reset input.
JTAG				
TMS	E6	I	IPU	JTAG test-port mode select input
TDO	B5	O/Z		JTAG test-port data output
TDI	A5	I	IPU	JTAG test-port data input
TCK	A6	I	IPU	JTAG test-port clock input
RTCK	B6	O/Z		JTAG test-port return clock output
$\overline{TRST}$	D7	I	IPD	JTAG test-port reset. For IEEE 1149.1 JTAG compatibility, see the IEEE 1149.1 JTAG compatibility statement portion of this data sheet.
EMU1	C6	I/O/Z	IPU	Emulation pin 1
EMU0	D6	I/O/Z	IPU	Emulation pin 0

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-13. EMIFA Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
EMIFA BOOT CONFIGURATION				
COUT2/ B5/ **EM_WIDTH**	A17	I/O/Z	IPD	This pin is multiplexed between EMIFA and the VPBE. At reset, the input state is sampled to set the EMIFA data bus width (EM_WIDTH). For an 8-bit wide EMIFA data bus, EM_WIDTH = 0. For a 16-bit wide EMIFA data bus, EM_WIDTH = 1. After reset, it is video encoder output COUT2 or RGB666/888 Blue output data bit 5 B5.
COUT3/ B6/ **DSP_BT**	B17	I/O/Z	IPD	This pin is multiplexed between DSP boot and the VPBE. At reset, the input state is sampled to set the DSP boot source DSP_BT. The DSP is booted by the ARM when DSP_BT=0. The DSP boots from EMIFA when DSP_BT=1. After reset, it is video encoder output COUT3 or RGB666/888 Blue data bit 6 output B6.
YOUT0/ G5/ **AEAW0**	D15	I/O/Z	IPD	These pins are multiplexed between EMIFA and the VPBE. At reset, the input states of AEAW[4:0] are sampled to set the EMIFA address bus width. See the Peripheral Selection at Device Reset section for details. After reset, these are video encoder outputs YOUT[0:4] or RGB666/888 Red and Green data bit outputs G5, G6, G7, R3, and R4.
YOUT1/ G6/ **AEAW1**	D16	I/O/Z	IPD	
YOUT2/ G7/ **AEAW2**	D17	I/O/Z	IPD	
YOUT3/ R3/ **AEAW3**	D18	I/O/Z	IPD	
YOUT4/ R4/ **AEAW4**	E15	I/O/Z	IPD	
EMIFA FUNCTIONAL PINS: ASYNC / NOR				
EM_CS2	C2	I/O/Z	IPD	For EMIFA, this pin is Chip Select 2 output EM_CS2 for use with asynchronous memories (i.e., NOR flash) or NAND flash. This is the chip select for the default boot and ROM boot modes.
EM_CS3	B1	I/O/Z	IPD	For EMIFA, this pin is Chip Select 3 output EM_CS3 for use with asynchronous memories (i.e., NOR flash) or NAND flash.
EM_CS4/ GPIO9/ VLYNQ_SCRUN	T2	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is Chip Select 4 output EM_CS4 for use with asynchronous memories (i.e., NOR flash) or NAND flash. For GPIO, it is GPIO9. For VLYNQ, it is the Serial Clock run request VLYNQ_SCRUN.
EM_CS5/ GPIO8/ VLYNQ_CLOCK	T1	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is Chip Select 5 output EM_CS5 for use with asynchronous memories (i.e., NOR flash) or NAND flash. For GPIO, it is GPIO pin 8 GPIO8 For VLYNQ, it is the clock VLYNQ_CLOCK.
EM_R/W/ INTRQ	G3	I/O/Z	IPD	This pin is multiplexed between EMIFA and ATA/CF. For EMIFA, it is read/write output EM_R/W. For ATA/CF, it is interrupt request input INTRQ.
EM_WAIT/ (RDY/BSY)/ IORDY	F1	I/O/Z	IPD	This pin is multiplexed between EMIFA (NAND/SmartMedia/xD) and ATA/CF. For EMIFA, it is wait state extension input EM_WAIT. For NAND/SmartMedia/xD, it is ready/busy input (RDY/BSY). For ATA/CF, it is IO Ready input IORDY.
EM_OE/ (RE)/ (IORD)/ DIOR	H4	I/O/Z	IPD	This pin is multiplexed between EMIFA (NAND/SmartMedia/xD) and ATA/CF. For EMIFA, it is output enable output EM_OE. For NAND/SmartMedia/xD, it is read enable output (RE). For CF, it is read strobe output (IORD). For ATA, it is read strobe output DIOR.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

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Table 2-13. EMIFA Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
$\overline{\text{EM\_WE}}$ ($\overline{\text{WE}}$) ($\overline{\text{IOWR}}$)/ $\overline{\text{DIOW}}$	G2	I/O/Z	IPD	This pin is multiplexed between EMIFA (NAND/SmartMedia/xD) and ATA/CF. For NAND/SmartMedia/xD or EMIFA, it is write enable output $\overline{\text{EM\_WE}}$. For NAND/SmartMedia/xD, it is write enable output ($\overline{\text{WE}}$). For CF, it is write strobe output ($\overline{\text{IOWR}}$). For ATA, it is write strobe output $\overline{\text{DIOW}}$.
EM_BA[0]/ DA0	J3	I/O/Z	IPD	This pin is multiplexed between EMIFA and ATA/CF. For EMIFA, this is the Bank Address 0 output (EM_BA[0]). When connected to an 8-bit asynchronous memory, this pin is the lowest order bit of the byte address. When connected to a 16-bit asynchronous memory, this pin has the same function as EMIF address pin 22 (EM_A[22]). For ATA/CF, it is Device address bit 0 output DA0.
EM_BA[1]/ DA1/ GPIO52	H2	I/O/Z	IPD	This pin is multiplexed between EMIFA, ATA/CF, and GPIO. For EMIFA, this is the Bank Address 1 output EM_BA[1]. When connected to a 16 bit asynchronous memory this pin is the lowest order bit of the 16-bit word address. When connected to an 8-bit asynchronous memory, this pin is the 2nd bit of the address. For ATA/CF, it is Device address bit 1 output DA1. In GPIO mode, it is GPIO52.
EM_A[21]/ GPIO10/ VLYNQ_TXD0	T3	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is address bit 21 output EM_A[21]. For GPIO, it is GPIO10. For VLYNQ, it is bit 0 of the transmit bus VLYNQ_TXD0.
EM_A[20]/ GPIO11/ VLYNQ_RXD0	R3	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is address bit 20 output EM_A[20]. For GPIO, it is GPIO11. For VLYNQ, it is receive bus bit 0 input VLYNQ_RXD0.
EM_A[19]/ GPIO12/ VLYNQ_TXD1	R4	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is address bit 19 output EM_A[19]. For GPIO, it is GPIO12. For VLYNQ, it is transmit bus bit 1 output VLYNQ_TXD1.
EM_A[18]/ GPIO13/ VLYNQ_RXD1	P5	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is address bit 18 output EM_A[18]. For GPIO, it is GPIO13. For VLYNQ, it is receive bus bit 1 input VLYNQ_RXD1.
EM_A[17]/ GPIO14/ VLYNQ_TXD2	R2	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is address bit 17 output EM_A[17]. For GPIO, it is GPIO14. For VLYNQ, it is transmit bus bit 2 output VLYNQ_TXD2.
EM_A[16]/ GPIO15/ VLYNQ_RXD2	R5	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is address bit 16 output EM_A[16]. For GPIO, it is GPIO15. For VLYNQ, it is receive bus bit 2 input VLYNQ_RXD2.
EM_A[15]/ GPIO16/ VLYNQ_TXD3	P3	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is address bit 15 output EM_A[15]. For GPIO, it is GPIO16. For VLYNQ, it is transmit bus bit 3 output VLYNQ_TXD3.
EM_A[14]/ GPIO17/ VLYNQ_RXD3	P4	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is address bit 14 output EM_A[14]. For GPIO, it is GPIO17. For VLYNQ, it is receive bus bit 3 input VLYNQ_RXD3.
EM_A[13]/ GPIO18	N4	I/O/Z	IPD	This pin is multiplexed between EMIFA and GPIO. For EMIFA, it is address bit 13 output EM_A[13]. For GPIO, it is GPIO18.
EM_A[12]/ GPIO19	R1	I/O/Z	IPD	This pin is multiplexed between EMIFA and GPIO. For EMIFA, it is address bit 12 output EM_A[12]. For GPIO, it is GPIO19.
EM_A[11]/ GPIO20	P2	I/O/Z	IPD	This pin is multiplexed between EMIFA and GPIO. For EMIFA, it is address bit 11 output EM_A[11]. For GPIO, it is GPIO20.
EM_A[10]/ GPIO21	P1	I/O/Z	IPD	This pin is multiplexed between EMIFA and GPIO. For EMIFA, it is address bit 10 output EM_A[10]. For GPIO, it is GPIO21.

Table 2-13. EMIFA Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE (1)	IPD/ IPU (2)	DESCRIPTION
EM_A[9]/ GPIO22	M4	I/O/Z	IPD	This pin is multiplexed between EMIFA and GPIO. For EMIFA, it is address bit 9 output EM_A[9]. For GPIO, it is GPIO22.
EM_A[8]/ GPIO23	N3	I/O/Z	IPD	This pin is multiplexed between EMIFA and GPIO. For EMIFA, it is address bit 8 output EM_A[8]. For GPIO, it is GPIO23.
EM_A[7]/ GPIO24	N2	I/O/Z	IPD	This pin is multiplexed between EMIFA and GPIO. For EMIFA, it is address bit 7 output EM_A[7]. For GPIO, it is GPIO24.
EM_A[6]/ GPIO25	N1	I/O/Z	IPD	This pin is multiplexed between EMIFA and GPIO. For EMIFA, it is address bit 6 output EM_A[6]. For GPIO, it is GPIO25.
EM_A[5]/ GPIO26	K3	I/O/Z	IPD	This pin is multiplexed between EMIFA and GPIO. For EMIFA, it is address bit 5 output EM_A[5]. For GPIO, it is GPIO26.
EM_A[4]/ GPIO27	K4	I/O/Z	IPD	This pin is multiplexed between EMIFA and GPIO. For EMIFA, it is address bit 4 output EM_A[4]. For GPIO, it is GPIO27.
EM_A[3]/ GPIO28	K2	I/O/Z	IPD	This pin is multiplexed between EMIFA and GPIO. For EMIFA, it is address bit 3 output EM_A[3]. For GPIO, it is GPIO28.
EM_A[2]/ (CLE)	J1	I/O/Z	IPD	For EMIFA, this pin is the EM_A[2] address line. For NAND/SmartMedia/xD, this pin is the Command Latch Enable output (CLE).
EM_A[1]/ (ALE)	J2	I/O/Z	IPD	When used for EMIFA, it is address output EM_A[1]. For NAND/SmartMedia/xD, it is Address Latch Enable output (ALE).
EM_A[0]/ DA2/ GPIO53	J4	I/O/Z	IPD	This pin is multiplexed between EMIFA, ATA/CF, and GPIO. For EMIFA, this is Address output EM_A[0], which is the least significant bit on a 32-bit word address. When connected to a 16-bit asynchronous memory, this pin is the 2nd bit of the address. For an 8-bit asynchronous memory, this pin is the 3rd bit of the address. For ATA/CF, it is Device address bit 2 output DA2. In GPIO mode, it is GPIO53.

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Table 2-13. EMIFA Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE (1)	IPD/ IPU (2)	DESCRIPTION
EM_D0/ DD0	E5	I/O/Z	IPD	These pins are multiplexed between EMIFA (NAND) and ATA/CF. In all cases they are used as a 16 bit bi-directional data bus. For EMIFA (NAND), these are EM_D[15:0]. For ATA/CF, these are DD[15:0].
EM_D1/ DD1	D3	I/O/Z	IPD	
EM_D2/ DD2	F5	I/O/Z	IPD	
EM_D3/ DD3	E3	I/O/Z	IPD	
EM_D4/ DD4	E4	I/O/Z	IPD	
EM_D5/ DD5	D2	I/O/Z	IPD	
EM_D6/ DD6	F4	I/O/Z	IPD	
EM_D7/ DD7	C1	I/O/Z	IPD	
EM_D8/ DD8	F3	I/O/Z	IPD	
EM_D9/ DD9	E2	I/O/Z	IPD	
EM_D10/ DD10	G5	I/O/Z	IPD	
EM_D11/ DD11	G4	I/O/Z	IPD	
EM_D12/ DD12	D1	I/O/Z	IPD	
EM_D13/ DD13	F2	I/O/Z	IPD	
EM_D14/ DD14	H5	I/O/Z	IPD	
EM_D15/ DD15	E1	I/O/Z	IPD	
EMIFA FUNCTIONAL PINS: NAND / SMARTMEDIA / xD				
EM_A[1]/ (ALE)	J2	I/O/Z	IPD	When used for EMIFA, it is address output EM_A[1]. For NAND/SmartMedia/xD, it is Address Latch Enable output (ALE).
EM_A[2]/ (CLE)	J1	I/O/Z	IPD	For EMIFA, this pin is the EM_A[2] address line. For NAND/SmartMedia/xD, this pin is the Command Latch Enable output (CLE).
EM_WAIT/ (RDY/BSY)/ IORDY	F1	I/O/Z	IPD	This pin is multiplexed between EMIFA (NAND/SmartMedia/xD) and ATA/CF. For EMIFA, it is wait state extension input EM_WAIT. For NAND/SmartMedia/xD, it is ready/busy input (RDY/BSY). For ATA/CF, it is IO Ready input IORDY.
EM_OE/ (RE)/ (IORD)/ DIOR	H4	I/O/Z	IPD	This pin is multiplexed between EMIFA (NAND/SmartMedia/xD) and ATA/CF. For EMIFA, it is output enable output EM_OE. For NAND/SmartMedia/xD, it is read enable output (RE). For CF, it is read strobe output (IORD). For ATA, it is read strobe output DIOR.
EM_WE (WE) (IOWR)/ DIOW	G2	I/O/Z	IPD	This pin is multiplexed between EMIFA (NAND/SmartMedia/xD) and ATA/CF. For EMIFA, it is write enable output EM_WE. For NAND/SmartMedia/xD, it is write enable output (WE). For CF, it is write strobe output (IOWR). For ATA, it is write strobe output DIOW.
EM_CS2	C2	I/O/Z	IPD	For EMIFA, this pin is Chip Select 2 output EM_CS2 for use with asynchronous memories (i.e. NOR flash) or NAND flash. This is the chip select for the default boot and ROM boot modes.
EM_CS3	B1	I/O/Z	IPD	For EMIFA, this pin is Chip Select 3 output EM_CS3 for use with asynchronous memories (i.e. NOR flash) or NAND flash.

Table 2-13. EMIFA Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE[1]	IPD/ IPU[2]	DESCRIPTION
EM_CS4/ GPIO9/ VLYNQ_SCRUN	T2	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is Chip Select 4 output EM_CS4 for use with asynchronous memories (i.e., NOR flash) or NAND flash. For GPIO, it is GPIO9. For VLYNQ, it is the Serial Clock run request VLYNQ_SCRUN.
EM_CS5/ GPIO8/ VLYNQ_CLOCK	T1	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is Chip Select 5 output EM_CS5 for use with asynchronous memories (i.e., NOR flash) or NAND flash. For GPIO, it is GPIO pin 8 GPIO8 For VLYNQ, it is the clock VLYNQ_CLOCK.
EM_D0/ DD0	E5	I/O/Z	IPD	These pins are multiplexed between EMIFA (NAND) and ATA/CF. In all cases they are used as a 16 bit bi-directional data bus. For EMIFA (NAND), these are EM_D[15:0]. For ATA/CF, these are DD[15:0].
EM_D1/ DD1	D3	I/O/Z	IPD	
EM_D2/ DD2	F5	I/O/Z	IPD	
EM_D3/ DD3	E3	I/O/Z	IPD	
EM_D4/ DD4	E4	I/O/Z	IPD	
EM_D5/ DD5	D2	I/O/Z	IPD	
EM_D6/ DD6	F4	I/O/Z	IPD	
EM_D7/ DD7	C1	I/O/Z	IPD	
EM_D8/ DD8	F3	I/O/Z	IPD	
EM_D9/ DD9	E2	I/O/Z	IPD	
EM_D10/ DD10	G5	I/O/Z	IPD	
EM_D11/ DD11	G4	I/O/Z	IPD	
EM_D12/ DD12	D1	I/O/Z	IPD	
EM_D13/ DD13	F2	I/O/Z	IPD	
EM_D14/ DD14	H5	I/O/Z	IPD	
EM_D15/ DD15	E1	I/O/Z	IPD	

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Table 2-14. DDR2 Memory Controller Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
DDR2 Memory Controller				
DDR_CLK0	W7	I/O/Z		DDR2 Clock
DDR_CLK0_#	W8	I/O/Z		DDR2 Differential clock
DDR_CKE	V8	I/O/Z		DDR2 Clock Enable
$\overline{\text{DDR\_CS}}$	T9	I/O/Z		DDR2 Active low chip select
$\overline{\text{DDR\_WE}}$	T8	I/O/Z		DDR2 Active low Write enable
DDR_DQM[3]	T16	I/O/Z		DDR2 Data mask outputs DQM3: For upper byte data bus DDR_D[31:24] DQM2: For DDR_D[23:16] DQM1: For DDR_D[15:8] DQM0: For lower byte DDR_D[7:0]
DDR_DQM[2]	T14	I/O/Z		
DDR_DQM[1]	T6	I/O/Z		
DDR_DQM[0]	T4	I/O/Z		
$\overline{\text{DDR\_RAS}}$	U7	I/O/Z		DDR2 Row Access Signal output
$\overline{\text{DDR\_CAS}}$	T7	I/O/Z		DDR2 Column Access Signal output
DDR_DQS[0]	U4	I/O/Z		Data strobe input/outputs for each byte of the 32-bit data bus. They are outputs to the DDR2 memory when writing and inputs when reading. They are used to synchronize the data transfers. DQS3 : For upper byte DDR_D[31:24] DQS2: For DDR_D[23:16] DQS1: For DDR_D[15:8] DQS0: For bottom byte DDR_D[7:0]
DDR_DQS[1]	U6	I/O/Z		
DDR_DQS[2]	U14	I/O/Z		
DDR_DQS[3]	U16	I/O/Z		
DDR_BS[0]	U8	I/O/Z		Bank select outputs (BS[2:0]). Two are required to support 1Gb DDR2 memories.
DDR_BS[1]	V9			
DDR_BS[2]	U9			
DDR_A[12]	W9	I/O/Z		DDR2 address bus
DDR_A[11]	W10			
DDR_A[10]	U10			
DDR_A[9]	U11			
DDR_A[8]	V10			
DDR_A[7]	V11			
DDR_A[6]	W11			
DDR_A[5]	W12			
DDR_A[4]	V12			
DDR_A[3]	U12			
DDR_A[2]	V13			
DDR_A[1]	U13			
DDR_A[0]	W13			

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-14. DDR2 Memory Controller Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE [1]	IPD/ IPU [2]	DESCRIPTION
DDR_D[31]	U19	I/O/Z		DDR2 data bus can be configured as 32 bits wide or 16 bits wide.
DDR_D[30]	V19			
DDR_D[29]	W18			
DDR_D[28]	V18			
DDR_D[27]	W17			
DDR_D[26]	U18			
DDR_D[25]	U17			
DDR_D[24]	V17			
DDR_D[23]	T17			
DDR_D[22]	V16			
DDR_D[21]	W16			
DDR_D[20]	U15			
DDR_D[19]	V15			
DDR_D[18]	W15			
DDR_D[17]	V14			
DDR_D[16]	W14			
DDR_D[15]	V7			
DDR_D[14]	W6			
DDR_D[13]	V6			
DDR_D[12]	W5			
DDR_D[11]	V5			
DDR_D[10]	U5			
DDR_D[9]	W4			
DDR_D[8]	V4			
DDR_D[7]	W3			
DDR_D[6]	V3			
DDR_D[5]	U3			
DDR_D[4]	W2			
DDR_D[3]	V2			
DDR_D[2]	V1			
DDR_D[1]	U2			
DDR_D[0]	U1			
DDR_VREF	T15	I		Reference voltage input for the SSTL_18 IO buffers.
DDR_VSSDLL	T11	GND		Ground for the DDR2 DLL
DDR_VDDDLL	T10	S		Power (1.8 Volts) for the DDR2 DLL
DDR_ZN	T12	O/Z		Impedance control for DDR2 outputs. This must be connected via a 200 Ω resistor to DV_{DDR2}.
DDR_ZP	T13	O/Z		Impedance control for DDR2 outputs. This must be connected via a 200 Ω resistor to V_{SS}.

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Table 2-15. I2C Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
I2C				
SCL/ GPIO43	C4	I/O/Z	IPD	This pin is multiplexed between I2C and GPIO. For I2C, it is clock output SCL. For GPIO, it is GPIO43.
SDA/ GPIO44	B4	I/O/Z	IPD	This pin is multiplexed between I2C and GPIO. For I2C, it is bi-directional data signal SDA. For GPIO, it is GPIO44.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-16. Audio Serial Port (ASP) Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
Audio Serial Port (ASP)				
CLKX/ GPIO29	B8	I/O/Z	IPD	This pin is multiplexed between ASP and GPIO. For ASP, it is Transmit clock IO CLKX. For GPIO, it is GPIO29.
CLKR/ GPIO30	A8	I/O/Z	IPD	This pin is multiplexed between ASP and GPIO. For ASP, it is Receive clock IO CLKR. For GPIO, it is GPIO30
FSX/ GPIO31	C8	I/O/Z	IPD	This pin is multiplexed between ASP and GPIO. For ASP, it is Transmit frame synchronization IO FSX. For GPIO, it is GPIO31.
FSR/ GPIO32	C7	I/O/Z	IPD	This pin is multiplexed between ASP and GPIO. For ASP, it is Receive frame synchronization IO FSR. For GPIO, it is GPIO32.
DX/ GPIO33	B7	I/O/Z	IPD	This pin is multiplexed between ASP and GPIO. For ASP, it is Data Transmit output DX. For GPIO, it is GPIO33.
DR/ GPIO34	A7	I/O/Z	IPD	This pin is multiplexed between ASP and GPIO. For ASP, it is Data Receive input DR. For GPIO, it is GPIO34.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-17. SPI Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
Serial Port Interface (SPI)				
SPI_EN0/ GPIO37	A4	I/O/Z	IPD	This pin is multiplexed between SPI and GPIO. When used by SPI, it is SPI slave device 0 enable output SPI_EN0. For GPIO, it is GPIO37.
SPI_EN1/ HDDIR/ GPIO42	B2	I/O/Z	IPD	This pin is multiplexed between SPI, ATA, and GPIO. When used by SPI, it is SPI slave device 1 enable output SPI_EN1. For ATA, it is buffer direction control output HDDIR. For GPIO, it is GPIO42.
SPI_CLK/ GPIO39	A3	I/O/Z	IPD	This pin is multiplexed between SPI and GPIO. For SPI, it is clock output SPI_CLK. For GPIO, it is GPIO39.
SPI_DI/ GPIO40	B3	I/O/Z	IPD	This pin is multiplexed between SPI and GPIO. For SPI, it is data input SPI_DI. For GPIO, it is GPIO40.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-17. SPI Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
SPI_DO/ GPIO41	A2	I/O/Z	IPD	This pin is multiplexed between SPI and GPIO. For SPI it is data output SPI_DO. For GPIO, it is GPIO41.

Table 2-18. EMAC and MDIO Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
EMAC				
GPIOV33_0/ TXEN	B13	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, this pin is 3.3V GPIO pin GPIOV33_0. In Ethernet MAC mode, it is Transmit Enable output TXEN.
GPIOV33_1/ TXCLK	A13	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_1. In Ethernet MAC mode, it is Transmit Clock output TXCLK.
GPIOV33_2/ COL	A12	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_2. In Ethernet MAC mode, it is Collision Detect input COL.
GPIOV33_6/ TXD3	C12	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_6. In Ethernet MAC mode, it is Transmit Data 3 output TXD3.
GPIOV33_5/ TXD2	A11	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_5. In Ethernet MAC mode, it is Transmit Data 2 output TXD2.
GPIOV33_4/ TXD1	D12	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_4. In Ethernet MAC mode, it is Transmit Data 1 output TXD1.
GPIOV33_3/ TXD0	B12	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_3. In Ethernet MAC mode, it is Transmit Data 0 output TXD0.
GPIOV33_11/ RXCLK	A10	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_11. In Ethernet MAC mode, it is Receive Clock input RXCLK.
GPIOV33_12/ RXDV	D11	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_12. In Ethernet MAC mode, it is Receive Data Valid input RXDV.
GPIOV33_13/ RXER	D10	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_13. In Ethernet MAC mode, it is Receive Error input RXER.
GPIOV33_14/ CRS	C10	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_14. In Ethernet MAC mode, it is Carrier Sense input CRS.
GPIOV33_10/ RXD3	E11	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_10. In Ethernet MAC mode, it is Receive Data 3 input RXD3.
GPIOV33_9/ RXD2	B11	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_9. In Ethernet MAC mode, it is Receive Data 2 input RXD2.
GPIOV33_8/ RXD1	C11	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_8. In Ethernet MAC mode, it is Receive data 1 input RXD1.
GPIOV33_7/ RXD0	E12	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_7. In Ethernet MAC mode, it is Receive Data 0 input RXD0.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

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Table 2-18. EMAC and MDIO Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
MDIO				
GPIOV33_16/ MDCLK	B10	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_16. In Ethernet MAC mode, it is Management Data Clock output MDCLK.
GPIOV33_15/ MDIO	E10	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_15. In Ethernet MAC mode, it is Management Data IO MDIO.

Table 2-19. GPIOV33 Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
GPIOV33				
GPIOV33_16/ MDCLK	B10	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_16. In Ethernet MAC mode, it is Management Data Clock output MDCLK.
GPIOV33_15/ MDIO	E10	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_15. In Ethernet MAC mode, it is Management Data IO MDIO.
GPIOV33_14/ CRS	C10	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_14. In Ethernet MAC mode, it is Carrier Sense input CRS.
GPIOV33_13/ RXER	D10	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_13. In Ethernet MAC mode, it is Receive Error input RXER.
GPIOV33_12/ RXDV	D11	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_12. In Ethernet MAC mode, it is Receive Data Valid input RXDV.
GPIOV33_11/ RXCLK	A10	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_11. In Ethernet MAC mode, it is Receive Clock input RXCLK.
GPIOV33_10/ RXD3	E11	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_10. In Ethernet MAC mode, it is Receive Data 3 input RXD3.
GPIOV33_9/ RXD2	B11	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_9. In Ethernet MAC mode, it is Receive Data 2 input RXD2.
GPIOV33_8/ RXD1	C11	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_8. In Ethernet MAC mode, it is Receive data 1 input RXD1.
GPIOV33_7/ RXD0	E12	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_7. In Ethernet MAC mode, it is Receive Data 0 input RXD0.
GPIOV33_6/ TXD3	C12	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_6. In Ethernet MAC mode, it is Transmit Data 3 output TXD3.
GPIOV33_5/ TXD2	A11	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_5. In Ethernet MAC mode, it is Transmit Data 2 output TXD2.
GPIOV33_4/ TXD1	D12	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_4. In Ethernet MAC mode, it is Transmit Data 1 output TXD1.
GPIOV33_3/ TXD0	B12	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_3. In Ethernet MAC mode, it is Transmit Data 0 output TXD0.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-19. GPIOV33 Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
GPIOV33_2/ COL	A12	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_2. In Ethernet MAC mode, it is Collision Detect input COL.
GPIOV33_1/ TXCLK	A13	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, it is 3.3V GPIO GPIOV33_1. In Ethernet MAC mode, it is Transmit Clock output TXCLK.
GPIOV33_0/ TXEN	B13	I/O/Z	IPD	This pin is multiplexed between GPIO and Ethernet MAC. In GPIO mode, this pin is 3.3V GPIO pin GPIOV33_0. In Ethernet MAC mode, it is Transmit Enable output TXEN.

Table 2-20. Standalone GPIOV18 Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
Standalone GPIOV18				
GPIO7	C3	I/O/Z	IPD	This pin is standalone and functions as GPIO7.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-21. USB Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
USB 2.0				
M24XI	F18	I		Crystal input for M24 oscillator (24 MHz for USB)
M24X0	F19	O		Crystal output for M24 oscillator
$M24V_{DD}$	F16	S		1.8V power supply for M24 oscillator
$M24V_{SS}$	F17	GND		Ground for M24 oscillator
$PLLV_{DD18}$	M2	S		1.8 Volt power supply for PLLs (system and USB)
USB_VBUS	J17	A I/O		5V input that signifies that VBUS is connected
USB_ID	J16	A I/O		USB operating mode identification pin. For Host mode operation, pull down this pin to ground (V_{SS}) via an external 1.5-kΩ resistor. For Device mode operation, pull up this pin to DV_{DD33} rail via an external 1.5-kΩ resistor.
USB_DP	G19	A I/O		USB bi-directional Data Differential signal pair [positive/negative].
USB_DM	H19	A I/O		
USB_R1	H18	A I/O		Reference current output. This must be connected via a 10 kΩ ± 1% resistor to USB_V_{SSREF}.
USB_V_{SSREF}	G16	GND		Ground for reference current.
USB_V_{DDA3P3}	J19	S		Analog 3.3 V power supply for USB phy
USB_V_{SSA3P3}	J18	GND		Analog ground for USB phy
USB_V_{DD1P8}	H17	S		1.8 V I/O power supply for USB phy
USB_V_{SS1P8}	H16	GND		I/O Ground for USB phy
$USB\_V_{DDA1P2LDO}$	G18	S		Core Power supply LDO output for USB phy. This must be connected via 1 µF capacitor to $USB\_V_{SSA1P2LDO}$. Do not connect this to other supply pins.
$USB\_V_{SSA1P2LDO}$	G17	GND		Core Ground for USB phy. This must be connected via 1 µF capacitor to $USB\_V_{DDA1P2LDO}$.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

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Table 2-22. VLYNQ Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
VLYNQ				
$\overline{\text{EM\_CS5}}$/ GPIO8/ VLYNQ_CLOCK	T1	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is Chip Select 5 output EM_CS5 for use with asynchronous memories (i.e., NOR flash) or NAND flash. For GPIO, it is GPIO pin 8 GPIO8 For VLYNQ, it is the clock (VLYNQ_CLOCK).
$\overline{\text{EM\_CS4}}$/ GPIO9/ VLYNQ_SCRUN	T2	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is Chip Select 4 output EM_CS4 for use with asynchronous memories (i.e., NOR flash) or NAND flash. For GPIO, it is GPIO9. For VLYNQ, it is the Serial Clock run request (VLYNQ_SCRUN).
EM_A[15]/ GPIO16/ VLYNQ_TXD3	P3	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is address bit 15 output EM_A[15]. For GPIO, it is GPIO16. For VLYNQ, it is transmit bus bit 3 output VLYNQ_TXD3.
EM_A[17]/ GPIO14/ VLYNQ_TXD2	R2	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is address bit 17 output EM_A[17]. For GPIO, it is GPIO14. For VLYNQ, it is transmit bus bit 2 output VLYNQ_TXD2.
EM_A[19]/ GPIO12/ VLYNQ_TXD1	R4	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is address bit 19 output EM_A[19]. For GPIO, it is GPIO12. For VLYNQ, it is transmit bus bit 1 output VLYNQ_TXD1.
EM_A[21]/ GPIO10/ VLYNQ_TXD0	T3	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is address bit 21 output EM_A[21]. For GPIO, it is GPIO10. For VLYNQ, it is bit 0 of the transmit bus (VLYNQ_TXD0).
EM_A[14]/ GPIO17/ VLYNQ_RXD3	P4	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is address bit 14 output EM_A[14]. For GPIO, it is GPIO17. For VLYNQ, it is receive bus bit 3 input VLYNQ_RXD3.
EM_A[16]/ GPIO15/ VLYNQ_RXD2	R5	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is address bit 16 output EM_A[16]. For GPIO, it is GPIO15. For VLYNQ, it is receive bus bit 2 input VLYNQ_RXD2.
EM_A[18]/ GPIO13/ VLYNQ_RXD1	P5	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is address bit 18 output EM_A[18]. For GPIO, it is GPIO13. For VLYNQ, it is receive bus bit 1 input VLYNQ_RXD1.
EM_A[20]/ GPIO11/ VLYNQ_RXD0	R3	I/O/Z	IPD	This pin is multiplexed between EMIFA, GPIO, and VLYNQ. For EMIFA, it is address bit 20 output EM_A[20]. For GPIO, it is GPIO11. For VLYNQ, it is receive bus bit 0 input VLYNQ_RXD0.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-23. VPFE Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
VIDEO/IMAGE IN (VPFE)				
PCLK	M19	I		Pixel clock input used to load image data into the CCD Controller (CCDC) on pins CI[7:0] and YI[7:0].
VD	L19	I/O/Z		Vertical synchronization signal that can be either an input (slave mode) or an output (master mode), which signals the start of a new frame to the CCDC.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-23. VPFE Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
HD	M18	I/O/Z		Horizontal synchronization signal that can be either an input (slave mode) or an output (master mode), which signals the start of a new line to the CCDC.
CI7/ CCD15/ UART_RXD2	N19	I/O/Z	IPD	This pin is multiplexed between the CCDC and UART2. When used by the CCDC as input CI7, it supports several modes. In 16-bit CCD Analog-Front-End (AFE) mode, it is input CCD15. In 16-bit YCbCr mode, it is time multiplexed between CB7 and CR7 inputs. In 8-bit YCbCr mode, it is time multiplexed between Y7, CB7, and CR7 of the upper 8-bit channel. When used by UART2 it is the receive data input UART_RXD2.
CI6/ CCD14/ UART_TXD2	N18	I/O/Z	IPD	This pin is multiplexed between the CCDC and UART2. When used by the CCDC as input CI6, it supports several modes. In 16-bit CCD AFE mode, it is input CCD14. In 16-bit YCbCr mode, it is time multiplexed between CB6 and CR6 inputs. In 8-bit YCbCr mode, it is time multiplexed between Y6, CB6, and CR6 of the upper 8-bit channel. In UART2 mode, it is the transmit data output UART_TXD2.
CI5/ CCD13/ UART_CTS2	N17	I/O/Z	IPD	This pin is multiplexed between the CCDC and UART2. When used by the CCDC as input CI5, it supports several modes. In 16-bit CCD AFE mode, it is input CCD13. In 16-bit YCbCr mode, it is time multiplexed between CB5 and CR5 inputs. In 8-bit YCbCr mode, it is time multiplexed between Y5, CB5, and CR5 of the upper 8-bit channel. In UART2 mode, it is the clear to send input UART_CTS2.
CI4/ CCD12/ UART_RTS2	N16	I/O/Z	IPD	This pin is multiplexed between the CCDC and UART2. When used by the CCDC as input CI4, it supports several modes. In 16-bit CCD AFE mode, it is input CCD12. In 16-bit YCbCr mode, it is time multiplexed between CB4 and CR4 inputs. In 8-bit YCbCr mode, it is time multiplexed between Y4, CB4, and CR4 of the upper 8-bit channel. In UART2 mode, it is the ready to send output UART_RTS2.
CI3/ CCD11	N15	I	IPD	This pin is CCDC input CI3 and it supports several modes. In 16-bit CCD AFE mode, it is input CCD11. In 16-bit YCbCr mode, it is time multiplexed between CB3 and CR3 inputs. In 8-bit YCbCr mode, it is time multiplexed between Y3, CB3, and CR3 of the upper 8-bit channel.
CI2/ CCD10	M17	I	IPD	This pin is CCDC input CI2 and it supports several modes. In 16-bit CCD AFE mode, it is input CCD10. In 16-bit YCbCr mode, it is time multiplexed between CB2 and CR2 inputs. In 8-bit YCbCr mode, it is time multiplexed between Y2, CB2, and CR2 of the upper 8-bit channel.
CI1/ CCD9	M16	I	IPD	This pin is CCDC input CI1 and it supports several modes. In 16-bit CCD AFE mode, it is input CCD9. In 16-bit YCbCr mode, it is time multiplexed between CB1 and CR1 inputs. In 8-bit YCbCr mode, it is time multiplexed between Y1, CB1, and CR1 of the upper 8-bit channel.
CI0/ CCD8	M15	I	IPD	This pin is CCDC input CI0 and it supports several modes. In 16-bit CCD AFE mode, it is input CCD8. In 16-bit YCbCr mode, it is time multiplexed between CB0 and CR0 inputs. In 8-bit YCbCr mode, it is time multiplexed between Y0, CB0, and CR0 of the upper 8-bit channel.
YI7/ CCD7	L18	I	IPD	This pin is CCDC input YI7 and it supports several modes. In 16-bit CCD AFE mode, it is input CCD7. In 16-bit YCbCr mode, it is input Y7. In 8-bit YCbCr mode, it is time multiplexed between Y7, CB7, and CR7 of the lower 8-bit channel.
YI6/ CCD6	L17	I	IPD	This pin is CCDC input YI6 and it supports several modes. In 16-bit CCD AFE mode, it is input CCD6. In 16-bit YCbCr mode, it is input Y6.IPDIn 8-bit YCbCr mode, it is time multiplexed between Y6, CB6, and CR6 of the lower 8-bit channel.

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Table 2-23. VPFE Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE (1)	IPD/ IPU (2)	DESCRIPTION
YI5/ CCD5	L16	I	IPD	This pin is CCDC input YI5 and it supports several modes. In 16-bit CCD AFE mode, it is input CCD5. In 16-bit YCbCr mode, it is input Y5. In 8-bit YCbCr mode, it is time multiplexed between Y5, CB5, and CR5 of the lower 8-bit channel.
YI4/ CCD4	L15	I	IPD	This pin is CCDC input YI4 and it supports several modes. In 16-bit CCD Analog-Front-End (AFE) mode, it is input CCD4. In 16-bit YCbCr mode, it is input Y4. In 8-bit YCbCr mode, it is time multiplexed between Y4, CB4, and CR4 of the lower 8-bit channel.
YI3/ CCD3	K19	I	IPD	This pin is CCDC input YI3 and it supports several modes. In 16-bit CCD AFE mode, it is input CCD3. In 16-bit YCbCr mode, it is input Y3. In 8-bit YCbCr mode, it is time multiplexed between Y3, CB3, and CR3 of the lower 8-bit channel.
YI2/ CCD2	K18	I	IPD	This pin is CCDC input YI2 and it supports several modes. In 16-bit CCD AFE mode, it is input CCD2. In 16-bit YCbCr mode, it is input Y2. In 8-bit YCbCr mode, it is time multiplexed between Y2, CB2, and CR2 of the lower 8-bit channel.
YI1/ CCD1	K17	I	IPD	This pin is CCDC input YI1 and it supports several modes. In 16-bit CCD AFE mode, it is input CCD1. In 16-bit YCbCr mode, it is input Y1. In 8-bit YCbCr mode, it is time multiplexed between Y1, CB1, and CR1 of the lower 8-bit channel.
YI0/ CCD0	K16	I	IPD	This pin is CCDC input YI0 and it supports several modes. In 16-bit CCD AFE mode, it is input CCD0. In 16-bit YCbCr mode, it is input Y0. In 8-bit YCbCr mode, it is time multiplexed between Y0, CB0, and CR0 of the lower 8-bit channel.
GPIO1/ $\overline{\text{C\_WE}}$	E13	I/O/Z	IPD	This pin is multiplexed between GPIO and the VPFE. In GPIO mode, it is GPIO pin GPIO1. In VPFE mode, it is the CCD Controller write enable input $\overline{\text{C\_WE}}$.
GPIO4/ R0/ C_FIELD	B14	I/O/Z	IPD	This pin is multiplexed between GPIO, the VPFE, and the VPBE. In GPIO mode, it is GPIO pin GPIO4. In VPBE mode, it is RGB888 Red data bit 0 output R0. In VPFE mode, it is CCDC field identification bidirectional signal C_FIELD.

Table 2-24. VPBE Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE (1)	IPD/ IPU (2)	DESCRIPTION
VIDEO OUT (VPBE)				
HSYNC	C17	I/O/Z	IPD	VPBE Horizontal Synch Output
VSYNC	C18	I/O/Z	IPD	VPBE Vertical Synch Output
VCLK	D19	I/O/Z	IPD	VPBE Clock Output
VPBECLK	C19	I/O/Z	IPD	VPBE Clock Input
COUT0/ B3/ **BTSEL0**	A16	I/O/Z	IPD	These pins are multiplexed between ARM boot mode and the VPBE. At reset, the boot mode inputs BTSEL0 and BTSEL1 are sampled to determine the ARM boot configuration. See below for the boot modes set by these inputs. See the Bootmode section for more details. After reset, these are video encoder outputs COUT0 and COUT1, or RGB666/888 Blue output data bits 3 and 4 B3/B4.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-24. VPBE Terminal Functions (continued)

<table>
<tr><th colspan="2">SIGNAL</th><th rowspan="2">TYPE(1)</th><th rowspan="2">IPD/
IPU(2)</th><th rowspan="2" colspan="3">DESCRIPTION</th></tr>
<tr><th>NAME</th><th>NO.</th></tr>
<tr><td rowspan="5">COUT1/
B4/
BTSEL1</td><td rowspan="5">B16</td><td rowspan="5">I/O/Z</td><td rowspan="5">IPD</td><th>BTSEL1</th><th>BTSEL0</th><th>ARM Boot Mode</th></tr>
<tr><td>0</td><td>0</td><td>ARM ROM Boot (NAND) [default]</td></tr>
<tr><td>0</td><td>1</td><td>ARM EMIFA Boot (NOR)</td></tr>
<tr><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>ARM ROM Boot (UART)</td></tr>
<tr><td>COUT2/
B5/
EM_WIDTH</td><td>A17</td><td>I/O/Z</td><td>IPD</td><td colspan="3">This pin is multiplexed between EMIFA and the VPBE. At reset, the input state is sampled to set the EMIFA data bus width (EM_WIDTH). For an 8-bit wide EMIFA data bus, EM_WIDTH = 0 [default]. For a 16-bit wide EMIFA data bus, EM_WIDTH = 1.
After reset, it is video encoder output COUT2 or RGB666/888 Blue output data bit 5 B5.</td></tr>
<tr><td>COUT3/
B6/
DSP_BT</td><td>B17</td><td>I/O/Z</td><td>IPD</td><td colspan="3">This pin is multiplexed between DSP boot and the VPBE. At reset, the input state is sampled to set the DSP boot source DSP_BT. The DSP is booted by the ARM when DSP_BT=0. The DSP boots from EMIFA when DSP_BT=1.
After reset, it is video encoder output COUT3 or RGB666/888 Blue data bit 6 output B6.</td></tr>
<tr><td>COUT4/
B7</td><td>A18</td><td>I/O/Z</td><td>IPD</td><td colspan="3">Video encoder output COUT4 or RGB666/888 Blue data bit 7 output B7.</td></tr>
<tr><td>COUT5/
G2</td><td>B18</td><td>I/O/Z</td><td>IPD</td><td colspan="3">Video encoder output COUT5 or RGB666/888 Green data bit 2 output G2.</td></tr>
<tr><td>COUT6/
G3</td><td>B19</td><td>I/O/Z</td><td>IPD</td><td colspan="3">Video encoder output COUT6 or RGB666/888 Green data bit 3 output G3.</td></tr>
<tr><td>COUT7/
G4</td><td>C16</td><td>I/O/Z</td><td>IPD</td><td colspan="3">Video encoder output COUT7 or RGB666/888 Green data bit 4 output G4.</td></tr>
<tr><td>YOUT0/
G5/
AEAW0</td><td>D15</td><td>I/O/Z</td><td>IPD</td><td rowspan="5" colspan="3">These pins are multiplexed between EMIFA and the VPBE. At reset, the input states of AEAW[4:0] are sampled to set the EMIFA address bus width. See the Peripheral Selection at Device Reset section for details.
After reset, these are video encoder outputs YOUT[0:4] or RGB666/888 Red and Green data bit outputs G5, G6, G7, R3, and R4.</td></tr>
<tr><td>YOUT1/
G6/
AEAW1</td><td>D16</td><td>I/O/Z</td><td>IPD</td></tr>
<tr><td>YOUT2/
G7/
AEAW2</td><td>D17</td><td>I/O/Z</td><td>IPD</td></tr>
<tr><td>YOUT3/
R3/
AEAW3</td><td>D18</td><td>I/O/Z</td><td>IPD</td></tr>
<tr><td>YOUT4/
R4/
AEAW4</td><td>E15</td><td>I/O/Z</td><td>IPD</td></tr>
<tr><td>YOUT5/
R5</td><td>E16</td><td>I/O/Z</td><td>IPD</td><td colspan="3">Video encoder output YOUT5 or RGB666/888 Red data bit 5 output R5.</td></tr>
<tr><td>YOUT6/
R6</td><td>E17</td><td>I/O/Z</td><td>IPD</td><td colspan="3">Video encoder output YOUT6 or RGB666/888 Red data bit 6 output R6.</td></tr>
<tr><td>YOUT7/
R7</td><td>E18</td><td>I/O/Z</td><td>IPD</td><td colspan="3">Video encoder output YOUT7 or RGB666/888 Red data bit 7 output R7.</td></tr>
<tr><td>GPIO0/
LCD_OE</td><td>C13</td><td>I/O/Z</td><td>IPD</td><td colspan="3">This pin is multiplexed between GPIO and the VPBE. In GPIO mode, it is GPIO pin GPIO0.
In VPBE mode, it is the LCD output enable LCD_OE.</td></tr>
<tr><td>GPIO2/
G0</td><td>D13</td><td>I/O/Z</td><td>IPD</td><td colspan="3">This pin is multiplexed between GPIO and the VPBE. In GPIO mode, it is GPIO pin GPIO2.
In VPBE mode, it is RGB888 Green data bit 0 output G0.</td></tr>
<tr><td>GPIO3/
B0/
LCD_FIELD</td><td>C14</td><td>I/O/Z</td><td>IPD</td><td colspan="3">This pin is multiplexed between GPIO, and the VPBE. In GPIO mode, it is GPIO pin GPIO3.
In VPBE mode, it is RGB888 Blue data bit 0 output B0.
or LCD interlaced output LCD_FIELD.</td></tr>
</table>

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Table 2-24. VPBE Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
GPIO4/ R0/ C_FIELD	B14	I/O/Z	IPD	This pin is multiplexed between GPIO, the VPFE, and the VPBE. In GPIO mode, it is GPIO pin GPIO4. In VPBE mode, it is RGB888 Red data bit 0 output R0. In VPFE mode, it is CCDC field identification bidirectional signal C_FIELD.
GPIO5/ G1	E14	I/O/Z	IPD	This pin is multiplexed between GPIO and the VPBE. In GPIO mode, it is GPIO pin GPIO5. In VPBE mode, it is RGB888 Green data bit 1 output G1.
GPIO6/ B1	A14	I/O/Z	IPD	This pin is multiplexed between GPIO and the VPBE. In GPIO mode, it is GPIO pin GPIO6. In VPBE mode, it is RGB888 Blue data bit 1 output B1.
GPIO38/ R1	D14	I/O/Z	IPD	This pin is multiplexed between VPBE and GPIO. When used by GPIO, it is GPIO38. In VPBE mode, it is RGB888 Red output data bit 1.
PWM1/ R2/ GPIO46	B15	I/O/Z	IPD	This pin is multiplexed between PWM1, VPBE, and GPIO. For PWM1, it is output PWM1. In VPBE mode, it is RGB888 Red output bit 2 (R2). For GPIO, it is GPIO46.
PWM2/ B2/ GPIO47	A15	I/O/Z	IPD	This pin is multiplexed between PWM2, VPBE, and GPIO. For PWM2, it is output PWM2. In VPBE mode, it is RGB888 Blue output bit 2 (B2). For GPIO, it is GPIO47.

Table 2-25. DAC [Part of VPBE] Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
DAC[A:D]				
DAC_VREF	R17	A I		Reference voltage input (0.5 V)
DAC_IOUT_A	P19	A O		Output of DAC A
DAC_IOUT_B	P18	A O		Output of DAC B
DAC_IOUT_C	R19	A O		Output of DAC C
DAC_IOUT_D	T19	A O		Output of DAC D
V_{DDA_1P8V}	R18	S		1.8 V Analog I/O power
V_{SSA_1P8V}	P17	GND		Analog I/O ground
V_{DDA_1P1V}	P16	S		1.20 V Analog core supply voltage (-594 device)
V_{SSA_1P1V}	T18	GND		Analog core ground
DAC_RBIAS	R16	A I		External resistor connection for current bias configuration. This must be connected via a 4 kΩ resistor to V_{SSA_1P8V}.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-26. UART0, UART1, UART2 Terminal Functions

SIGNAL NAME	NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
UART2				
CI7/ CCD15/ UART_RXD2	N19	I/O/Z	IPD	This pin is multiplexed between the CCDC and UART2. When used by the CCDC as input CI7, it supports several modes. In 16-bit CCD Analog-Front-End (AFE) mode, it is input CCD15. In 16-bit YCbCr mode, it is time multiplexed between CB7 and CR7 inputs. In 8-bit YCbCr mode, it is time multiplexed between Y7, CB7, and CR7 of the upper 8-bit channel. When used by UART2 it is the receive data input UART_RXD2.
CI6/ CCD14/ UART_TXD2	N18	I/O/Z	IPD	This pin is multiplexed between the CCDC and UART2. When used by the CCDC as input CI6, it supports several modes. In 16-bit CCD AFE mode, it is input CCD14. In 16-bit YCbCr mode, it is time multiplexed between CB6 and CR6 inputs. In 8-bit YCbCr mode, it is time multiplexed between Y6, CB6, and CR6 of the upper 8-bit channel. In UART2 mode, it is the transmit data output UART_TXD2.
CI5/ CCD13/ UART_CTS2	N17	I/O/Z	IPD	This pin is multiplexed between the CCDC and UART2. When used by the CCDC as input CI5, it supports several modes. In 16-bit CCD AFE mode, it is input CCD13. In 16-bit YCbCr mode, it is time multiplexed between CB5 and CR5 inputs. In 8-bit YCbCr mode, it is time multiplexed between Y5, CB5, and CR5 of the upper 8-bit channel. In UART2 mode, it is the clear to send input UART_CTS2.
CI4/ CCD12/ UART_RTS2	N16	I/O/Z	IPD	This pin is multiplexed between the CCDC and UART2. When used by the CCDC as input CI4, it supports several modes. In 16-bit CCD AFE mode, it is input CCD12. In 16-bit YCbCr mode, it is time multiplexed between CB4 and CR4 inputs. In 8-bit YCbCr mode, it is time multiplexed between Y4, CB4, and CR4 of the upper 8-bit channel. In UART2 mode, it is the ready to send output UART_RTS2.
UART1				
DMACK/ UART_TXD1	H3	I/O/Z	IPD	This pin is multiplexed between ATA/CF and UART1. For ATA/CF, it is DMA acknowledge output DMACK. For UART1, it is transmit data output UART_TXD1.
DMARQ/ UART_RXD1	G1	I/O/Z	IPD	This pin is multiplexed between ATA/CF and UART1. For ATA/CF, it is DMA request DMARQ input. For UART1, it is receive data input UART_RXD1.
UART0				
UART_RXD0/ GPIO35	D5	I/O/Z	IPD	This pin is multiplexed between UART0 and GPIO. For UART0, it is Receive Data input UART_RXD0. For GPIO, it is GPIO35.
UART_TXD0/ GPIO36	C5	I/O/Z	IPD	This pin is multiplexed between UART0 and GPIO. For UART0, it is Transmit Data output UART_TXD0. For GPIO, it is GPIO36.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-27. PWM0, PWM1, PWM2 Terminal Functions

SIGNAL NAME	NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
PWM2				
PWM2/ B2/ GPIO47	A15	I/O/Z	IPD	This pin is multiplexed between PWM2, VPBE, and GPIO. For PWM2, it is output PWM2. For the VPBE, it is RGB888 Blue output bit 2 (B2). For GPIO, it is GPIO47.
PWM1				

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

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Table 2-27. PWM0, PWM1, PWM2 Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
PWM1/ R2/ GPIO46	B15	I/O/Z	IPD	This pin is multiplexed between PWM1, VPBE, and GPIO. For PWM1, it is output PWM1. For the VPBE, it is RGB888 Red output bit 2 (R2). For GPIO, it is GPIO46.
PWM0				
PWM0/ GPIO45	C15	I/O/Z	IPD	This pin is multiplexed between PWM0 and GPIO. For PWM0, it is output PWM0. For GPIO, it is GPIO45.

Table 2-28. ATA/CF Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
ATA/CF				
SPI_EN1/ HDDIR/ GPIO42	B2	I/O/Z	IPD	This pin is multiplexed between SPI, ATA, and GPIO. When used by SPI, it is SPI slave device 1 enable output SPI_EN1. For ATA, it is buffer direction control output HDDIR. For GPIO, it is GPIO42.
GPIO50/ ATA_CS0	J5	O	IPD	This pin is multiplexed between GPIO and ATA/CF. In GPIO mode, it is GPIO50. In ATA mode, it is ATA/CF chip select output ATA_CS0.
GPIO51/ ATA_CS1	H1	O	IPD	This pin is multiplexed between GPIO and ATA/CF. In GPIO mode, it is GPIO51. In ATA mode, it is ATA/CF chip select output ATA_CS1.
EM_R/W/ INTRQ	G3	I	IPD	This pin is multiplexed between EMIFA and ATA/CF. For EMIFA, it is EMIF read/write output EM_R/W. For ATA/CF, it is interrupt request input INTRQ.
EM_WAIT/ (RDY/BSY)/ IORDY	F1	I	IPD	This pin is multiplexed between EMIFA (NAND/SmartMedia/xD) and ATA/CF. For EMIFA, it is wait state extension input EM_WAIT. For NAND/SmartMedia/xD, it is ready/busy input (RDY/BSY). For ATA/CF, it is IO Ready input IORDY.
EM_OE/ (RE)/ (IORD)/ DIOR	H4	O	IPD	This pin is multiplexed between EMIFA (NAND/SmartMedia/xD) and ATA/CF. For EMIFA, it is output enable output EM_OE. For NAND/SmartMedia/xD, it is read enable output (RE). For CF, it is read strobe output (IORD). For ATA, it is read strobe output DIOR.
EM_WE (WE) (IOWR)/ DIOW	G2	O	IPD	This pin is multiplexed between EMIFA (NAND/SmartMedia/xD) and ATA/CF. For EMIFA, it is write enable output EM_WE. For NAND/SmartMedia/xD, it is write enable output (WE). For CF, it is write strobe output (IOWR). For ATA, it is write strobe output DIOW.
DMACK/ UART_TXD1	H3	O	IPD	This pin is multiplexed between ATA/CF and UART1. For ATA/CF, it is DMA acknowledge output DMACK. For UART1, it is transmit data output UART_TXD1.
DMARQ/ UART_RXD1	G1	O	IPD	This pin is multiplexed between ATA/CF and UART1. For ATA/CF, it is DMA request DMARQ input. For UART1, it is receive data input UART_RXD1.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-28. ATA/CF Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
EM_D15/ DD15	E1	I/O/Z	IPD	These pins are multiplexed between EMIFA (NAND) and ATA/CF. In all cases they are used as a 16 bit bi-directional data bus. For EMIFA (NAND), these are EM_D[15:0]. For ATA/CF, these are DD[15:0].
EM_D14/ DD14	H5			
EM_D13/ DD13	F2			
EM_D12/ DD12	D1			
EM_D11/ DD11	G4			
EM_D10/ DD10	G5			
EM_D9/ DD9	E2			
EM_D8/ DD8	F3			
EM_D7/ DD7	C1			
EM_D6/ DD6	F4			
EM_D5/ DD5	D2			
EM_D4/ DD4	E4			
EM_D3/ DD3	E3			
EM_D2/ DD2	F5			
EM_D1/ DD1	D3			
EM_D0/ DD0	E5			
EM_A[0]/ DA2/ GPIO53	J4	I/O/Z	IPD	This pin is multiplexed between EMIFA, ATA/CF, and GPIO. For EMIFA, this is Address output EM_A[0], which is the least significant bit on a 32-bit word address. When connected to a 16-bit asynchronous memory, this pin is the 2nd bit of the address. For an 8-bit asynchronous memory, this pin is the 3rd bit of the address. For ATA/CF, it is Device address bit 2 output DA2. In GPIO mode, it is GPIO53.
EM_BA[1]/ DA1/ GPIO52	H2	I/O/Z	IPD	This pin is multiplexed between EMIFA, ATA/CF, and GPIO. For EMIFA, this is the Bank Address 1 output EM_BA[1]. When connected to a 16 bit asynchronous memory this pin is the lowest order bit of the 16-bit word address. When connected to an 8-bit asynchronous memory, this pin is the 2nd bit of the address. For ATA/CF, it is Device address bit 1 output DA1. In GPIO mode, it is GPIO52.
EM_BA[0]/ DA0	J3	I/O/Z	IPD	This pin is multiplexed between EMIFA and ATA/CF. For EMIFA, this is the Bank Address 0 output EM_BA[0]. When connected to an 8-bit asynchronous memory, this pin is the lowest order bit of the byte address. When connected to a 16-bit asynchronous memory, this pin has the same function as EMIF address pin 22 EM_A[22]. For ATA/CF, it is Device address bit 0 output DA0.

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Table 2-29. MMC/SD Terminal Functions

SIGNAL NAME	NO.	TYPE (1)	IPD/ IPU (2)	DESCRIPTION
MMC/SD				
SD_CLK	A9	O	IPD	Data clock output SD_CLK
SD_CMD	B9	O	IPD	Command IO output SD_CMD
SD_DATA3	C9	I/O/Z	IPD	These pins are the nibble wide bi-directional data bus SD_DATA[3:0].
SD_DATA2	D9	I/O/Z	IPD	
SD_DATA1	E9	I/O/Z	IPD	
SD_DATA0	D8	I/O/Z	IPD	

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-30. Timer 0, Timer 1, and Timer 2 Terminal Functions

SIGNAL NAME	NO.	TYPE (1)	IPD/ IPU (2)	DESCRIPTION
Timer 2 and Timer 1				
No external pins. The Timer 2 and Timer 1 peripheral pins are not pinned out as external pins.				
Timer 0				
CLK_OUT1/ TIM_IN/ GPIO49	E19	I/O/Z	IPD	This pin is multiplexed between the USB clock generator, timer, and GPIO. For the USB clock generator, it is clock output CLK_OUT1. This is configurable for 12 MHz or 24 MHz clock outputs. For Timer0, it is the timer event capture input TIM_IN. For GPIO, it is GPIO49.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 2-31. Reserved Terminal Functions

SIGNAL NAME	NO.	TYPE (1)	IPD/ IPU (2)	DESCRIPTION
RESERVED				
RSV1	A1			Reserved. This pin should not be connected.
RSV2	A19			Reserved. This pin should not be connected.
RSV3	W1			Reserved. This pin should not be connected.
RSV4	W19			Reserved. This pin should not be connected.
RSV5	D4	I	IPD	Reserved. This pin **must** be tied directly to V_{SS} for normal device operation.
RSV6	L3	A O		Reserved. This pin should not be connected.
RSV7	R8	A		Reserved. This pin should not be connected.

(1) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)
(2) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal

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Table 2-32. Supply Terminal Functions

SIGNAL NAME	NO.	TYPE[(1)]	IPD/ IPU[(2)]	DESCRIPTION
SUPPLY VOLTAGE PINS				
DV_{DD33}	F10	S		3.3 V I/O supply voltage (see the Power-Supply Decoupling section of this data sheet)
	F11			
	F12			
	F13			
DV_{DD18}	N5	S		1.8 V I/O supply voltage (see the Power-Supply Decoupling section of this data sheet)
	G15			
	F14			
	J15			
	H14			
	K14			
	M14			
	L13			
	G9			
	F8			
	E7			
	G7			
	J7			
	L7			
	F6			
	H6			
	K6			
	M6			
DV_{DDR2}	T5	S		1.8 V DDR2 I/O supply voltage (see the Power-Supply Decoupling section of this data sheet)
	P6			
	N7			
	P8			
	N9			
	R9			
	P10			
	N11			
	R11			
	P12			
	N13			
	R13			
	P14			
	R15			

(1) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)
(2) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal

Table 2-32. Supply Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
CV_{DD}	F15	S		1.20 V core supply voltage (-594 device) (see the Power-Supply Decoupling section of this data sheet)
	K12			
	M12			
	L11			
	M10			
	L10			
	K10			
	L9			
	L8			
	M8			
CV_{DDDSP}	J13	S		1.20 V DSPSS supply voltage (-594 devices) (see the Power-Supply Decoupling section of this data sheet)
	H12			
	H11			
	J11			
	K11			
	J10			
	H10			
	J9			
	K9			
	K8			
	H8			

Table 2-33. Ground Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
GROUND PINS				
V_{SS}	K5	GND		Ground pins
	M5			
	G6			
	J6			
	L6			
	N6			
	R6			
	F7			
	H7			
	K7			
	M7			
	P7			
	R7			
	E8			
	G8			
	J8			
	N8			
	F9			
	H9			
	M9			
	P9			
	G10			
	N10			
	R10			
	G11			
	M11			
	P11			
	G12			
	J12			
	N12			
	L12			
	R12			
	G13			
	H13			
	K13			
	M13			
	P13			
	G14			
	J14			

(1) IPD = Internal pulldown, IPU = Internal pullup. (To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)
(2) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal

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Table 2-33. Ground Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1)	IPD/ IPU(2)	DESCRIPTION
V_{SS}	L14	GND		Ground pins
	N14			
	R14			
	H15			
	K15			
	P15			

2.8 Device Support

2.8.1 Development Support

TI offers an extensive line of development tools for the TMS320DM644x SoC platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Intergrated Development Environment (IDE).

The following products support development of TMS320DM644x SoC-based applications:

Software Development Tools:

Code Composer Studio™ Integrated Development Environment (IDE): including Editor

C/C++/Assembly Code Generation, and Debug plus additional development tools

Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any SoC application.

Hardware Development Tools:

Extended Development System (XDS™) Emulator (supports TMS320DM644x SoC multiprocessor system debug) EVM (Evaluation Module)

For a complete listing of development-support tools for the TMS320DM644x SoC platform, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

2.8.2 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., TMX320DM6446ZWT). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications.

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

TMS Fully-qualified production device.

Support tool development evolutionary flow:

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TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

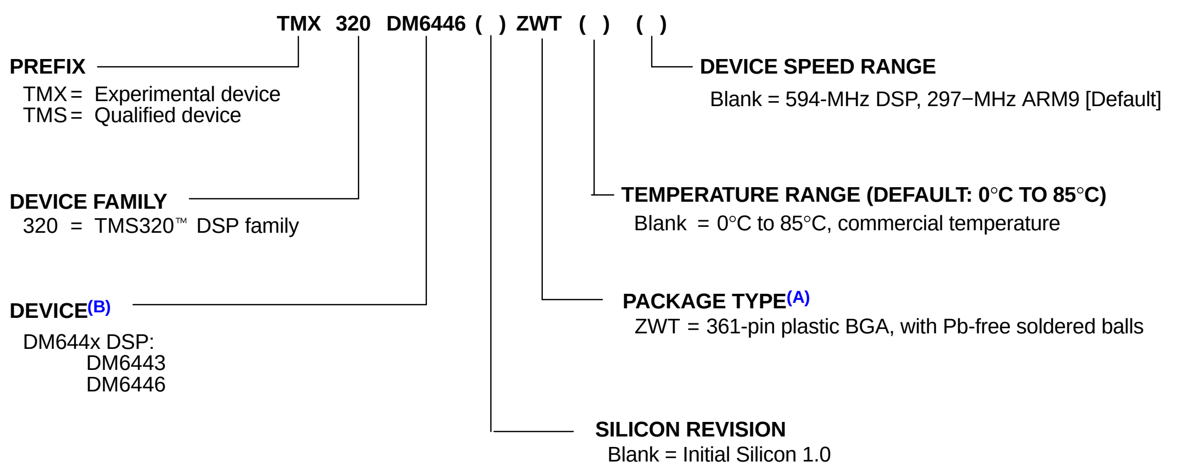
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZWT), the temperature range (for example, "Blank" is the commercial temperature range), and the device speed range in megahertz (for example, "Blank" is the default [594-MHz DSP, 297-MHz ARM9]).

Figure 2-7 provides a legend for reading the complete device name for any TMS320DM644x SoC platform member.



A. BGA = Ball Grid Array

B. For actual device part numbers (P/Ns) and ordering information, see the TI website (http://www.ti.com).

Figure 2-7. Device Nomenclature

2.8.3 Documentation Support

2.8.3.1 Related Documentation From Texas Instruments

The following documents describe the TMS320DM644x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the DM644x DMSoC, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

SPRUE14 ***TMS320DM644x DMSoC ARM Subsystem Reference Guide.*** Describes the ARM subsytem in the TMS320DM644x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the DSP subsystem, the video processing subsystem, and a majority of the peripherals and external memories.

SPRUE15 ***TMS320DM644x DMSoC DSP Subsystem Reference Guide.*** Describes the digital signal processor (DSP) subsystem in the TMS320DM644x Digital Media System-on-Chip (DMSoC).

SPRUE19 ***TMS320DM644x DMSoC Peripherals Overview Reference Guide.*** Provides an overview and briefly describes the peripherals available on the TMS320DM644x Digital Media System-on-Chip (DMSoC).

SPRAA84 ***TMS320C64x to TMS320C64x+ CPU Migration Guide.*** Describes migrating from the Texas Instruments TMS320C64x digital signal processor (DSP) to the TMS320C64x+ DSP. The objective of this document is to indicate differences between the two cores. Functionality in the devices that is identical is not included.

SPRU732 ***TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide.*** Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

SPRU871 ***TMS320C64x+ DSP Megamodule Reference Guide.*** Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

SPRAAA6 ***EDMA v3.0 (EDMA3) Migration Guide for TMS320DM644x DMSoC.*** Describes migrating from the Texas Instruments TMS320C64x digital signal processor (DSP) enhanced direct memory access (EDMA2) to the TMS320DM644x Digital Media System-on-Chip (DMSoC) EDMA3. This document summarizes the key differences between the EDMA3 and the EDMA2 and provides guidance for migrating from EDMA2 to EDMA3.

3 Device Configuration

3.1 System Module Registers

The system module includes status and control registers required for configuration of the device. Brief descriptions of the various registers are shown in Table 3-1. System Module registers required for device configurations are discussed in the following sections.

Table 3-1. System Module Register Memory Map

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x01C4 0000	PINMUX0	Pin multiplexing control 0. See Section 3.6.4 for details.
0x01C4 0004	PINMUX1	Pin multiplexing control 1. See Section 3.6.5 for details.
0x01C4 0008	DSPBOOTADDR	Boot address of DSP. See Section 3.4.1.2 for details.
0x01C4 000C	SUSPSRC	Emulator Suspend Source. See Section 3.7 for details.
0x01C4 0010	INTGEN	ARM/DSP Interrupt Status and Control. See ARM/DSP Communucations Interrupts section for details.
0x01C4 0014	BOOTCFG	Device boot configuration. See Section 3.4.1.1 for details.
0x01C4 0018 - 0x01C4 0027	–	Reserved
0x01C4 0028	DEVICE_ID	Device ID number. See the JTAG section for details.
0x01C4 002C	–	Reserved
0x01C4 0030	–	Reserved
0x01C4 0034	USBPHY_CTL	USB PHY control. See the USB peripheral section for details.
0x01C4 0038	CHP_SHRTSW	Chip shorting switch control. See Section 3.2.1 for details.
0x01C4 003C	MSTPRI0	Bus master priority control 0. See Section 3.6.1 for details.
0x01C4 0040	MSTPRI1	Bus master priority control 1. See Section 3.6.1 for details.
0x01C4 0044	VPSS_CLKCTL	VPSS clock control.
0x01C4 0048	VDD3P3V_PWDN	VDD 3.3V I/O powerdown control. See Section 3.2.2 for details.
0x01C4 004C	DRRVTPER	Enables access to the DDR2 VTP Register
0x01C4 0050 - 0x01C4 006F	–	Reserved

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3.2 Power Considerations

Global device power domains are controlled by the Power and Sleep Controller, except as shown in the following sections.

3.2.1 Power Configurations at Reset

As described in the *DM6446 Power and Clock Domains* section, the DM6446 has two power domains: Always On and DSP. There is a shorting switch between the two power domains that must be opened when the DSP domain is powered off and closed when the DSP domain is powered on.

The CHP_SHRTSW register, shown in Figure 3-1, controls the shorting switch between the device always-on and DSP power domains. This switch should be enabled after powering-up the DSP domain. Setting the DSPPWRON bit to '1' closes (enables) the switch and enables the DSP power domain. The default switch value is determined by the DSP_BT configuration input. If DSP self boot is selected (DSP_BT=1), the DSP will be powered-up and DSPPWRON will be set to a value of '1'. For ARM boot operation (DSP_BT=0), DSPPWRON will be set to the disable value of '0' and must be set by the ARM before the DSP domain power is turned on.

Figure 3-1. CHP_SHRTSW Register

31–16
RESERVED
R-0000 0000 0000 0000

15–1	0
RESERVED	DSP PWR ON
R-0000 0000 0000 000	R/W-L

LEGEND: R = Read, W = Write, n = value at reset, L = pin state latched at reset rising

Table 3-2. CHP_SHRTSW Register Description

NAME	DESCRIPTION
DSPPWRON	DSP power domain enable. 0 = DSP power domain off 1 = DSP power domain on

3.2.2 *Power Configurations after Reset*

The VDD3P3V_PWDN register controls power to the 3.3V I/O buffers for MMC/SD and GPIOV33. The 3.3V I/Os are separated into two groups for independent control as shown in Figure 3-2 and described in Table 3-3. By default, these pins are all disabled at reset.

The VDD3P3V_PWDN register controls power to the 3.3V I/O buffers for MMC/SD and GPIOV33. The 3.3V I/Os are separated into two groups for independent control as shown in Figure 3-2 and described in Table 3-3. By default, these pins are all disabled at reset.

Figure 3-2. VDD3P3V_PWDN Register

31–16
RESERVED
R-0000 0000 0000 0000

15–2	1	0
RESERVED	IO PWDN1	IO PWDN0
R-0000 0000 0000 00	R/W-1	R/W-1

LEGEND: R = Read, W = Write, n = value at reset

Table 3-3. VDD3P3V_PWDN Register Description

NAME	DESCRIPTION
IOPWDN0	MMC/SD I/O Powerdown controls SD_CLK, SD_CMD, SD_DATA[3:0] pins. 0 = I/O buffers powered up 1 = I/O buffers powered down
IOPWDN1	GIOV33 I/O Powerdown controls GIOV33[16:0] pins. 0 = I/O buffers powered up 1 = I/O buffers powered down

3.3 Clocks Considerations

Global device and local peripheral clocks are controlled by the Power and Sleep Controller, except as shown in the following sections.

3.3.1 Clock Configurations at Reset

TBD

3.3.2 Clock Configurations after Power-On/Hard Reset

As described in the DM6446 *Power and Clock Domains* section, the DM6446 system includes two separate power domains and up to forty-one separate modules. The "AlwaysOn" power domain is always on when the chip is on. The "AlwaysOn" domain is powered by the CV_{DD} pin of the DM6446 chip. The majority of the DM6446 modules lie within the "AlwaysOn" power domain. The DSP Subsystem lies in a separate domain that is not always on. This domain is referred to as the "DSP" domain. The DSP power domain is powered by the CV_{DDDSP} pin of the device.

Table 3-4 shows the state of each module after a chip Power-On/Hard Reset. The default state of the "DSP" power domain and the DSP module is determined by the DSP boot select pin (COUT3/B6/**DSP_BT**). If the DSP is selected to self boot (COUT3/B6/**DSP_BT** = 1) at reset, the "DSP" domain will power up by default.

Table 3-4. Module Configuration

		DEFAULT STATES		
			MODULE	
MODULE NAME	POWER DOMAIN	POWER DOMAIN STATE	MODULE STATE	LOCAL RESET STATE
VPSS	Always On	ON	Disable	-
EDMA	Always On	ON	BTSEL[1:0] = 00 - Enable (NAND) BTSEL[1:0] = 01 - Enable (NOR) BTSEL[1:0] = 10 - Reserved BTSEL[1:0] = 11- Enable (UART)	-
USB2.0	Always On	ON	Disable	-
ATA/CF	Always On	ON	Disable	-
VLNYQ	Always On	ON	Disable	-
DDR2 EMIF	Always On	ON	Disable	-
EMIFA	Always On	ON	BTSEL[1:0] = 00 - Enable (NAND) BTSEL[1:0] = 01 - Enable (NOR) BTSEL[1:0] = 10 - Reserved BTSEL[1:0] = 11- Enable (UART)	-
MMC/SD	Always On	ON	Disable	-
ASP	Always On	ON	Disable	-
I2C	Always On	ON	Disable	-
UART0	Always On	ON	BTSEL[1:0] = 00 - SyncRst (NAND) BTSEL[1:0] = 01 - SyncRst (NOR) BTSEL[1:0] = 10 - Reserved BTSEL[1:0] = 11- Enable (UART)	-
UART1	Always On	ON	Disable	-
UART2	Always On	ON	Disable	-
SPI	Always On	ON	Disable	-
PWM0	Always On	ON	Disable	-
PWM1	Always On	ON	Disable	-
PWM2	Always On	ON	Disable	-
GPIO	Always On	ON	Disable	-
TIMER0	Always On	ON	Enable	-
TIMER1	Always On	ON	Disable	-
TIMER2	Always On	ON	Enable	-
EMAC/MDIO	Always On	ON	Disable	-

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Table 3-4. Module Configuration (continued)

		DEFAULT STATES		
System Module	Always On	ON	Enable	-
ARM	Always On	ON	Enable	-
Switched Central Resource (SCR)	Always On	ON	Enable	-
DSP	DSP	OFF	COUT3_DSP_BT	COUT3_DSP_BT
VICP	DSP	OFF	Disable	-

3.3.2.1 Power Domain and Module States Defined

3.3.2.1.1 Power Domain States

A power domain can only be in one of two states – **ON** or **OFF**, defined as follows:

- **ON**: Power to the power domain is on.
- **OFF**: Power to the power domain is off.

3.3.2.1.2 Module States

A module can be in one of four states – **Disable**, **Enable**, **SwRstDisable**, or **SyncReset**. As shown in Table 3-5, the four states correspond to combinations of module reset asserted or de-asserted and module clock on or off.

Table 3-5. Module States

MODULE STATE	MODULE RESET	MODULE CLOCK
Enable	De-Asserted	ON
Disable	De-Asserted	OFF
SyncReset	Asserted	ON
SwRstDisable	Asserted	OFF

The module states are defined as follows:

- **Enable**: A module in the ***enable*** state has its module reset ***de-asserted*** and its clock ***on***.
- **Disable**: A module in the ***disable*** state has its module reset ***de-asserted*** and its clock ***off***. This state is typically used for disabling a module clock for power savings. The DM6446 is designed in full static CMOS, so when you stop a module clock, the modules state is retained. When the clock is restarted, the module resumes operating from the point it was stopped.
- **SyncRst**: A module in the ***SyncRst*** state has its module reset ***asserted*** and its clock ***on***. After initial power-on, most modules are by default in the SyncRst state.
- **SwRstDisable**: A module in the **SwRstDisable** state has its module reset ***asserted*** and its clock ***off***.

3.3.2.2 DAC and Video Encoder Clocks

The DAC and Video Encoder Clocks within the Video Processing SubSystem (VPSS) are controlled via the VPSS_CLK_CTRL register as shown in Figure 3-3. Descriptions of the register fields are given in Table 3-6.

Figure 3-3. VPSS_CLK_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0000 0000 0000 0000															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DAC CLKEN	VEN CLKEN	PCLK_INV	VPSS_MUXSEL	
R-0000 0000 000											R/W-0	R/W-0	R/W-0	R/W-00	

LEGEND: R = Read, W = Write, n = value at reset

Table 3-6. VPSS_CLK_CTRL Register Description

Name	Description		
DACCLKEN	Video DAC clock control 0 = DAC clock disabled 1 = DAC clock enabled		
VENCLKEN	Video Encoder clock control 0 = Video Encoder clock disabled 1 = Video Encoder clock enabled		
PCLK_INV	Video Encoder PCLK polarity control 0 = VENC clock mux and CCDC receives normal PCLK 1 = VENC clock mux and CCDC receives inverted PCLK		
VPSS_MUXSEL	Video Encoder and DAC clock selection		
	VPSS_MUXSEL [1:0]	VENC Clock	DAC Clock
	00	MXI (27 MHz)	MXI (27 MHz)
	01	MXI x 2 (54 MHz)	MXI x 2 (54 MHz)
	10	VPBECLK input	VPBECLK input
	11	PCLK or inverted PCLK	off

3.4 Bootmode

The device is booted through multiple means: pin states captured at reset, primary bootloaders within internal ROM or EMIFA, and secondary user bootloaders from peripherals or external memories. Boot modes, pin configurations, and register configurations required for booting the device, are described in the following sections.

3.4.1 Bootmode Registers

The BOOTCFG and DSPBOOTADDR registers are described in the following sections. At reset, the status of various pins required for proper boot are stored within these registers.

3.4.1.1 BOOTCFG Register Description

The BOOTCFG register (located at address 0x01C4 000A) contains the status values of the BTSEL1, BTSEL0, DSP_BT, EM_WIDTH, and AEAW[4:0] pins captured at the rising edge of $\overline{\text{RESET}}$. The register format is shown in Figure 3-4 and bit field descriptions are shown in Table 3-7. The captured bits are software readable after reset.

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Figure 3-4. BOOTCFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0000 0000 0000 0000															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							DSP_ BT	BTSEL		EM_ WIDTH	DAEAW				
R-0000 000							R-L	R-LL		R-L	R-LLLLL				

LEGEND: R = Read; W = Write; L = pin state latched at reset rising; -*n* = value after reset

Table 3-7. BOOTCFG Register Description

NAME	DESCRIPTION
BTSEL	ARM Boot mode selection pin states (BTSEL1, BTSEL0) captured at the rising edge of $\overline{\text{RESET}}$. '00' indicates ARM boots from ROM (NAND Flash). '01' indicates that ARM boots from EMIFA (NOR Flash). '10' RESERVED. '11' indicates that ARM boots from ROM (UART).
DSP_BT	DSP Boot mode selection pin state captured at the rising edge of $\overline{\text{RESET}}$. '0' sets ARM boot of C64x+. '1' sets C64x+ self boot.
EM_WIDTH	EMIFA data bus width selection pin state captured at the rising edge of $\overline{\text{RESET}}$. '0' sets EMIFA to 8 bit data bus width '1' sets EMIFA to 16 bit data bus width.
DAEAW	EMIFA address bus width selection pin states (AEAW[4:0]) captured at the rising edge of $\overline{\text{RESET}}$. This configures EMIFA address pins multiplexed with GPIO. See Table 3-12,Table 3-13, and Table 3-14

3.4.1.2 DSPBOOTADDR Register Description

The DSPBOOTADDR register contains the upper 22 bits of the C64x+ DSP reset vector. The register format is shown in Figure 3-5 and bit field descriptions are shown in Table 3-8. DSPBOOTADDR is readable and writable by software after reset.

Figure 3-5. DSPBOOTADDR Registers

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BOOT ADDR 21	BOOT ADDR 20	BOOT ADDR 19	BOOT ADDR 18	BOOT ADDR 17	BOOT ADDR 16	BOOT ADDR 15	BOOT ADDR 14	BOOT ADDR 13	BOOT ADDR 12	BOOT ADDR 11	BOOT ADDR 10	BOOT ADDR 19	BOOT ADDR 8	BOOT ADDR 7	BOOT ADDR 6
R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOT ADDR 5	BOOT ADDR 4	BOOT ADDR 3	BOOT ADDR 2	BOOT ADDR 1	BOOT ADDR 0	RESERVED									
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-00 0000 0000									

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 3-8. DSPBOOTADDR Register Description

NAME	DESCRIPTION
BOOTADDR[21:0]	Upper 22 bits of the C64x+ DSP boot address.

3.4.2 ARM Boot

The DM6446 ARM can boot from EMIFA, internal ROM (NAND) or UART as determined by the setting of the BTSEL[1:0] pins. The BTSEL[1:0] pins are read by the ARM ROM Boot Loader (RBL) to further define the ROM boot mode. The ARM boot modes are summarized in Table 3-9.

Table 3-9. ARM Boot Modes

BTSEL1	BTSEL0	Boot Mode	ARM Reset Vector	Brief Description
0	0	ARM NAND RBL	0x0000 4000	Up to 14 K-bytes secondary boot loader through NAND with up to 2 K-bytes page sizes.
0	1	ARM EMIFA External Boot	0x0200 0000	EMIFA EM_CS2 external memory space.
1	0	Reserved	0x0000 4000	Reserved
1	1	ARM UART RBL	0x0000 4000	Up to 14 K-bytes secondary boot loader through UART.

When the BTSEL[1:0] pins are set to the ARM EMIFA External Boot ("01"), the ARM immediately begins executing code from the EMIFA EM_CS2 memory space (0x0200 0000). When the BTSEL[1:0] pins indicate a condition other than the ARM EMIFA External Boot (!01), the RBL begins execution.

ARM NAND Boot mode has the following features:

- No support for a full firmware boot. Instead, copies a secondary User Boot Loader (UBL) from NAND flash to ARM Internal RAM (AIM) and transfers control to the user software.
- Support for NAND with page sizes up to 2048 bytes.
- Support for error correction when loading UBL
- Support for up to 14KB UBL
- Optional, user selectable, support for use of DMA, I-cache, and PLL enable while loading UBL

ARM UART Boot mode has the following features:

- No support for a full firmware boot. Instead, loads a secondary UBL via UART to AIM and transfers control to the user software.
- Support for up to 14KB UBL

For further details on the ROM Bootloader, refer to the *ARM Subsystem Users Guide*.

3.4.3 DSP Boot

For C64x+ booting, the state of the DSP_BT pin is sampled at reset. If DSP_BT is low, the MPU will be the master of C64x+ and control booting (Host Boot mode). If DSP_BT is high, the C64x+ will boot itself coming out of device reset (Self-Boot mode). Table 3-10 shows a summary of the DSP boot modes.

Table 3-10. DSP Boot Modes

DSP_BT	DSP Boot Mode	ARM Boot Mode	DSPBOOTADDR Register Value	Brief Description
0	Host Boot	Internal Boot	Programmable	ARM sets an internal DSP memory location in DSPBOOTADDR register where valid DSP code resides and loads code to this internal DSP memory through DMA prior to releasing DSP reset.
0	Host Boot	External Boot	Programmable	ARM sets an external DSP memory location in DSPBOOTADDR register (EMIFA or DDR2) where valid DSP code resides prior to releasing DSP reset.
1	Self Boot	Any	0x4220 0000	Default EMIFA Base Address

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3.4.3.1 Host-Boot Mode

In host boot mode, the ARM is the master and controls the reset and boot of the C64x+. The C64x+ DSP remains powered-off after device reset. The ARM is responsible for enabling power to the C64x+ and releasing it from reset (PSC MMR bits: MDCTL[39].LRST and MRSTOUT1.MRSTz[39]). Prior to releasing the C64x+ reset, the ARM must program the address from which the C64x+ will begin execution in the DSPBOOTADDR register.

3.4.3.2 Self-Boot Mode

In self-boot mode, the C64x+ power domain is turned on and the C64x+ DSP is released from reset without ARM intervention. The C64x+ begins execution from the default EMIFA address (0x4220 0000) contained within the DSPBOOTADDR register. The C64x+ begins execution with instruction (L1P) cache enabled.

3.5 Configurations at Reset

The following sections give information on configuration settings for the device at reset.

3.5.1 Device Configuration at Device Reset

Table 3-11 shows a summary of device inputs required for booting the ARM and DSP, and configuring EMIFA data and address bus widths for proper operation of the device at the rising edge of the $\overline{\text{RESET}}$ input.

Table 3-11. Device Configurations (Input Pins Sampled at Reset)

DEVICE SIGNALS SAMPLED AT RESET	DEVICE SIGNAL NAME AFTER RESET	DESCRIPTION
BTSEL[1:0]	COUT[1:0]	ARM Boot mode selection pins. ‘00’ indicates ARM boots from ROM (NAND Flash). ‘01’ indicates that ARM boots from EMIFA (NOR Flash). ‘10’ Reserved. ‘11’ indicates that ARM boots from ROM (UART).
DSP_BT	COUT3	DSP Boot mode selection pin. ‘0’ sets ARM boot of C64x+. ‘1’ sets C64x+ self boot.
EM_WIDTH	COUT2	EMIFA data bus width selection pin. ‘0’ sets EMIFA to 8-bit data bus width ‘1’ sets EMIFA to 16-bit data bus width.
AEAW[4:0]	YOUT[4:0]	EMIFA address bus width selection pins for EMIFA address pins multiplexed with GPIO. See Table 3-12, Table 3-13, and Table 3-14 for details.

3.5.2 Peripheral Selection at Device Reset

As briefly mentioned in Table 3-11, the state of the AEAW[4:0] pins captured at reset configures the number of EMIFA address pins required for device boot. These values are stored in the AEAW field of the PINMUX0 register. At reset, this provides proper addressing for external boot. Unused address pins are available for use as GPIO. The register settings are software programmable after reset. Table 3-12, Table 3-13, and Table 3-14 show the AEAW[4:0] bit settings and the corresponding multiplexing for EMIFA address and GPIO pins.

The number of EMIFA address bits enabled is configurable from 0 to 23. EM_BA[1] and EM_A[21:0] pins that are not assigned to another peripheral and not enabled as address signals become GPIO pins. The enabled address pins are always contiguous from EM_BA[1] upwards and address bits cannot be skipped.

The exception to this are the EM_A[2:1] pins. EM_A[2:1] are usable as the ALE and CLE signals for the NAND Flash mode of EMIFA and are always enabled as EMIFA pins. If an address width of 0 is selected, this still allows a NAND Flash to be accessed. Also, selecting an address width of 2, 3, or 4 (AEAW[4:0] = 00010, 00011, or 00100) always results in 4 address outputs. For these and other address bit enable settings, see Table 3-12, Table 3-13, and Table 3-14.

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Table 3-12. GPIO and EMIFA Multiplexing (Part 1)

Pin Mux Register AEAW[4:0] Bit Settings							
00000 (default)	**00001**	**00010**	**00011**	**00100**	**00101**	**00111**	**00111**
GPIO[52]	EM_BA[1]	EM_BA[1]	EM_BA[1]	EM_BA[1]	EM_BA[1]	EM_BA[1]	EM_BA[1]
GPIO[53]	GPIO[53]	EM_A[0]	EM_A[0]	EM_A[0]	EM_A[0]	EM_A[0]	EM_A[0]
EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]
EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]
GPIO[28]	GPIO[28]	GPIO[28]	GPIO[28]	GPIO[28]	EM_A[3]	EM_A[3]	EM_A[3]
GPIO[27]	GPIO[27]	GPIO[27]	GPIO[27]	GPIO[27]	GPIO[27]	EM_A[4]	EM_A[4]
GPIO[26]	GPIO[26]	GPIO[26]	GPIO[26]	GPIO[26]	GPIO[26]	GPIO[26]	EM_A[5]
GPIO[25]	GPIO[25]	GPIO[25]	GPIO[25]	GPIO[25]	GPIO[25]	GPIO[25]	GPIO[25]
GPIO[24]	GPIO[24]	GPIO[24]	GPIO[24]	GPIO[24]	GPIO[24]	GPIO[24]	GPIO[24]
GPIO[23]	GPIO[23]	GPIO[23]	GPIO[23]	GPIO[23]	GPIO[23]	GPIO[23]	GPIO[23]
GPIO[22]	GPIO[22]	GPIO[22]	GPIO[22]	GPIO[22]	GPIO[22]	GPIO[22]	GPIO[22]
GPIO[21]	GPIO[21]	GPIO[21]	GPIO[21]	GPIO[21]	GPIO[21]	GPIO[21]	GPIO[21]
GPIO[20]	GPIO[20]	GPIO[20]	GPIO[20]	GPIO[20]	GPIO[20]	GPIO[20]	GPIO[20]
GPIO[19]	GPIO[19]	GPIO[19]	GPIO[19]	GPIO[19]	GPIO[19]	GPIO[19]	GPIO[19]
GPIO[18]	GPIO[18]	GPIO[18]	GPIO[18]	GPIO[18]	GPIO[18]	GPIO[18]	GPIO[18]
GPIO[17]	GPIO[17]	GPIO[17]	GPIO[17]	GPIO[17]	GPIO[17]	GPIO[17]	GPIO[17]
GPIO[16]	GPIO[16]	GPIO[16]	GPIO[16]	GPIO[16]	GPIO[16]	GPIO[16]	GPIO[16]
GPIO[15]	GPIO[15]	GPIO[15]	GPIO[15]	GPIO[15]	GPIO[15]	GPIO[15]	GPIO[15]
GPIO[14]	GPIO[14]	GPIO[14]	GPIO[14]	GPIO[14]	GPIO[14]	GPIO[14]	GPIO[14]
GPIO[13]	GPIO[13]	GPIO[13]	GPIO[13]	GPIO[13]	GPIO[13]	GPIO[13]	GPIO[13]
GPIO[12]	GPIO[12]	GPIO[12]	GPIO[12]	GPIO[12]	GPIO[12]	GPIO[12]	GPIO[12]
GPIO[11]	GPIO[11]	GPIO[11]	GPIO[11]	GPIO[11]	GPIO[11]	GPIO[11]	GPIO[11]
GPIO[10]	GPIO[10]	GPIO[10]	GPIO[10]	GPIO[10]	GPIO[10]	GPIO[10]	GPIO[10]

Table 3-13. GPIO and EMIFA Multiplexing (Part 2)

Pin Mux Register AEAW[4:0] Bit Settings							
01000	**01001**	**01010**	**01011**	**01100**	**01101**	**01110**	**01111**
EM_BA[1]	EM_BA[1]	EM_BA[1]	EM_BA[1]	EM_BA[1]	EM_BA[1]	EM_BA[1]	EM_BA[1]
EM_A[0]	EM_A[0]	EM_A[0]	EM_A[0]	EM_A[0]	EM_A[0]	EM_A[0]	EM_A[0]
EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]
EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]
EM_A[3]	EM_A[3]	EM_A[3]	EM_A[3]	EM_A[3]	EM_A[3]	EM_A[3]	EM_A[3]
EM_A[4]	EM_A[4]	EM_A[4]	EM_A[4]	EM_A[4]	EM_A[4]	EM_A[4]	EM_A[4]
EM_A[5]	EM_A[5]	EM_A[5]	EM_A[5]	EM_A[5]	EM_A[5]	EM_A[5]	EM_A[5]
EM_A[6]	EM_A[6]	EM_A[6]	EM_A[6]	EM_A[6]	EM_A[6]	EM_A[6]	EM_A[6]
GPIO[24]	EM_A[7]	EM_A[7]	EM_A[7]	EM_A[7]	EM_A[7]	EM_A[7]	EM_A[7]
GPIO[23]	GPIO[23]	EM_A[8]	EM_A[8]	EM_A[8]	EM_A[8]	EM_A[8]	EM_A[8]
GPIO[22]	GPIO[22]	GPIO[22]	EM_A[9]	EM_A[9]	EM_A[9]	EM_A[9]	EM_A[9]
GPIO[21]	GPIO[21]	GPIO[21]	GPIO[21]	EM_A[10]	EM_A[10]	EM_A[10]	EM_A[10]
GPIO[20]	GPIO[20]	GPIO[20]	GPIO[20]	GPIO[20]	EM_A[11]	EM_A[11]	EM_A[11]
GPIO[19]	GPIO[19]	GPIO[19]	GPIO[19]	GPIO[19]	GPIO[19]	EM_A[12]	EM_A[12]
GPIO[18]	GPIO[18]	GPIO[18]	GPIO[18]	GPIO[18]	GPIO[18]	GPIO[18]	EM_A[13]
GPIO[17]	GPIO[17]	GPIO[17]	GPIO[17]	GPIO[17]	GPIO[17]	GPIO[17]	GPIO[17]
GPIO[16]	GPIO[16]	GPIO[16]	GPIO[16]	GPIO[16]	GPIO[16]	GPIO[16]	GPIO[16]
GPIO[15]	GPIO[15]	GPIO[15]	GPIO[15]	GPIO[15]	GPIO[15]	GPIO[15]	GPIO[15]
GPIO[14]	GPIO[14]	GPIO[14]	GPIO[14]	GPIO[14]	GPIO[14]	GPIO[14]	GPIO[14]
GPIO[13]	GPIO[13]	GPIO[13]	GPIO[13]	GPIO[13]	GPIO[13]	GPIO[13]	GPIO[13]
GPIO[12]	GPIO[12]	GPIO[12]	GPIO[12]	GPIO[12]	GPIO[12]	GPIO[12]	GPIO[12]
GPIO[11]	GPIO[11]	GPIO[11]	GPIO[11]	GPIO[11]	GPIO[11]	GPIO[11]	GPIO[11]
GPIO[10]	GPIO[10]	GPIO[10]	GPIO[10]	GPIO[10]	GPIO[10]	GPIO[10]	GPIO[10]

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Table 3-14. GPIO and EMIFA Multiplexing (Part 3)

Pin Mux Register AEAW[4:0] Bit Settings							
10000	**10001**	**10010**	**10011**	**10100**	**10101**	**10110**	**Others**
EM_BA[1]	EM_BA[1]	EM_BA[1]	EM_BA[1]	EM_BA[1]	EM_BA[1]	EM_BA[1]	EM_BA[1]
EM_A[0]	EM_A[0]	EM_A[0]	EM_A[0]	EM_A[0]	EM_A[0]	EM_A[0]	EM_A[0]
EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]
EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]
EM_A[3]	EM_A[3]	EM_A[3]	EM_A[3]	EM_A[3]	EM_A[3]	EM_A[3]	EM_A[3]
EM_A[4]	EM_A[4]	EM_A[4]	EM_A[4]	EM_A[4]	EM_A[4]	EM_A[4]	EM_A[4]
EM_A[5]	EM_A[5]	EM_A[5]	EM_A[5]	EM_A[5]	EM_A[5]	EM_A[5]	EM_A[5]
EM_A[6]	EM_A[6]	EM_A[6]	EM_A[6]	EM_A[6]	EM_A[6]	EM_A[6]	EM_A[6]
EM_A[7]	EM_A[7]	EM_A[7]	EM_A[7]	EM_A[7]	EM_A[7]	EM_A[7]	EM_A[7]
EM_A[8]	EM_A[8]	EM_A[8]	EM_A[8]	EM_A[8]	EM_A[8]	EM_A[8]	EM_A[8]
EM_A[9]	EM_A[9]	EM_A[9]	EM_A[9]	EM_A[9]	EM_A[9]	EM_A[9]	EM_A[9]
EM_A[10]	EM_A[10]	EM_A[10]	EM_A[10]	EM_A[10]	EM_A[10]	EM_A[10]	EM_A[10]
EM_A[11]	EM_A[11]	EM_A[11]	EM_A[11]	EM_A[11]	EM_A[11]	EM_A[11]	EM_A[11]
EM_A[12]	EM_A[12]	EM_A[12]	EM_A[12]	EM_A[12]	EM_A[12]	EM_A[12]	EM_A[12]
EM_A[13]	EM_A[13]	EM_A[13]	EM_A[13]	EM_A[13]	EM_A[13]	EM_A[13]	EM_A[13]
EM_A[14]	EM_A[14]	EM_A[14]	EM_A[14]	EM_A[14]	EM_A[14]	EM_A[14]	EM_A[14]
GPIO[16]	EM_A[15]	EM_A[15]	EM_A[15]	EM_A[15]	EM_A[15]	EM_A[15]	EM_A[15]
GPIO[15]	GPIO[15]	EM_A[16]	EM_A[16]	EM_A[16]	EM_A[16]	EM_A[16]	EM_A[16]
GPIO[14]	GPIO[14]	GPIO[14]	EM_A[17]	EM_A[17]	EM_A[17]	EM_A[17]	EM_A[17]
GPIO[13]	GPIO[13]	GPIO[13]	GPIO[13]	EM_A[18]	EM_A[18]	EM_A[18]	EM_A[18]
GPIO[12]	GPIO[12]	GPIO[12]	GPIO[12]	GPIO[12]	EM_A[19]	EM_A[19]	EM_A[19]
GPIO[11]	GPIO[11]	GPIO[11]	GPIO[11]	GPIO[11]	GPIO[11]	EM_A[20]	EM_A[20]
GPIO[10]	GPIO[10]	GPIO[10]	GPIO[10]	GPIO[10]	GPIO[10]	GPIO[10]	EM_A[21]

3.6 Configurations After Reset

The following sections give the details on configuring the device after reset.

3.6.1 Switched Central Resource (SCR) Bus Priorities

Prioritization within the switched central resource (SCR) is selected to be either fixed or dynamic. Dynamic prioritization is based on the incoming epriority signals from each master. On DM6446, only the C64x+, VPSS, and EDMA masters actually generate epriority values. For all other masters, the value is programmed in the chip-level MSTPRI0/1 registers. The register bit fields and default priority levels for DM6446 bus masters are shown in Table 3-15. The priority levels should be tuned to obtain the best system performance for a particular application. Details on the MSTPRI0/1 registers are given in Figure 3-6 and Figure 3-7.

Table 3-15. DM6446 Default Bus Master Priorities

Priority Bit Field	Bus Master	Default Priority Level
VPSSP	VPSS	0 (VPSS PCR Register)
EDMATC0P	EDMATC0	0 (EDMACC QUEPRI Register)
EDMATC1P	EDMATC1	0 (EDMACC QUEPRI Register)
ARM_DMAP	ARM (DMA)	1
ARM_CFGP	ARM (CFG)	1
C64X+_DMAP	C64X+ (DMA)	7 (C64X+ MDMAARBE.PRI Register bit field)
C64X+_CFGP	C64X+ (CFG)	1

Table 3-15. DM6446 Default Bus Master Priorities (continued)

Priority Bit Field	Bus Master	Default Priority Level
EMACP	EMAC	4
USBP	USB	4
ATAP	ATA/CF	4
VLYNQP	VLYNQ	4
VICPP	VICP	5

Figure 3-6. MSTPRI0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED													VICPP[(1)]		
R-0000 0000 0000 0													R/W-101		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV					C64X+_CFGP			RSV	ARM_CFGP			RSV	ARM_DMAP		
R-0000 0					R/W-001			R-0	R/W-001			R-0	R/W-001		

LEGEND: R = Read; W = Write; -*n* = value after reset

(1) The VICPP bit field is configured by the Third-Party software. When modifying the MSTPRI0 register a read/modify/write must be performed to preserve the configuration set by the Third-Party software.

Figure 3-7. MSTPRI1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									RESERVED			RSV	VLYNQP		
R-0000 0000 0									R-100			R-0	R/W-100		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV	ATAP			RSV	USBP			RSV	RESERVED			RSV	EMACP		
R-0	R/W-100			R-0	R/W-100			R-0	R-100			R-0	R/W-100		

LEGEND: R = Read; W = Write; -*n* = value after reset

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3.6.2 Multiplexed Pin Configurations

There are numerous multiplexed pins that are shared by more than one peripheral. Some of these pins are configured by external pullup/pulldown resistors only at reset, and others are configured by software. As described in detail in Section 3.5.1 and Section 3.5.2, hardware configurable multiplexed pins are programmed by external pullup/pulldown resistors at reset to set the initial functionality of pins for use by a single peripheral. After reset, software configurable multiplexed pins are programmable through Memory Mapped Registers (MMR) to allow the switching of pin functionalities during run-time. See Section 3.6.3 for more details on the register settings.

A summary of the pin multiplexing is shown in Table 3-16. The EMAC peripheral shares pins with the 3.3V GPIO pins. The VLYNQ pins overlap upper EMIFA address pins resulting in a reduced EMIFA address range as the VLYNQ width is increased. The ATA peripheral shares data lines and some control signals with EMIFA. The ATA DMA pins are multiplexed with UART1. The ASP, UART0/1/2, SPI, I2C, and PWM0/1/2 all default to GPIO pins when not enabled. The VPBE function of the VPSS requires additional pins to implement the RGB888 mode. These are multiplexed with GPIOs.

Table 3-16. DM6446 Multiplexed Peripheral Pins and Multiplexing Controls

MULTIPLEXED PERIPHERALS	PRIMARY (DEFAULT) FUNCTION	SECONDARY(1) FUNCTION	TERTIARY(2) FUNCTION	SECONDARY REGISTER/PIN(3) CONTROL	TERTIARY REGISTER/PIN(3) CONTROL
EMIFA, ATA (CF)	**EMIFA:** EM_D[0:15], EM_BA[0]	**ATA (CF):** DD[0:15], DA0		**PinMux0:**ATAEN	
EMIFA (NAND), ATA (CF)	**EMIFA (NAND):** R/W, EM_WAIT (RDY/BSY), EM_OE (RE), EM_WE (WE)	**ATA (CF):** INTRQ, IORDY, DIOR(IORD) , DIOW(IOWR)		**PinMux0:**ATAEN	
VPBE LCD, GPIO	**GPIO:**GPIO[0]	**VPBE:** LCD_OE		**PinMux0:**LOEEN	
VPFE CCD, GPIO	**GPIO:**GPIO[1]	**VPFE:** C_WE		**PinMux0:**CWEN	
VPBE RGB888, GPIO	**GPIO:**GPIO[2]	**VPBE:** RGB888 G0		**PinMux0:**RGB888	
VPBE LCD/RGB888, GPIO	**GPIO:**GPIO[3]	**VPBE:** RGB888 B0	**VPBE:** LCD_FIELD	**PinMux0:**RGB888	**PinMux0:**LFLDEN
VPFE CCD, VPBE RGB888, GPIO	**GPIO:**GPIO[4]	**VPBE:** RGB888 R0	**VPFE:** CCD_FIELD	**PinMux0:**RGB888	**PinMux0:**CFLDEN
VPBE RGB888, GPIO	**GPIO:** GPIO[5:6, 38]	**VPBE:** RGB888 G1, B1, R1		**PinMux0:**RGB888	
EMIFA, VLYNQ, GPIO	**GPIO:**GPIO[8]	**EMIFA:** EM_CS5	**VLYNQ:** VLYNQ_CLOCK	**PinMux0:**AECS5	**PinMux0:**VLYNQEN
EMIFA, VLYNQ, GPIO	**GPIO:**GPIO[9]	**EMIFA:** EM_CS4	**VLYNQ:** VLYNQ_SCRUN	**PinMux0:**AECS4	**PinMux0:**VLSCREN
EMIFA, VLYNQ, GPIO	**GPIO:** GPIO[10:17]	**EMIFA:** EM_A[21:14]	**VLYNQ:** VLYNQ_TXD[0:3], VLYNQ_RXD[0:3]	**PinMux0:**AEAW, **Pins:**DAEAW[4:0]	**PinMux0:**VLYNQEN, **PinMux0:**VLYNQWD[1:0]
EMIFA, GPIO	**GPIO:** GPIO[18:28]	**EMIFA:** EM_A[13:3]		**PinMux0:**AEAW, **Pins:**DAEAW[4:0]	
ASP, GPIO	**GPIO:** GPIO[29:34]	**ASP:** (all pins)(4)		**PinMux1:**ASP	
UART0, GPIO	**GPIO:** GPIO[35:36]	**UART0:** RXD, TXD		**PinMux1:**UART0	

(1) When the Secondary function is enabled, to avoid potential contention, ensure that the Primary (if not GPIO) and Tertiary functions are disabled.
(2) When the Tertiary function is enabled, to avoid potential contention, ensure that the Primary (if not GPIO), Secondary, and other Tertiary functions are disabled.
(3) Pin states are sampled at power on reset and written into the register fields.
(4) See the Terminal Functions section for pin details.

Table 3-16. DM6446 Multiplexed Peripheral Pins and Multiplexing Controls (continued)

MULTIPLEXED PERIPHERALS	PRIMARY (DEFAULT) FUNCTION	SECONDARY[(1)] FUNCTION	TERTIARY[(2)] FUNCTION	SECONDARY REGISTER/PIN[(3)] CONTROL	TERTIARY REGISTER/PIN[(3)] CONTROL
SPI, GPIO	**GPIO:** GPIO[37, 39:41]	**SPI:** SPI_EN0, SPI_CLK, SPI_DI, SPI_DO		**PinMux1:**SPI	
SPI, ATA, GPIO	**GPIO:**GPIO[42]	**SPI:** SPI_EN1	**ATA:** HDDIR	**PinMux1:**SPI	**PinMux0:**HDIREN
I2C, GPIO	**GPIO:** GPIO[43:44]	**I2C:** SCL, SDA		**PinMux1:**I2C	
PWM0, GPIO	**GPIO:**GPIO[45]	PWM0		**PinMux1:**PWM0	
PWM1, VPBE (RGB666/RGB888), GPIO	**GPIO:**GPIO[46]	**VPBE:** RGB666/RGB888 R2	**PWM1:** PWM1	**PinMux0:**RGB666/ **PinMux0:**RGB888	**PinMux1:**PWM1
PWM2, VPBE (RGB666/RGB888), GPIO	**GPIO:**GPIO[47]	**VPBE:** RGB666/RGB888 B2	**PWM2:** PWM2	**PinMux0:**RGB666/ **PinMux0:**RGB888	**PinMux1:**PWM2
ClockOut0, GPIO	**GPIO:**GPIO[48]	CLK_OUT0		**PinMux1:**CLK0	
ClockOut1, TIMER0, GPIO	**GPIO:**GPIO[49]	CLK_OUT1	**TIMER0:** TIM_IN	**PinMux1:**CLK1	**PinMux1:**TIM_IN
ATA, GPIO	**GPIO:** GPIO[50:51]	**ATA:** ATA_CS0, ATA_CS1		**PinMux0:**ATAEN	
EMIFA, GPIO, ATA (CF)	**GPIO:**GPIO[52]	**EMIFA:** EM_BA[1]	**ATA (CF):** DA1	**PinMux0:**AEAW[4:0], **Pins:**DAEAW[4:0]	**PinMux0:**ATAEN
EMIFA, ATA (CF), GPIO	**GPIO:**GPIO[53]	**EMIFA:** EM_A[0]	**ATA (CF):** DA2	**PinMux0:**AEAW[4:0], **Pins**:DAEAW[4:0]	**PinMux0:**ATAEN, **Pins:**BTSEL[1:0] = 10
EMAC, GPIO3V	**GPIO:** GPIO3V[0:13]	**EMAC:** (all pins, except CRS)[(4)]		**PinMux0:**EMACEN	
EMAC, MDIO, GPIO3V	**GPIO:** GPIO3V[14:16]	**EMAC:** CRS, **MDIO:** MDIO, MDCLK		**PinMux0:**EMACEN	
UART1, ATA (CF)	N/A	**ATA (CF):** DMACK,DMARQ	**UART1:** TXD, RXD	**PinMux0:**ATAEN	**PinMux1:**UART1
UART2, VPFE	**VPFE:** CI[7:6]/ CCD_DATA[15:14]	**UART2:** UART_RXD2, UART_TXD2		**PinMux1:**UART2	
UART2, VPFE	**VPFE:** CI[5:4]/ CCD_DATA[13:12]	**UART2:** UART_CTS2, UART_RTS2		**PinMux1:**UART2, **PinMux1:**U2FLO	

3.6.3 Peripheral Selection After Device Reset

After device reset, the PINMUX0 and PINMUX1 registers are software programmable to allow multiplexing of shared device pins between peripherals, as given in the Terminal Functions section. Section 3.6.4, Section 3.6.5, and Section 3.6.6 identify the register settings necessary to configure specific multiplexed functions and show the primary (default) function after reset.

3.6.4 PINMUX0 Register Description

The PINMUX0 pin multiplexing register controls which peripheral is given ownership over shared pins among EMAC, CCD, LCD, RGB888, RGB666, ATA, VLYNQ, EMIFA, and GPIO peripherals. The register format is shown in Figure 3-8 and bit field descriptions are given in Table 3-17. More details on the PINMUX0 pin muxing fields are given in Section 3.6.6. A value of "1" enables the secondary or tertiary pin function.

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Figure 3-8. PINMUX0 Register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EMACEN	RSV	RSV	RSV	CFLDEN	CWEN	LFLDEN	LOEEN	RGB888	RGB666	RESERVED				ATAEN	HDIREN
R/W-0	R/W-0	R/W-D	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0000				R/W-0	R/W-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VLYNQEN	VLSCREN	VLYNQWD		AECS5	AECS4	RESERVED					AEAW				
R/W-0	R/W-0	R/W-00		R/W-0	R/W-0	R-00000					R/W-LLLL				

LEGEND: R = Read; W = Write; L = pin state latched at reset rising edge; D = derived from pin states; -*n* = value after reset

(1) For proper DM6446 device operation, ***always*** write a value of '0' to RSV bits 30 and 29

Table 3-17. PINMUX0 Register Description

Name	Description
EMACEN	Enable EMAC and MDIO function on default GPIO3V[0:16] pins.
CFLDEN	Enable CCD C_FIELD function on default GPIO[4] pin
CWEN	Enable CCD C_WEN function on default GPIO[1] pin
LFLDEN	Enable LCD_FIELD function on default GPIO[3] pin
LOEEN	Enable LCD_OE function on default GPIO[0] pin
RGB888	Enable VPBE RGB888 function on default GPIO[2:6, 46:47] pins
RGB666	Enable VPBE RGB666 function on default GPIO[46:47] pins
ATAEN	Enable ATA function on default EMIFA and GPIO[52:53] pins and shared UART1 pins
HDIREN	Enable HDDIR function on default GPIO[42] pin
VLYNQEN	Enable VLYNQ function on default GPIO[9,10:17] pins
VLSCREN	Enable VLYNQ SCRUN function on default GPIO[9] pin
VLYNQWD	VLYNQ data width selection. This expands the VLYNQ TXD[0:3] and RXD[0:3] functions on default GPIO[10:17] pins.
AECS5	Enable EMIFA EM_CS5 function on GPIO[8]
AECS4	Enable EMIFA EM_CS4 function on GPIO[9]
AEAW	EMIFA address width selection. Default value is latched at reset from AEAW[4:0] configuration input pins. This enables EMIF address function on default GPIO[10:28] pins.

3.6.5 PINMUX1 Register Description

The PINMUX1 pin multiplexing register controls which peripheral is given ownership over shared pins among Timer, PLL, ASP, SPI, I2C, PWM, and UART peripherals. The register format is shown in Figure 3-9 and bit field descriptions are given in Table 3-18. More details on the PINMUX1 pin muxing fields are given in Section 3.6.6. A value of "1" enables the secondary or tertiary pin function.

Figure 3-9. PINMUX1 Register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED													TIMIN	CLK1	CLK0
R-0000 0000 0000 0													R/W-0	R/W-0	R/W-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					ASP	RSV	SPI	I2C	PWM2	PWM1	PWM0	U2FLO	UART2	UART1	UART0
R-0000 0					R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) For proper DM6446 device operation, ***always*** write a value of '0' to RSV bit 9.

Table 3-18. PINMUX1 Register Description

Name	Description
TIMIN	Enable TIM_IN function on default GPIO[49] pin
CLK1	Enable CLK_OUT1 function on default GPIO[49] pin
CLK0	Enable CLK_OUT0 function on default GPIO[48] pin
ASP	Enable ASP function on default GPIO[29:34] pins
SPI	Enable SPI function on default GPIO[37,39:42] pins
I2C	Enable I2C function on default GPIO[43:44] pins
PWM2	Enable PWM2 function on default GPIO[47] pin
PWM1	Enable PWM1 function on default GPIO[46] pin
PWM0	Enable PWM0 function on default GPIO[45] pin
U2FLO	Enable UART2 flow control function on default VPFE CI[5:4]/CCD_DATA[13:12] pins
UART2	Enable UART2 function on default VPFE CI[7:6]/CCD_DATA[15:14] pins
UART1	Enable UART1 function on shared ATA (CF) DMACK, DMARQ pins
UART0	Enable UART0 function on default GPIO[35:36] pins

3.6.6 *Pin Multiplexing Register Field Details*

The bit fields for various pin multiplexing options within the PINMUX0 and PINMUX1 registers are described in the following sections.

3.6.6.1 EMAC and GPIO3V Pin Multiplexing

The EMAC pin functions are selected as shown in Table 3-19. The functionality for each of the individual pins affected by the PINMUX0 field settings is given in Table 3-20.

Table 3-19. EMAC and GPIO3V Pin Multiplexing Control

EMACEN	PIN FUNCTIONALITY SELECTED
0	GPIO3V
1	EMAC

Table 3-20. EMAC and GPIO3V Multiplexed Pins

GPIO	EMAC
GPIO3V[0]	TXEN
GPIO3V[1]	TXCLK
GPIO3V[2]	COL
GPIO3V[3]	TXD[0]
GPIO3V[4]	TXD[1]
GPIO3V[5]	TXD[2]
GPIO3V[6]	TXD[3]
GPIO3V[7]	RXD[0]
GPIO3V[8]	RXD[1]
GPIO3V[9]	RXD[2]
GPIO3V[10]	RXD[3]
GPIO3V[11]	RXCLK
GPIO3V[12]	RXDV
GPIO3V[13]	RXER
GPIO3V[14]	CRS

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Table 3-20. EMAC and GPIO3V Multiplexed Pins (continued)

GPIO	EMAC
GPIO3V[15]	MDIO
GPIO3V[16]	MDCLK

3.6.6.2 VPFE (CCD), VPBE (LCD), and GPIO Pin Multiplexing

The CCD and LCD controllers in the VPSS require multiplex control bit settings for certain modes of operation. Bits within the PinMux0 register, which select between the CCD or LCD control signal function and GPIO, are summarized in Table 3-21.

Table 3-21. VPFE (CCD), VPBE (LCD), and GPIO Pin Multiplexing

PINMUX0 REGISTER FIELDS				MULTIPLEXED PINS			
CFLDEN	LFLDEN	CWEN	LOEEN	C_FIELD/ R0/ GPIO[4]	LCD_FIELD/ B0/ GPIO[3]	C_WEN/ GPIO[1]	LCD_OE/ GPIO[0]
-	-	-	0	-	-	-	GPIO[0]
-	-	-	1	-	-	-	LCD_OE
-	-	0	-	-	-	GPIO[1]	-
-	-	1	-	-	-	C_WEN	-
-	0	-	-	-	B0/GPIO[3][(1)]	-	-
-	1	-	-	-	LCD_FIELD	-	-
0	-	-	-	R0/GPIO[4][(1)]	-	-	-
1	-	-	-	C_FIELD	-	-	-

(1) Depends on RGB888 bit setting, see Table 3-22

3.6.6.3 VPBE (RGB666 and RGB888) and GPIO Pin Multiplexing

Use of the RGB666 and RGB888 modes of the VPBE requires enabling RGB pins as shown in Table 3-22 and Table 3-23. Enabling PWM2, PWM1, CCD, and LCD functionality overrides the the RGB modes. RGB666 interface pin functionality requires setting the RGB666 PINMUX0 Register bit field to ‘1’ and PINMUX1 Register bit fields PWM2 and PWM1 to ‘0’. Proper RGB888 interface operation requires setting PINMUX0 Register bit field RGB888 to ‘1’ and bit fields PWM2, PWM1, CFLDEN, and LFLDEN must be set to ‘0’.

Table 3-22. VPBE (RGB666, RGB888, and LCD), VPFE (CCD), and GPIO Pin Multiplexing

PINMUX0 AND PINMUX1 REGISTER BIT FIELDS						MULTIPLEXED PINS			
RGB888	RGB666	PWM2	PWM1	CFLDEN	LFLDEN	PWM2/ B2/ GPIO[47]	PWM1/ R2/ GPIO[46]	C_FIELD/ R0/ GPIO[4]	LCD_FIELD/ B0/ GPIO[3]
0	0	0	0	0	0	GPIO[47]	GPIO[46]	GPIO[4]	GPIO[3]
-	-	-	-	-	1	-	-	-	LCD_FIELD
-	-	-	-	1	-	-	-	C_FIELD	-
-	-	-	1	-	-	-	PWM1	-	-
-	-	1	-	-	-	PWM2	-	-	-
0	1	0	0	0	0	B2	R2	GPIO[4]	GPIO[3]
1	-	0	0	0	0	B2	R2	R0	B0

Table 3-23. VPBE (RGB666, RGB888, and LCD) and GPIO Pin Multiplexing

PINMUX0 AND PINMUX1 REGISTER BIT FIELDS					MULTIPLEXED PINS			
RGB888	PWM2	PWM1	CFLDEN	LFLDEN	R1/ GPIO[38]	B1/ GPIO[6]	G1/ GPIO[5]	G0/ GPIO[2]
0	0	0	0	0	GPIO[38]	GPIO[6]	GPIO[5]	GPIO[2]
1	0	0	0	0	R1	B1	G1	G0

3.6.6.4 ATA, EMIFA, UART1, SPI, and GPIO Pin Multiplexing

The ATA peripheral shares pins with the EMIFA and UART1 as seen in Table 3-24. If ATA pin functionality is enabled by setting the ATAEN bit field, the ATA module will drive the EMIFA data and control pins. Enabling UART1 disables the use of the ATA DMARQ and DMACK signals and thus only allows the ATA module to use PIO mode. The ATA HDDIR buffer direction control bit field works in conjunction with the HDIREN enable bit field to allow the ATA pins to still be used as a GPIO or SPI_EN1 if the buffer is not being used (i.e. for Compact Flash). This multiplexing is shown in Table 3-25. When ATAEN=0 and HDIREN=1 it indicates that the ATA interface has been disabled so that the EMIFA can be used, but the ATA buffers are still present. HDDIR is driven low in this situation to ensure that the ATA buffers drive away from DM644X and don't cause bus contention with the EMIFA. Note that switching between EMIFA and ATA (clearing or setting ATAEN) must be carefully performed to prevent bus contention. Since the ATA device can be a bus master, software must ensure that all outstanding DMA requests have completed before clearing the ATAEN bit.

Table 3-24. ATA, EMIFA, and GPIO Pin Multiplexing Control

PINMUX0 REGISTER BIT FIELD	MULTIPLEXED PINS									
ATAEN	GPIO[50]/ ATA_CS0	GPIO[51]/ ATA_CS1	EM_R/W INTRQ	EM_BA[0]/ ATA0	RDY/BSY/ EM_WAIT	DIOR/ EM_OE	DIOW/ EM_WE	EM_BA[1]/ GPIO[52]/ ATA1	EM_A[0]/ GPIO[53]/ ATA2	EM_D[15:0]/ DD[15:0]
0	GPIO[50]	GPIO[51]	EM_R/W	EM_BA[0]	RDY/BSY	EM_OE	EM_WE	EM_BA[1]/ GPIO[52] (1)	EM_A[0]/ GPIO[53] (1)	EM_D[15:0]
1	ATA_CS0	ATA_CS1	INTRQ	ATA0	EM_WAIT	DIOR	DIOW	ATA1	ATA2	DD[15:0]

(1) This pin shares GPIO functionality set by AEAW[4:0] as shown in Table 3-12.

Table 3-25. ATA, EMIFA, UART1, SPI, and GPIO Pin Multiplexing

PINMUX0 AND PINMUX1 REGISTER BIT FIELDS				MULTIPLEXED PINS		
ATAEN	UART1	HDIREN	SPI	UART_TXD1/ DMACK	UART_RXD1/ DMARQ	SPI_EN1/ HDDIR/ GPIO[42]
0	0	0	0	DMACK	DMARQ	GPIO[42]
0	0	0	1	DMACK	DMARQ	SPI_EN1
0	0	1	-	DMACK	DMARQ	Driven Low
0	1	0	0	UART_TXD1	UART_RXD1	GPIO[42]
0	1	0	1	UART_TXD1	UART_RXD1	SPI_EN1
0	1	1	-	UART_TXD1	UART_RXD1	Driven Low
1	0	0	0	DMACK	DMARQ	GPIO[42]x
1	0	0	1	DMACK	DMARQ	SPI_EN1x
1	0	1	-	DMACK	DMARQ	HDDIR
1	1	0	0	UART_TXD1	UART_RXD1	GPIO[42]x
1	1	0	1	UART_TXD1	UART_RXD1	SPI_EN1x
1	1	1	-	UART_TXD1	UART_RXD1	HDDIR

3.6.6.5 VLYNQ, EMIFA, and GPIO Pin Multiplexing

Table 3-26 and Table 3-27 show the VLYNQ pin control and multiplexing. If VLYNQ is disabled (VLYNQEN=0), the AECS5 and AECS4 bits select between the GPIO[8] / EMIFA EM_CS5 and GPIO[9] / EMIFA EM_CS4 functions, and the AEAW field determines the partitioning between GPIO and the upper EMIFA address pins. If VLYNQ is enabled (VLYNQEN=1), VLYNQ_CLOCK, VLYNQ_TXD0, and VLYNQ_RXD0 are always selected. The VLYNQ_SCRUN function is only enabled if VLYNQEN=1 and VLSCREN=1 (VLSCREN overrides AECS4). The remaining VLYNQ TX/RX pins are selected based on the VLYNQWD value. Unselected VLYNQ TX/RX pins will function as either GPIO or EMIFA address based on the AEAW value.

Table 3-26. VLYNQ Control, EMIFA, and GPIO Pin Multiplexing

PINMUX0 REGISTER BIT FIELDS				MULTIPLEXED PINS	
VLYNQEN	VLSCREN	AECS5	AECS4	EM_CS5/ GPIO[8]/ VLYNQ_CLOCK	EM_CS4/ GPIO[9]/ VLYNQ_SCRUN
0	-	0	0	GPIO[8]	GPIO[9]
0	-	0	1	GPIO[8]	EM_CS4
0	-	1	0	EM_CS5	GPIO[9]
0	-	1	1	EM_CS5	EM_CS4
1	0	-	0	VLYNQ_CLOCK	GPIO[9]
1	0	-	1	VLYNQ_CLOCK	EM_CS4
1	1	-	-	VLYNQ_CLOCK	VLYNQ_SCRUN

Table 3-27. VLYNQ Data, EMIFA, and GPIO Pin Multiplexing

PINMUX0 REGISTER BIT FIELDS		MULTIPLEXED PINS							
VLYNQEN	VLYNQWD	EM_A[21]/ GPIO[10]/ VL_TXD0	EM_A[20]/ GPIO[11]/ VL_RXD0	EM_A[19]/ GPIO[12]/ VL_TXD1	EM_A[18]/ GPIO[13]/ VL_RXD1	EM_A[17]/ GPIO[14]/ VL_TXD2	EM_A[16]/ GPIO[15]/ VL_RXD2	EM_A[15]/ GPIO[16]/ VL_TXD3	EM_A[14]/ GPIO[17]/ VL_RXD3
0	-	EM_A[21]/ GPIO[10][(1)]	EM_A[20]/ GPIO[11][(1)]	EM_A[19]/ GPIO[12][(1)]	EM_A[18]/ GPIO[13][(1)]	EM_A[17]/ GPIO[14][(1)]	EM_A[16]/ GPIO[15][(1)]	EM_A[15]/ GPIO[16][(1)]	EM_A[14]/ GPIO[17][(1)]
1	00	VL_TXD0	VLRXD0	EM_A[19]/ GPIO[12][(1)]	EM_A[18]/ GPIO[13][(1)]	EM_A[17]/ GPIO[14][(1)]	EM_A[16]/ GPIO[15][(1)]	EM_A[15]/ GPIO[16][(1)]	EM_A[14]/ GPIO[17][(1)]
1	01	VL_TXD0	VLRXD0	VL_TXD1	VLRXD1	EM_A[17]/ GPIO[14][(1)]	EM_A[16]/ GPIO[15][(1)]	EM_A[15]/ GPIO[16][(1)]	EM_A[14]/ GPIO[17][(1)]
1	10	VL_TXD0	VLRXD0	VL_TXD1	VLRXD1	VL_TXD2	VLRXD2	EM_A[15]/ GPIO[16][(1)]	EM_A[14]/ GPIO[17][(1)]
1	11	VL_TXD0	VLRXD0	VL_TXD1	VLRXD1	VL_TXD2	VLRXD2	VL_TXD3	VLRXD3

(1) This pin shares GPIO functionality set by AEAW[4:0] as shown in Table 3-12.

3.6.6.6 Timer0 Input, CLKOUT1, and GPIO Pin Multiplexing

The multiplexing of the CLKOUT1 and Timer0 Input (Timer 0 only) functions is shown in Table 3-28.

Table 3-28. Timer0 Input, CLKOUT1, and GPIO Pin Multiplexing

PINMUX1 REGISTER BIT FIELDS		MULTIPLEXED PINS
TIMIN	CLK1	CLKOUT1/ TIM_IN/ GPIO[49]
0	0	GPIO[49]
0	1	CLKOUT1
1	-	TIM_IN

3.6.6.7 ASP, SPI, I2C, ATA, and GPIO Pin Multiplexing

When the ASP, SPI, or I2C serial port functions are not selected, their pins may be used as GPIOs as seen in Table 3-29, Table 3-30, and Table 3-31. The SPI_EN1 pin can also function as the HDDIR buffer control when ATAEN is selected and the HDIREN bit is set.

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Table 3-29. ASP and GPIO Pin Multiplexing

PINMUX1 REGISTER BIT FIELD	MULTIPLEXED PINS					
ASP	**CLKX/ GPIO[29]**	**CLKR/ GPIO[30]**	**FSX/ GPIO[31]**	**FSR/ GPIO[32]**	**DX/ GPIO[33]**	**DR/ GPIO[34]**
0	GPIO[29]	GPIO[30]	GPIO[31]	GPIO[32]	GPIO[33]	GPIO[34]
1	CLKX	CLKR	FSX	FSR	DX	DR

Table 3-30. SPI and GPIO Pin Multiplexing

PINMUX0 AND PINMUX1 REGISTER BIT FIELDS			MULTIPLEXED PINS				
SPI	**ATAEN**	**HDIREN**	**SP_EN1/ HDDIR/ GPIO[42]**	**SPI_DO/ GPIO[41]**	**SPI_DI/ GPIO[40]**	**SPI_CLK/ GPIO[39]**	**SPI_EN0/ GPIO[37]**
0	0	0	GPIO[42]	GPIO[41]	GPIO[40]	GPIO[39]	GPIO[37]
0	0	1	Driven Low	GPIO[41]	GPIO[40]	GPIO[39]	GPIO[37]
0	1	0	GPIO[42]	GPIO[41]	GPIO[40]	GPIO[39]	GPIO[37]
0	1	1	HDDIR	GPIO[41]	GPIO[40]	GPIO[39]	GPIO[37]
1	0	0	SP_EN1	SPI_DO	SPI_DI	SPI_CLK	SPI_EN0
1	0	1	Driven Low	SPI_DO	SPI_DI	SPI_CLK	SPI_EN0
1	1	0	SP_EN1	SPI_DO	SPI_DI	SPI_CLK	SPI_EN0
1	1	1	HDDIR	SPI_DO	SPI_DI	SPI_CLK	SPI_EN0

Table 3-31. I2C and GPIO Pin Multiplexing

PINMUX1 REGISTER BIT FIELD	MULTIPLEXED PINS	
I2C	**I2C_CLK/ GPIO[43]**	**I2C_DATA/ GPIO[44]**
0	GPIO[43]	GPIO[44]
1	I2C_CLK	I2C_DATA

3.6.6.8 PWM, RGB888, and GPIO Pin Multiplexing

Table 3-32 shows the PWM0/1/2 pin multiplexing. Each PWM output is independently controlled by its own enable bit. The PWM function has priority over RGB888 muxing (see Section 3.6.6.3).

Table 3-32. PWM0/1/2, RGB888, and GPIO Pin Multiplexing

PINMUX1 REGISTER BIT FIELDS				MULTIPLEXED PINS		
PWM2	**PWM1**	**PWM0**	**RGB888**	**PWM2/ B2/ GPIO[47]**	**PWM1/ R2/ GPIO[46]**	**PWM0/ GPIO[45]**
0	0	0	0	GPIO[47]	GPIO[46]	GPIO[45]
0	0	0	1	B2	R2	GPIO[45]
-	-	1	-	-	-	PWM0
-	1	-	-	-	PWM1	-
1	-	-	-	PWM2	-	-

3.6.6.9 UART, VPFE, ATA, and GPIO Pin Multiplexing

Each UART has independent pin multiplexing control bits in the PINMUX1 register. The UART2 peripheral may be used with or without the flow control signals. Table 3-33 shows how UART2 selection reduces the width of the VPFE interface.

Setting the UART1 bit enables UART1 transmit and receive pin functionality. Since these are shared with the ATA DMA handshake signals, enabling UART1 effectively disables the ATA DMA mode. However, ATA PIO mode is still supported with UART1 enabled. This is shown in Table 3-34. If the ATA module is not enabled, the pins are always configured for use by UART1.

Table 3-33. UART2, VPFE, and GPIO Pin Multiplexing

PINMUX1 REGISTER BIT FIELDS		MULTIPLEXED PINS			
UART2	**U2FLO**	**CCD[15]/ CI[7]/ UART_RXD2**	**CCD[14]/ CI[6]/ UART_TXD2**	**CCD[13]/ CI[5]/ UART_CTS2**	**CCD[12]/ CI[4]/ UART_RTS2**
0	-	CCD[15]/ CI[7][(1)]	CCD[14]/ CI[6][(1)]	CCD[13]/ CI[5][(1)]	CCD[12]/ CI[4][(1)]
1	0	UART_RXD2	UART_TXD2	CCD[13]/ CI[5][(1)]	CCD[12]/ CI[4][(1)]
1	1	UART_RXD2	UART_TXD2	UART_CTS2	UART_RTS2

(1) Functionality set by VPFE operating mode.

Table 3-34. UART1 and ATA Pin Multiplexing

PINMUX0 AND PINMUX1 REGISTER BIT FIELDS		MULTIPLEXED PINS	
ATAEN	**UART1**	**UART_TXD1/ DMACK**	**UART_RXD1/ DMARQ**
0	-	UART_TXD1	UART_RXD1
1	0	DMACK	DMARQ
1	1	UART_TXD1	UART_RXD1

As Table 3-35 shows, the UART0 pins are configurable for either UART0 transmit and receive data functions or for GPIO.

Table 3-35. UART0 and GPIO Pin Multiplexing

PINMUX1 REGISTER BIT FIELD	MULTIPLEXED PINS	
UART0	**UART_TXD0/ GPIO[36]**	**UART_RXD0/ GPIO[35]**
0	GPIO[36]	GPIO[35]
1	UART_TXD0	UART_RXD0

3.7 Emulation Control

The flexibility of the DM644x architecture allows either the ARM or DSP to control the various peripherals (setup registers, service interrupts, etc.). While this assignment is purely a matter of software convention, during an emulation halt it is necessary for the device to know which peripherals are associated with the halting processor so that only those modules receive the suspend signal. This allows peripherals associated with the other (unhalted) processor to continue normal operation. The SUSPSRC register indicates the emulation suspend source for those peripherals which support emulation suspend. The SUSPSRC register format is shown in Figure 3-10. Brief details on the peripherals which correspond to the register bits is given in Table 3-36. When the associated SUSPSRC bit is '0', the peripheral's emulation suspend signal is controlled by the ARM emulator and when set to '1' it is controlled by the DSP emulator.

Figure 3-10. Emulation Suspend Source Register (SUSPSRC)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VICP SRC	VICP EN	TIMR2 SRC	TIMR1 SRC	TIMR0 SRC	GPIO SRC	PWM2 SRC	PWM1 SRC	PWM0 SRC	SPI SRC	UART2 SRC	UART1 SRC	UART0 SRC	I2C SRC	ASP SRC	RSV
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV			RSV	RSV		USB SRC	RSV			EMAC SRC	RESERVED				
R-000			R/W-0	R-00		R/W-0	R-000			R/W-0	R-0 0000				

LEGEND: R = Read, W = Write, n = value at reset

Table 3-36. SUSPSRC Register Description

Name	Description
VICPSRC	Video Imaging Coprocessor emulation suspend source 0 = ARM emulation suspend 1 = DSP emulation suspend
VICPEN	Video Imaging Coprocessor emulation suspend enable 0 = Emulation suspend ignored by VICP 1 = VICP emulation suspend enabled
TIMR2SRC	Timer2 (WD Timer) emulation suspend source 0 = ARM emulation suspend 1 = DSP emulation suspend
TIMR1SRC	Timer1 emulation suspend source 0 = ARM emulation suspend 1 = DSP emulation suspend
TIMR0SRC	Timer0 emulation suspend source 0 = ARM emulation suspend 1 = DSP emulation suspend
GPIOSRC	GPIO emulation suspend source 0 = ARM emulation suspend 1 = DSP emulation suspend
PWM2SRC	PWM2 emulation suspend source 0 = ARM emulation suspend 1 = DSP emulation suspend
PWM1SRC	PWM1 emulation suspend source 0 = ARM emulation suspend 1 = DSP emulation suspend
PWM0 SRC	PWM0 emulation suspend source 0 = ARM emulation suspend 1 = DSP emulation suspend
SPISRC	SPI emulation suspend source 0 = ARM emulation suspend 1 = DSP emulation suspend
UART2SRC	UART2 emulation suspend source 0 = ARM emulation suspend 1 = DSP emulation suspend
UART1SRC	UART1 emulation suspend source 0 = ARM emulation suspend 1 = DSP emulation suspend
UART0SRC	UART0 emulation suspend source 0 = ARM emulation suspend 1 = DSP emulation suspend
I2CSRC	I2C emulation suspend source 0 = ARM emulation suspend 1 = DSP emulation suspend

Table 3-36. SUSPSRC Register Description (continued)

Name	Description
ASPSRC	ASP emulation suspend source 0 = ARM emulation suspend 1 = DSP emulation suspend
USBSRC	USB emulation suspend source 0 = ARM emulation suspend 1 = DSP emulation suspend
EMACSRC	Ethernet MAC emulation suspend source 0 = ARM emulation suspend 1 = DSP emulation suspend

3.8 Debugging Considerations

TBD external connections, internal pullup/pulldown resistors

For the internal pullup/pulldown resistors for all device pins, see the terminal functions table.

3.9 Configuration Examples

TBD

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4 Device Operating Conditions

4.1 Absolute Maximum Ratings Over Operating Case Temperature Range (Unless Otherwise Noted) [(1)]

Supply voltage ranges	Core (CV_{DD}, APLLREFV, V_{DDA_1P1V}, USB_$V_{DDA1P2LDO}$ [(2)], CV_{DDDSP}) [(3)]	-0.3 V to 1.8 V
	I/O, 3.3V (DV_{DD33}, USB_DV_{DDA_3P3}) [(3)]	-0.3 V to 4 V
	I/O, 1.8V (DV_{DD18}, DV_{DDR2}, DDR_V_{DDDLL}, $PLLV_{DD18}$, V_{DDA_1P8V}, USB_V_{DD1P8}, MXV_{DD}, $M24V_{DD}$) [(3)]	-0.3 V to 2.4 V
Input voltage ranges	V_I I/O, 3.3V	-0.3 V to 4 V
	V_I I/O, 1.8V	-0.3 V to 2.4 V
Output voltage ranges	V_O I/O, 3.3V	-0.3 V to 4 V
	V_O I/O, 1.8V	-0.3 V to 2.4 V
Operating case temperature ranges, T_C	(default)	0°C to 85°C
Storage temperature range, T_{stg}	(default)	-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This pin is an internal LDO output and connected via 1 µF capacitor to USB_$V_{SSA1P2LDO}$.
(3) All voltage values are with respect to V_{SS}.

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4.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
CV_{DD}	Supply voltage, Core (CV_{DD}, APLLREFV, V_{DDA_1P1V}, USB_$V_{DDA1P2LDO}$ (1), CV_{DDDSP}) (-594 devices) (2)		1.14	1.2	1.26	V
DV_{DD}	Supply voltage, I/O, 3.3V (DV_{DD33}, USB_DV_{DDA3P3})		3.14	3.3	3.46	V
	Supply voltage, I/O, 1.8V (DV_{DD18}, DV_{DDR2}, DDR_V_{DDDLL}, $PLLV_{DD18}$, V_{DDA_1P8V}, USB_V_{DD1P8}, MXV_{DD}, $M24V_{DD}$)		1.71	1.8	1.89	V
V_{SS}	Supply ground (V_{SS}, V_{SSA_1P8V}, V_{SSA_1P1V}, DDR_V_{SSDLL}, USB_V_{SSREF}, USB_V_{SS1P8}, USB_V_{SSA3P3}, USB_$V_{SSA1P2LDO}$, MXV_{SS} (3), $M24V_{SS}$ (3))		0	0	0	V
DDR_VREF	DDR2 reference voltage (4)		$0.49DV_{DDR2}$	$0.5DV_{DDR2}$	$0.51DV_{DDR2}$	V
DDR_ZP	DDR2 impedance control, connected via 200 Ω resistor to V_{SS}			V_{SS}		V
DDR_ZN	DDR2 impedance control, connected via 200 Ω resistor to DV_{DDR2}			DV_{DDR2}		V
DAC_VREF	DAC reference voltage input			0.5		V
DAC_RBIAS	DAC biasing, connected via 4 kΩ resistor to V_{SSA_1P8V}			V_{SSA_1P8V}		V
USB_VBUS	USB external charge pump input			5		V
USB_R1	USB reference current output, connected via 10 kΩ +/- 1% resistor to USB_V_{SSREF}			USB_V_{SSREF}		
V_{IH}	High-level input voltage, I/O, 3.3V		2			V
	High-level input voltage, non-DDR I/O, 1.8V		$0.65DV_{DD}$			V
	High-level input voltage, DDR I/O, 1.8V		DDR_VREF + 0.25			V
V_{IL}	Low-level input voltage, I/O, 3.3V				0.8	V
	Low-level input voltage, non-DDR I/O, 1.8V				$0.35DV_{DD}$	V
	Low-level input voltage, DDR I/O, 1.8V				DDR_VREF - 0.25	V
T_C	Operating case temperature	Default	0		85	°C

(1) This pin is an internal LDO output and connected via 1 µF capacitor to USB_$V_{SSA1P2LDO}$.
(2) Future variants of TI SOC devices may operate at voltages ranging from 0.9 V to 1.4 V to provide a range of system power/performance options. TI highly recommends that users design-in a supply that can handle multiple voltages within this range (i.e., 1.0 V, 1.05 V, 1.1 V, 1.14 V, 1.2, 1.26 V with ± 3% tolerances) by implementing simple board changes such as reference resistor values or input pin configuration modifications. Not incorporating a flexible supply may limit the system's ability to easily adapt to future versions of TI SOC devices.
(3) Oscillator ground must be kept separate from other grounds and connected directly to the crystal load capacitor ground.
(4) DDR_VREF is expected to equal $0.5DV_{DDR2}$ of the transmitting device and to track variations in the DV_{DDR2}.

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4.3 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Case Temperature (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage (3.3V I/O)	DV_{DD33} = MIN, I_{OH} = MAX	DV_{DD} - 0.2			V
	High-level output voltage (1.8V I/O)	DV_{DD18} = MIN, I_{OH} = MAX	DV_{DD} - 0.45			V
	High-level output voltage (1.8V I/O DDR2)	DV_{DDR} = MIN, I_{OH} = MAX	DDR_VREF + 0.643			V
V_{OL}	Low-level output voltage (3.3V I/O)	DV_{DD33} = MIN, I_{OL} = MAX			0.2	V
	Low-level output voltage (1.8V I/O)	DV_{DD18} = MIN, I_{OL} = MAX			0.45	V
	Low-level output voltage (1.8V I/O DDR2)	DV_{DDR} = MIN, I_{OL} = MAX			DDR_VREF - 0.643	V
I_I	Input current	$V_I = V_{SS}$ to DV_{DD} without opposing internal resistor			1	µA
		$V_I = V_{SS}$ to DV_{DD} with opposing internal pullup resistor (2)			TBD	µA
		$V_I = V_{SS}$ to DV_{DD} with opposing internal pulldown resistor (2)			TBD	µA
I_{OH}	High-level output current	VCLK, GPIO[48]/CLK_OUT0, GPIO[8]/EM_CS5/VLYNQ_CLK, EM_A[21:14]/VLYNQ_(TX/RX)D[3:0]			8	mA
		DDR2			-13.4	mA
		All other peripherals			4	mA
I_{OL}	Low-level output current	VCLK, GPIO[48]/CLK_OUT0, GPIO[8]/EM_CS5/VLYNQ_CLK, EM_A[21:14]/VLYNQ_(TX/RX)D[3:0]			8	mA
		DDR2			13.4	mA
		All other peripherals			4	mA
I_{OZ}	I/O Off-state output current	$V_O = DV_{DD}$ or V_{SS}			±20	µA
I_{CDD}	Core (CV_{DD}, APLLREFV, V_{DDA_1P1V}, $V_{DDA1P2LDO}$ (3), CV_{DDDSP}) supply current (4)	CV_{DD} = 1.2 V, DSP clock = 594 MHz		TBD		mA
I_{DDD}	3.3V I/O (DV_{DD33}, USB_DV_{DDA3P3}) supply current (4)	DV_{DD} = 3.3 V, DSP clock = 594 MHz		TBD		mA
I_{DDD}	1.8V I/O (DV_{DD18}, DV_{DDR2}, DDR_V_{DDDLL}, $PLLV_{DD18}$, V_{DDA_1P8V}, USB_V_{DD1P8}, MXVDD, M24VDD) supply current (4)	DV_{DD} = 1.8 V, DSP clock = 594 MHz		TBD		mA
C_i	Input capacitance				10	pF
C_o	Output capacitance				10	pF

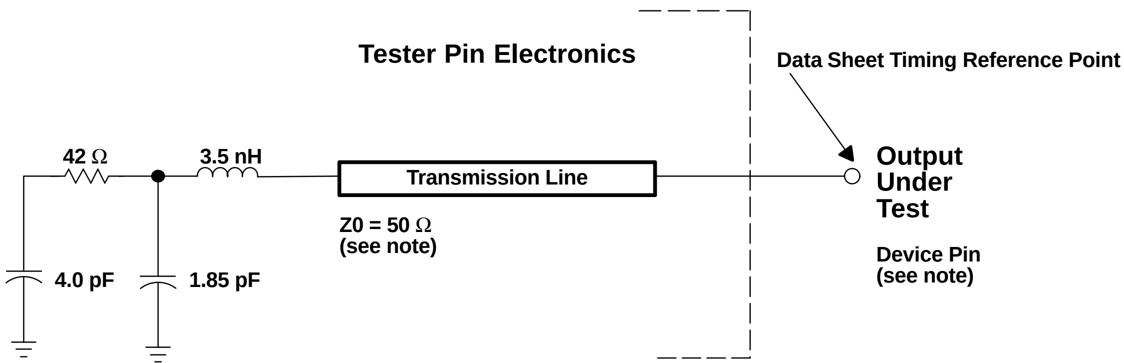
(1) For test conditions shown as MIN, MAX, or NOM, use the appropriate value specified in the recommended operating conditions table.
(2) Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor.
(3) This pin is an internal LDO output and connected via 1 µF capacitor to USB_$V_{SSA1P2LDO}$.
(4) Measured with average activity (50% high/50% low power) at 25°C case temperature and TBD-MHz EMIFA for -594 speed. This model represents a device performing high-MPU/DSP-activity operations 50% of the time, and the remainder performing low-MPU/DSP-activity operations. The high/low-MPU/DSP-activity models are defined as follows:
- High-MPU/DSP-Activity Model:
  - MPU: TBD
  - DSP: TBD
- Low-MPU/DSP-Activity Model:
  - MPU: TBD
  - DSP: TBD

The actual current draw is highly application-dependent. For more details on core and I/O activity, see the *DM644xPower Consumption Summary* application report (literature number SPRATBD).

5 Peripheral and Electrical Specifications

5.1 Parameter Information

5.1.1 Parameter Information Device-Specific Information



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 5-1. Test Load Circuit for AC Timing Measurements

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

5.1.1.1 Signal Transition Levels

All input and output timing parameters are referenced to V_{ref} for both "0" and "1" logic levels. For 3.3 V I/O, V_{ref} = 1.5 V. For 1.8 V I/O, V_{ref} = 0.9 V.

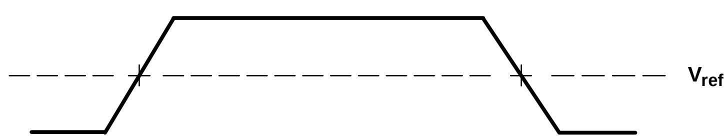


Figure 5-2. Input and Output Voltage Reference Levels for AC Timing Measurements

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL}MAX and V_{OH} MIN for output clocks.

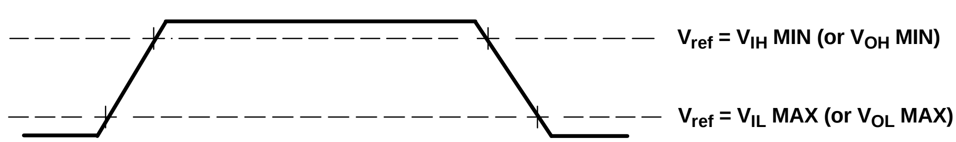


Figure 5-3. Rise and Fall Transition Time Voltage Reference Levels

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5.1.1.2 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data sheet do *not* include delays by board routings. As a good board design practice, such delays must *always* be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends utilizing the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number SPRA839). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

5.2 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals should transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

5.3 Power Supplies

For more information regarding TI's power management products and suggested devices to power TI DSPs, visit www.ti.com/dsppower.

5.3.1 Power-Supply Sequencing

Note: This power sequencing information is preliminary and subject to change.

Currently, DM6446 devices do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to ensure that neither supply is powered up for extended periods of time(>1 second) if the other supply is below the proper operating voltage.

5.3.1.1 Power-Supply Design Considerations

Core and I/O supply voltage regulators should be located close to the DSP (or DSP array) to minimize inductance and resistance in the power delivery path. Additionally, when designing for high-performance applications utilizing the DM6446 device, the PC board should include separate power planes for core, I/O, and ground, all bypassed with high-quality low-ESL/ESR capacitors.

5.3.1.2 Power-Supply Decoupling

In order to properly decouple the supply planes from system noise, place as many capacitors (caps) as possible close to DM6446. Assuming 0603 caps, the user should be able to fit a total of 60 caps, 30 for the core supplies and 30 for the I/O supplies. These caps need to be close to the DM6446 power pins, no more than 1.25 cm maximum distance to be effective. Physically smaller caps, such as 0402, are better because of their lower parasitic inductance. Proper capacitance values are also important. Small bypass caps (near 560 pF) should be closest to the power pins. Medium bypass caps (220 nF or as large as can be obtained in a small package) should be next closest. TI recommends no less than 8 small and 8 medium caps per supply be placed immediately next to the BGA vias, using the "interior" BGA space and at least the corners of the "exterior".

Larger caps for each supply can be placed further away for bulk decoupling. Large bulk caps (on the order of 100 μF) should be furthest away, but still as close as possible. Large caps for each supply should be placed outside of the BGA footprint.

Any cap selection needs to be evaluated from a yield/manufacturing point-of-view. As with the selection of any component, verification of capacitor availability over the product’s production lifetime should be considered.

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5.3.1.3 DM6446 Power and Clock Domains

DM6446 includes two separate power domains: "Always On" and "DSP". The "Always On" power domain is always on when the chip is on. The "Always On" domain is powered by the V_{DD} pins of the DM6446. The majority of the DM6446's modules lie within the "Always On" power domain. A separate domain called the "DSP" domain houses the C64x+ and VICP. The "DSP" domain is not always on. The "DSP" power domain is powered by the CV_{DDDSP} pins of the DM6446. Table 5-1 provides a listing of the DM6446 power and clock domains.

Two primary reference clocks are required for the DM6446 device. These can either be crystal input or driven by external oscillators. A 27-MHz crystal is recommended for the system PLLs, which generate the internal clocks for the ARM, DSP, coprocessors, peripherals (including imaging peripherals), and EDMA3. The recommended 27-MHz input enables the use of the video DACs to drive NTSC/PAL television signals at the proper frequencies. A 24-MHz crystal is also required if the USB peripheral is to be used. For further description of the DM6446 clock domains, see Table 5-2 and Figure 5-4.

Table 5-1. DM6446 Power and Clock Domains

Power Domain	Clock Domain	Peripheral/Module
Always On	CLKIN	UART0
Always On	CLKIN	UART1
Always On	CLKIN	UART2
Always On	CLKIN	I2C
Always On	CLKIN	Timer0
Always On	CLKIN	Timer1
Always On	CLKIN	Timer2
Always On	CLKIN	PWM0
Always On	CLKIN	PWM1
Always On	CLKIN	PWM2
Always On	CLKDIV2	ARM Subsystem
Always On	CLKDIV3	DDR2
Always On	CLKDIV3	VPSS
Always On	CLKDIV3	EDMA
Always On	CLKDIV3	SCR
Always On	CLKDIV6	GPSC
Always On	CLKDIV6	LPSCs
Always On	CLKDIV6	Ice Pick
Always On	CLKDIV6	EMIFA
Always On	CLKDIV6	USB
Always On	CLKDIV6	VLYNQ
Always On	CLKDIV6	EMAC
Always On	CLKDIV6	ATA/CF
Always On	CLKDIV6	MMC/SD
Always On	CLKDIV6	SPI
Always On	CLKDIV6	ASP
Always On	CLKDIV6	GPIO
DSP	CLKDIV1	C64x+ CPU
DSP	CLKDIV2	VICP
DSP	CLKDIV4	VICP
DSP	CLKDIV6	VICP

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Table 5-2. DM6446 Clock Domains(1)

Subsystem	Fixed Ratio vs. PLL1	Clock Modes (Frequency)	
		PLL Bypass	PLL Enabled
PLL1	–	27 MHz	594 MHz
DSP	1:1	27 MHz	594 MHz
ARM	1:2	13.5 MHz	297 MHz
IMX/LCD	1:2	13.5 MHz	297 MHz
Sequencer	1:4	6.75 MHz	148.5 MHz
EDMA3/VPSS	1:3	9 MHz	198 MHz
Peripherals	1:6	4.5 MHz	99 MHz

(1) These table values assume a MXI/CLKIN of 27 MHz and a PLL1 multiplier equal to 22.

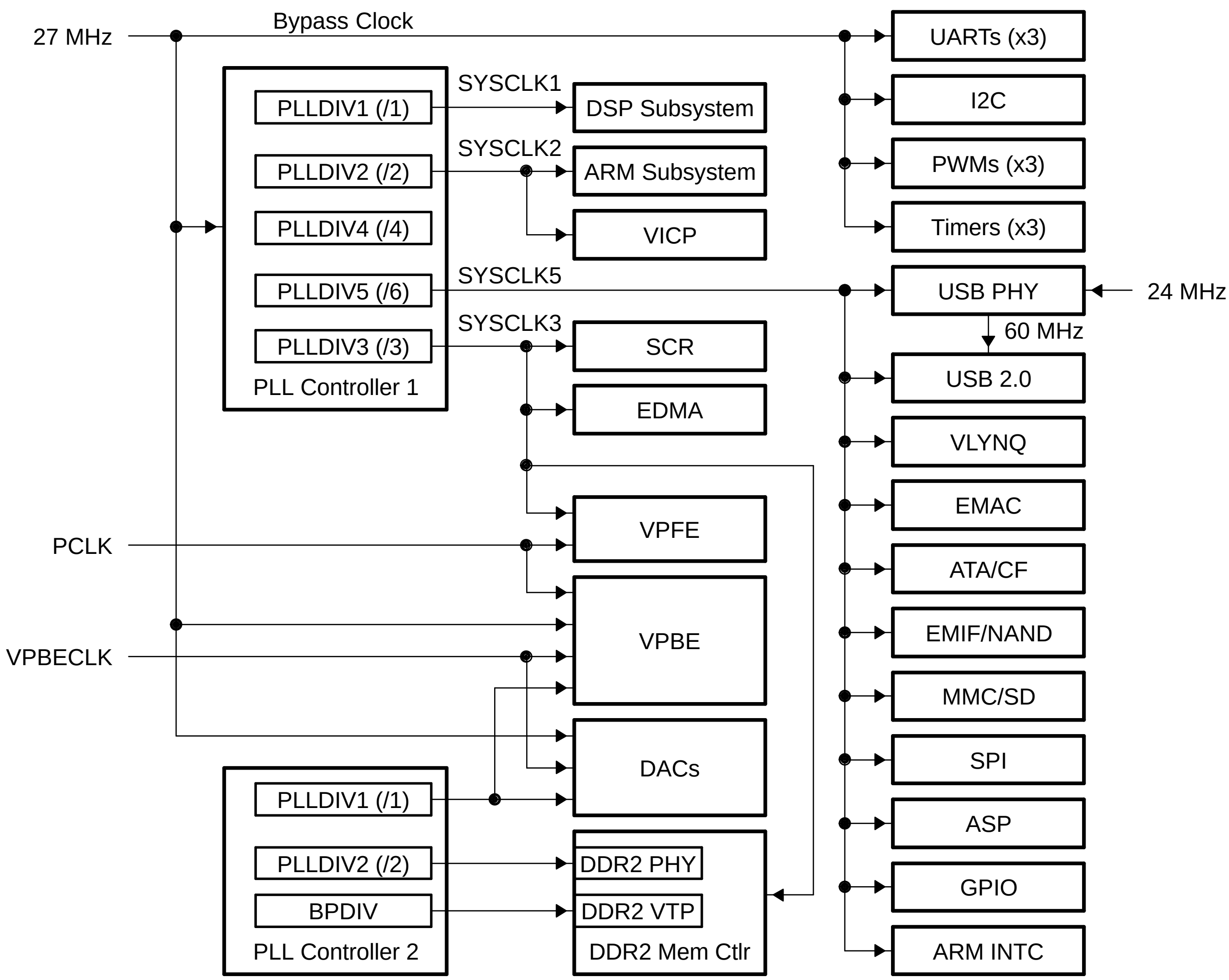

Figure 5-4. PLL1 and PLL2 Clock Domain Block Diagram

For further detail on PLL1 and PLL2, see the structure block diagrams Figure 5-5 and Figure 5-6, respectively.

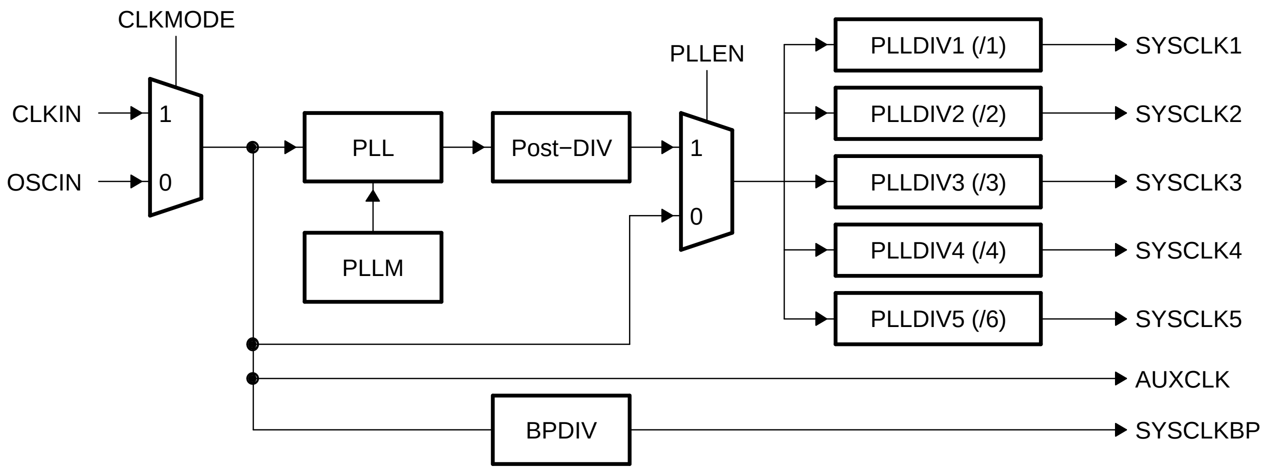

Figure 5-5. PLL1 Structure Block Diagram

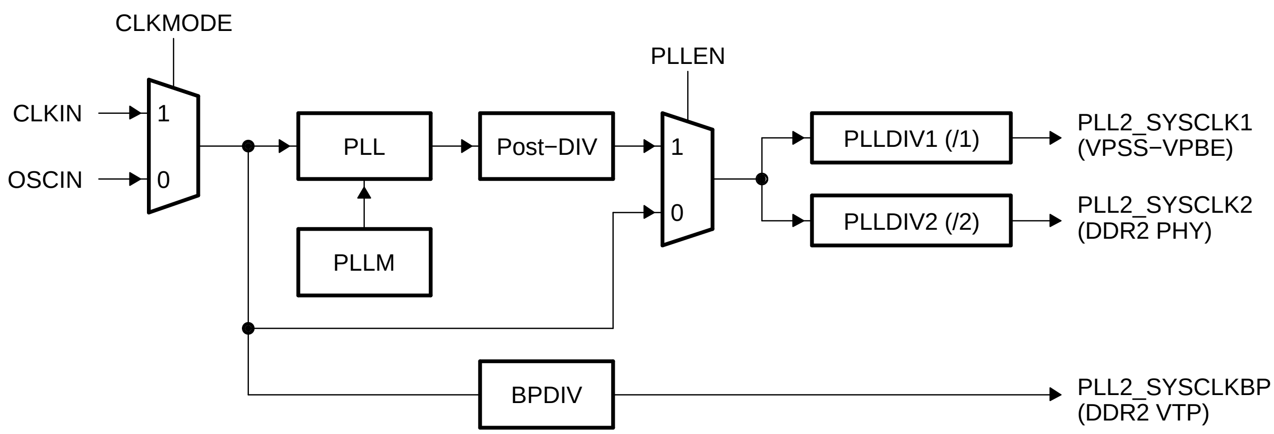

Figure 5-6. PLL2 Structure Block Diagram

5.3.1.4 Power and Sleep Controller (PSC)

The Power and Sleep Controller (PSC) controls DM6446 device power by turning off unused power domains or gating off clocks to individual peripherals/modules. The PSC consists of a Global PSC (GPSC) and a set of Local PSCs (LPSCs). The GPSC contains memory mapped registers, power domain control, PSC interrupt control, and a state machine for each peripheral/module. An LPSC is associated with each peripheral/module and provides clock and reset control. The GPSC controls all of DM6446's LPSCs. The ARM Subsystem does not have an LPSC module. ARM sleep mode is accomplished through the wait for interrupt instruction. The LPSCs for DM6446 are shown in Table 5-3. The PSC Register memory map is given in Table 5-4. For more details on the PSC, see the *Documentation Support* section for the ARM Subsystem User's Guide.

Table 5-3. DM6446 LPSC Assignments

LPSC Number	Peripheral/Module	LPSC Number	Peripheral/Module	LPSC Number	Peripheral/Module
0	VPSS DMA	14	EMIFA	28	TIMER1
1	VPSS MMR	15	MMC/SD	29	Reserved
2	EDMACC	16	Reserved	30	Reserved
3	EDMATC0	17	ASP	31	Reserved
4	EDMATC1	18	I2C	32	Reserved

Table 5-3. DM6446 LPSC Assignments (continued)

LPSC Number	Peripheral/Module	LPSC Number	Peripheral/Module	LPSC Number	Peripheral/Module
5	EMAC	19	UART0	33	Reserved
6	EMAC Memory Controller	20	UART1	34	Reserved
7	MDIO	21	UART2	35	Reserved
8	Reserved	22	SPI	36	Reserved
9	USB	23	PWM0	37	Reserved
10	ATA/CF	24	PWM1	38	Reserved
11	VLYNQ	25	PWM2	39	C64x+ CPU
12	Reserved	26	GPIO	40	VICP
13	DDR2 Memory Controller	27	TIMER0		

Table 5-4. PSC Register Memory Map

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x01C4 1000	PID	Peripheral Revision and Class Information Register
0x01C4 1003 - 0x01C4 101F	-	Reserved
0x01C4 1010	GBLCTL	Global Control Register
0x01C4 1014	-	Reserved
0x01C4 1018	INTEVAL	Interrupt Evaluation Register
0x01C4 101C - 0x01C4 103F	-	Reserved
0x01C4 1040	MERRPR0	Module Error Pending 0 (mod 0 - 31) Register
0x01C4 1044	MERRPR1	Module Error Pending 1 (mod 32- 63) Register
0x01C4 1048 - 0x01C4 104F	-	Reserved
0x01C4 1050	MERRCR0	Module Error Clear 0 (mod 0 - 31) Register
0x01C4 1054	MERRCR1	Module Error Clear 1 (mod 32 - 63) Register
0x01C4 1058 - 0x01C4 105F	-	Reserved
0x01C4 1060	PERRPR	Power Error Pending Register
0x01C4 1064 - 0x01C4 1067	-	Reserved
0x01C4 1068	PERRCR	Power Error Clear Register
0x01C4 106C - 0x01C4 106F	-	Reserved
0x01C4 1070	EPCPR	External Power Error Pending Register
0x01C4 1074 - 0x01C4 1077	-	Reserved
0x01C4 1078	EPCCR	External Power Control Clear Register
0x01C4 107C - 0x01C4 10FF	-	Reserved
0x01C4 1100	RAILSTAT	Power Rail Status Register
0x01C4 1104	RAILCTL	Power Rail Control Register
0x01C4 1108	RAILSEL	Power Rail Counter Select Register
0x01C4 110C - 0x01C4 111F	-	Reserved
0x01C4 1120	PTCMD	Power Domain Transition Command Register
0x01C4 1124 - 0x01C4 1127	-	Reserved
0x01C4 1128	PTSTAT	Power Domain Transition Status Register
0x01C4 112C - 0x01C4 11FF	-	Reserved
0x01C4 1200	PDSTAT0	Power Domain Status 0 Register (Always On)
0x01C4 1204	PDSTAT1	Power Domain Status 1 Register (DSP)
0x01C4 1208 - 0x01C4 12FF	-	Reserved
0x01C4 1300	PDCTL0	Power Domain Control 0 Register (Always On)

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PSC Register Memory Map (continued)

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x01C4 1304	PDCTL1	Power Domain Control 1 Register (DSP)
0x01C4 1308 - 0x01C4 14FF	-	Reserved
0x01C4 1500		Reserved
0x01C4 1504		Reserved
0x01C4 1508 0x1C4 150F	-	Reserved
0x01C4 1510	MCKOUT0	Module Clock Output Status (mod 0-31) Register
0x01C4 1514	MCKOUT1	Module Clock Output Status (mod 32-63) Register
0x01C4 1518 - 0x01C4 15FF	-	Reserved
0x01C4 1600	MDCFG0	Module Configuration 0 Register (VPSS DMA)
0x01C4 1604	MDCFG1	Module Configuration 1 Register (VPSS MMR)
0x01C4 1608	MDCFG2	Module Configuration 2 Register (EDMACC)
0x01C4 160C	MDCFG3	Module Configuration 3 Register (EDMATC0)
0x01C4 1610	MDCFG4	Module Configuration 4 Register (EDMATC1)
0x01C4 1614	MDCFG5	Module Configuration 5 Register (EMAC)
0x01C4 1618	MDCFG6	Module Configuration 6 Register (EMAC Memory Controller)
0x01C4 161C	MDCFG7	Module Configuration 7 Register (MDIO)
0x01C4 1620		Reserved
0x01C4 1624	MDCFG9	Module Configuration 9 Register (USB)
0x01C4 1628	MDCFG10	Module Configuration 10 Register (ATA/CF)
0x01C4 162C	MDCFG11	Module Configuration 11 Register (VLYNQ)
0x01C4 1630		Reserved
0x01C4 1634	MDCFG13	Module Configuration 13 Register (DDR2)
0x01C4 1638	MDCFG14	Module Configuration 14 Register (EMIFA)
0x01C4 163C	MDCFG15	Module Configuration 15 Register (MMC/SD)
0x01C4 1640		Reserved
0x01C4 1644	MDCFG17	Module Configuration 17 Register (ASP)
0x01C4 1648	MDCFG18	Module Configuration 18 Register (I2C)
0x01C4 164C	MDCFG19	Module Configuration 19 Register (UART0)
0x01C4 1650	MDCFG20	Module Configuration 20 Register (UART1)
0x01C4 1654	MDCFG21	Module Configuration 21 Register (UART2)
0x01C4 1658	MDCFG22	Module Configuration 22 Register (SPI)
0x01C4 165C	MDCFG23	Module Configuration 23 Register (PWM0)
0x01C4 1660	MDCFG24	Module Configuration 24 Register (PWM1)
0x01C4 1664	MDCFG25	Module Configuration 25 Register (PWM2)
0x01C4 1668	MDCFG26	Module Configuration 26 Register (GPIO)
0x01C4 166C	MDCFG27	Module Configuration 27 Register (TIMER0)
0x01C4 1670	MDCFG28	Module Configuration 28 Register (TIMER1)
0x01C4 1674 - 0x01C4 169B	-	Reserved
0x01C4 169C	MDCFG39	Module Configuration 39 Register (C64x+ CPU)
0x01C4 16A0	MDCFG40	Module Configuration 40 Register (VICP)
0x01C4 16A4 - 0x01C4 17FF	-	Reserved
0x01C4 1800	MDSTAT0	Module Status 0 Register (VPSS DMA)
0x01C4 1804	MDSTAT1	Module Status 1 Register (VPSS MMR)
0x01C4 1808	MDSTAT2	Module Status 2 Register (EDMACC)
0x01C4 180C	MDSTAT3	Module Status 3 Register (EDMATC0)
0x01C4 1810	MDSTAT4	Module Status 4 Register (EDMATC1)

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PSC Register Memory Map (continued)

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x01C4 1814	MDSTAT5	Module Status 5 Register (EMAC)
0x01C4 1818	MDSTAT6	Module Status 6 Register (EMAC Memory Controller)
0x01C4 181C	MDSTAT7	Module Status 7 Register (MDIO)
0x01C4 1820		Reserved
0x01C4 1824	MDSTAT9	Module Status 9 Register (USB)
0x01C4 1828	MDSTAT10	Module Status 10 Register (ATA/CF)
0x01C4 182C	MDSTAT11	Module Status 11 Register (VLYNQ)
0x01C4 1830		Reserved
0x01C4 1834	MDSTAT13	Module Status 13 Register (DDR2)
0x01C4 1838	MDSTAT14	Module Status 14 Register (EMIFA)
0x01C4 183C	MDSTAT15	Module Status 15 Register (MMC/SD)
0x01C4 1840		Reserved
0x01C4 1844	MDSTAT17	Module Status 17 Register (ASP)
0x01C4 1848	MDSTAT18	Module Status 18 Register (I2C)
0x01C4 184C	MDSTAT19	Module Status 19 Register (UART0)
0x01C4 1850	MDSTAT20	Module Status 20 Register (UART1)
0x01C4 1854	MDSTAT21	Module Status 21 Register (UART2)
0x01C4 1858	MDSTAT22	Module Status 22 Register (SPI)
0x01C4 185C	MDSTAT23	Module Status 23 Register (PWM0)
0x01C4 1860	MDSTAT24	Module Status 24 Register (PWM1)
0x01C4 1864	MDSTAT25	Module Status 25 Register (PWM2)
0x01C4 1868	MDSTAT26	Module Status 26 Register (GPIO)
0x01C4 186C	MDSTAT27	Module Status 27 Register (TIMER0)
0x01C4 1870	MDSTAT28	Module Status 28 Register (TIMER1)
0x01C4 1874 - 0x01C4 189B	-	Reserved
0x01C4 189C	MDSTAT39	Module Status 39 Register (C64x+ CPU)
0x01C4 18A0	MDSTAT40	Module Status 40 Register (VICP)
0x01C4 18A4 - 0x01C4 19FF	-	Reserved
0x01C4 1A00	MDCTL0	Module Control 0 Register (VPSS DMA)
0x01C4 1A04	MDCTL1	Module Control 1 Register (VPSS MMR)
0x01C4 1A08	MDCTL2	Module Control 2 Register (EDMACC)
0x01C4 1A0C	MDCTL3	Module Control 3 Register (EDMATC0)
0x01C4 1A10	MDCTL4	Module Control 4 Register (EDMATC1)
0x01C4 1A14	MDCTL5	Module Control 5 Register (EMAC)
0x01C4 1A18	MDCTL6	Module Control 6 Register (EMAC Memory Controller)
0x01C4 1A1C	MDCTL7	Module Control 7 Register (MDIO)
0x01C4 1A20		Reserved
0x01C4 1A24	MDCTL9	Module Control 9 Register (USB)
0x01C4 1A28	MDCTL10	Module Control 10 Register (ATA/CF)
0x01C4 1A2C	MDCTL11	Module Control 11 Register (VLYNQ)
0x01C4 1A30		Reserved
0x01C4 1A34	MDCTL13	Module Control 13 Register (DDR2)
0x01C4 1A38	MDCTL14	Module Control 14 Register (EMIFA)
0x01C4 1A3C	MDCTL15	Module Control 15 Register (MMC/SD)
0x01C4 1A40		Reserved
0x01C4 1A44	MDCTL17	Module Control 17 Register (ASP)

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PSC Register Memory Map (continued)

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x01C4 1A48	MDCTL18	Module Control 18 Register (I2C)
0x01C4 1A4C	MDCTL19	Module Control 19 Register (UART0)
0x01C4 1A50	MDCTL20	Module Control 20 Register (UART1)
0x01C4 1A54	MDCTL21	Module Control 21 Register (UART2)
0x01C4 1A58	MDCTL22	Module Control 22 Register (SPI)
0x01C4 1A5C	MDCTL23	Module Control 23 Register (PWM0)
0x01C4 1A60	MDCTL24	Module Control 24 Register (PWM1)
0x01C4 1A64	MDCTL25	Module Control 25 Register (PWM2)
0x01C4 1A68	MDCTL26	Module Control 26 Register (GPIO)
0x01C4 1A6C	MDCTL27	Module Control 27 Register (TIMER0)
0x01C4 1A70	MDCTL28	Module Control 28 Register (TIMER1)
0x01C4 1A74 - 0x01C4 1A9B	-	Reserved
0x01C4 1A9C	MDCTL39	Module Control 39 Register (C64x+ CPU)
0x01C4 1AA0	MDCTL40	Module Control 40 Register (VICP)
0x01C4 1AA4 - 0x01C4 1FFF	-	Reserved
0x01C4 1000	MPFAR	Memory Protection Fault Address Register
0x01C4 1004	MPFSR	Memory Protection Fault Status Register
0x01C4 1008	MPFCR	Memory Protection Fault Command Register
0x01C4 100C	MPAA	Memory Protection Page Attribute Register
0x01C4 1010 - 0x01C4 1FFF	-	Reserved

5.3.1.5 Triggering, Wake-up, and Effects

Table 5-5 summarizes the DM6446 power-down modes, trigger, wake-up method, and effect on the DM6446. For more details, see the *Documentation Support* section for the ARM Subsystem User's Guide.

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Table 5-5. Characteristics of the Power-Down Modes

POWER-DOWN MODE	TRIGGER/ENTRY	WAKE-UP METHOD	EFFECT ON CHIP'S OPERATION
Standby	PSC, System Module, PLLC1/2, DDR2 Memory Controller, ARM Wait For Interrupt instruction	Interrupts	This mode consumes the lowest power, with the minimum set of modules kept alive that are required to wake up the chip to a higher power mode. DSP and coprocessor subsystems are not powered. The rest of the chip is powered and clocks are suspended, except for GPIO (interrupts), UARTs, I2C (in slave mode), and Ethernet MAC. PLLs are operating in bypass mode. 27-MHz clock is the only clock available to the system. DDR2 clock is suspended and DDR2 is put into self-refresh mode.
Low Power	PSC, System Module, PLLC1/2, DDR2 Memory Controller	Interrupts	This mode is for ARM to sustain some basic control functions. DSP and coprocessor subsystems are not powered. The rest of the chip is powered, but most clocks are suspended, except for ARM, GPIO, UARTs, SPI, I2C, PWMs, and Timers. PLLs are operating in bypass mode. 27-MHz clock is the only clock available to the system. ARM runs at 13.5 MHz, and handles all peripherals by direct access. DDR2 clock is suspended and DDR2 is put into self-refresh mode. ARM will not have access to DDR2 and its caches are either frozen or inaccessible.
Preview	PSC, System Module, PLLC1/2	Interrupts	This mode is for Digital Still Camera (DSC) preview. DSP and coprocessor subsystems are not powered. The rest of the chip is powered, and the PLLs are operating to support the activities needed for preview processing and data flow. ARM and DDR2 EMIF operate at nominal frequencies.
Active	PSC, System Module, PLLC1/2	N/A	The entire chip is powered. All modules operate at nominal clock frequency. Unused peripherals have their clocks suspended. Active peripherals have their clocks suspended when unneeded.

5.3.1.6 DM6446 Power-Down Mode with an Emulator

TBD

5.4 Reset

DM6446 supports various types of resets. Power-on-reset (POR), warm reset, max reset, system reset, C64x+ local reset, and module reset are summarized in Table 5-6.

Table 5-6. DM6446 Resets

Type	Initiator	Description
Power-on-reset (POR)	$\overline{\text{RESET}}$ pin active low while $\overline{\text{TRST}}$ is low.	Global chip reset (Cold reset). Activates the POR signal on chip, which is used to reset test and emulation logic.
Warm reset	$\overline{\text{RESET}}$ pin active low while $\overline{\text{TRST}}$ is high.	Resets everything except for test and emulation logic. ARM emulator stays alive during warm reset, but the C64x+ emulator does not.
Maximum reset	Emulator, WD Timer	Same as Warm reset, except for initiators.

Table 5-6. DM6446 Resets (continued)

Type	Initiator	Description
System reset	Software (register bit)	This is a soft reset that maintains memory contents and does not affect clocks or power states.
C64x+ Local reset	Software (register bit)	MMR controls the C64x+ reset input. This is used for control of C64x+ reset by the ARM. The C64x+ Slave DMA port is still alive when in local reset.

Power-on-reset (POR) is the global chip reset and it affects test, emulation, and other circuitry. It is invoked by driving the $\overline{\text{RESET}}$ pin active low while $\overline{\text{TRST}}$ is held low. A POR is required to place DM6446 into a known good initial state. POR can be asserted prior to ramping the core and I/O voltages or after the core and I/O voltages have reached their proper operating conditions. As a best practice, $\overline{\text{RESET}}$ should be asserted (held low) during power-up. Prior to deasserting $\overline{\text{RESET}}$ (low-to-high transition), the core and I/O voltages should be at their proper operating conditions and if an external 27 MHz oscillator is used on the MXI/CLKIN pin, the external clock should also be running at the correct frequency.

Warm reset is activated by driving the $\overline{\text{RESET}}$ pin active low, while $\overline{\text{TRST}}$ is inactive high. This does not reset test or ARM emulation logic. An ARM emulator session will stay alive during warm reset, but a C64x+ emulator session will not.

Maximum reset is initiated by the emulator or the watchdog timer and the reset effects are the same as a warm reset. The emulator initiates a maximum reset via the ICEPICK module. When the watchdog timer counter reaches zero, this will initiate a maximum reset to recover from a runaway condition. Both of the maximum reset initiators can be masked by the ARM emulator.

System reset is initiated by the emulator and is a soft reset. Memory contents are maintained. Test, emulation, clock, and power control logic are unaffected. The emulator initiates a system reset via the C64x+ emulation logic, or through ICECRUSHER. Both of these reset initiators are non-maskable resets.

The C64x+ DSP has an internal reset input that allows a host to control it. This reset is configured through a MMR bit (MDCTL[39].LRSTz) in the PSC module. When in C64x+ local reset, the slave DMA port on C64x+ will remain active and the internal memory will be accessible, including access to the VICP memory through the L2 port (UMAP port).

Refer to the ARM Subsystem User's Guide for details on reset control/status registers.

For information on peripheral selection at the rising edge of $\overline{\text{RESET}}$, see the Device Configuration section of this data manual.

5.4.1 Reset Electrical Data/Timing

Table 5-7. Timing Requirements for Reset (1)(2)(3) (see Figure 5-7)

NO.			-594 MIN	-594 MAX	UNIT
1	$t_{w(RESET)}$	Active low width of the $\overline{\text{RESET}}$ pulse	12C		ns
2	$t_{su(BOOT)}$	Setup time, boot configuration bits valid before $\overline{\text{RESET}}$ rising edge	1		µs
3	$t_{h(BOOT)}$	Hold time, boot configuration bits valid after $\overline{\text{RESET}}$ rising edge	1		µs

(1) For proper $\overline{\text{RESET}}$ operation, the RSV5 pin ***must*** be driven low or tied directly to V_{SS} at all times and the user ***must not*** switch values throughout device operation.
(2) BTSEL[1:0], DSP_BT, and AEAW[4:0] are the boot configuration pins during device reset.
(3) C = MXI/CLKIN cycle time in ns. For example, when MXI/CLKIN frequency is 27 MHz, use C = $37.\overline{037}$ ns.

Table 5-8. Switching Characteristics Over Recommended Operating Conditions During Reset (see Figure 5-7)

NO.	PARAMETER		-594		UNIT
			MIN	MAX	
4	$t_{d(PLL\_LOCK)}$	Delay time, $\overline{RESET}$ rising edge to PLL1 locked internally		500	µs

Figure 5-7. Reset Timing TBD

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5.5 Oscillators

DM6446 has two oscillator input/output pairs (MXI/MXO and M24XI/M24XO) usable with external crystals or ceramic resonators to provide clock inputs. The optimal frequencies for the crystals are 27 MHz (MXI/MXO) and 24 MHz (M24XI/M24XO). Optionally, the oscillator inputs are configurable for use with external oscillators.

5.5.1 27-MHz System Oscillator

The 27-MHz oscillator provides the reference clock for all DM6446 subsystems and peripherals, with the exception of USB. The on-chip oscillator requires an external 27-MHz crystal connected across the MXI and MXO pins, along with two load capacitors, as shown in Figure 5-8. The external crystal load capacitors ***must*** be connected only to the 27-MHz oscillator ground pin (MXV_{SS}). ***Do not*** connect to board ground (V_{SS}).

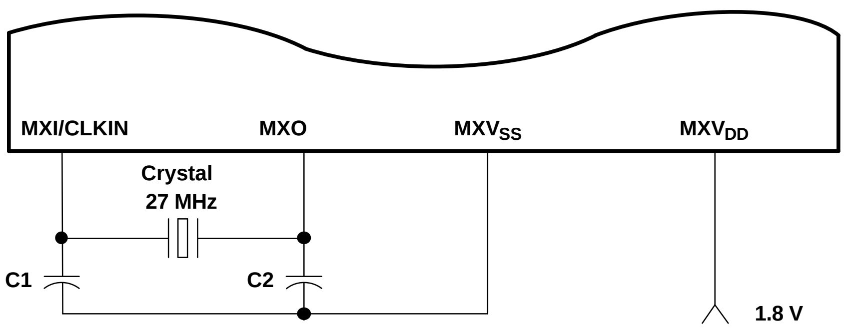

Figure 5-8. 27-MHz System Oscillator

The load capacitors, C1 and C2, should be chosen such that the equation is satisfied (typical values are C1 = C2 = 10 pF). CL in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator pins (MXI and MXO) and to the MXV_{SS} pin.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

Table 5-9. Switching Characteristics Over Recommended Operating Conditions for 27-MHz System Oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Start-up time (from power up until oscillating at stable frequency of 27 MHz)	C1 = C2 = TBD pF, CV_{DD} = TBD V		TBD	TBD	ms
	I_{DDA}, active current consumption			TBD		µA
	Oscillaton frequency			27		MHz

5.5.2 24-MHz USB Oscillator

The 24-MHz oscillator provides the reference clock for the DM6446 USB peripheral. The on-chip oscillator requires an external 24-MHz crystal connected across the M24XI and M24XO pins, along with two load capacitors, as shown in Figure 5-9.The external crystal load capacitors ***must*** be connected only to the 24-MHz oscillator ground pin ($M24V_{SS}$). ***Do not*** connect to board ground (V_{SS}).

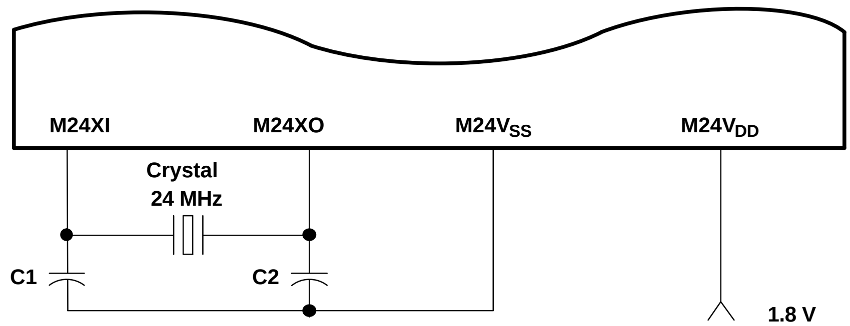

Figure 5-9. 24-MHz USB Oscillator

The load capacitors, C1 and C2, should be chosen such that the equation is satisfied (typical values are C1 = C2 = 10 pF). CL in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator pins (M24XI and M24XO) and to the M24XV$_{SS}$ pin.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

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Table 5-10. Switching Characteristics Over Recommended Operating Conditions for 24-MHz System Oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Start-up time (from power up until oscillating at stable frequency of 24 MHz)	C1 = C2 = TBD pF, CV_{DD} = TBD V		TBD	TBD	ms
	I_{DDA}, active current consumption			TBD		μA
	Oscillaton frequency			24		MHz

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5.6 Clock PLLs

There are two independently controlled PLLs on DM6446. PLL1 generates the frequencies required for the DSP, ARM, VICP, DMA, VPFE, and other peripherals. PLL2 generates the frequencies required for the DDR2 interface and the VPBE in certain modes. The recommended reference clock for both PLLs is the 27-MHz crystal input. The USB2.0 PHY contains a third PLL embedded within it and the 24-MHz oscillator is its reference clock source. This particular PLL is only usable for USB operation, and is discussed further in the TMS320DM6446 DMSoC Universal Serial Bus (USB) Controller User's Guide (see the *Documentation Support* section).

A summary of the PLL controller registers is shown in Table 5-11. Refer to the ARM Subsystem User's Guide for more details.

Table 5-11. PLL and Reset Controller Registers Memory Map

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
PLL1 Controller Registers		
0x01C4 0800	PID	Peripheral Identification and Revision Information Register
0x01C4 08E0	-	Reserved
0x01C4 08E4	RSTYPE	Reset Type Register
0x01C4 08E8 - 0x01C4 08FF	-	Reserved
0x01C4 0900	PLLCTL	PLL Controller 1 Operations Control Register
0x01C4 0908 - 0x01C4 090F	-	Reserved
0x01C4 0910	PLLM	PLL Controller 1 Multiplier Control Register
0x01C4 0914 - 0x01C4 0917	-	Reserved
0x01C4 0918	PLLDIV1	PLL Controller 1 Control-Divider 1 Register (SYSCLK1)
0x01C4 091C	PLLDIV2	PLL Controller 1 Control-Divider 2 Register (SYSCLK2)
0x01C4 0920	PLLDIV3	PLL Controller 1 Control-Divider 3 Register (SYSCLK3)
0x01C4 0928	POSTDIV	PLL Controller 1 Post-Divider Control Register
0x01C4 092C	BPDIV	PLL Controller 1 Bypass Control-Divider Register (SYSCLKBP)
0x01C4 0938	PLLCMD	PLL Controller 1 Command Register
0x01C4 093C	PLLSTAT	PLL Controller 1 Status Register (Shows PLLCTRL Status)
0x01C4 0940	ALNCTL	PLL Controller 1 Alignment Control Register (Indicates Which SYSCLKs Need to be Aligned for Proper Device Operation)
0x01C4 0944	DCHANGE	PLL Controller 1 Divider Change Register (Indicates if SYSCLK Divide Ratio has Been Modified)
0x01C4 0948	CKEN	PLL Controller 1 Clock Enable Register
0x01C4 094C	CKSTAT	PLL Controller 1 Clock Status Register (For All Clocks Except SYSCLKx)
0x01C4 0950	SYSTAT	PLL Controller 1 System Clock Status 1 Register (Indicates SYSCLK on/off Status)
0x01C4 0960	PLLDIV4	PLL Controller 1 Control-Divider 4 Register (SYSCLK4)
0x01C4 0964	PLLDIV5	PLL Controller 1 Control-Divider 5 Register (SYSCLK5)
0x01C4 0968 - 0x01C4 0BFF	-	Reserved
0x01C4 0C00	PID	Peripheral Identification and Revision Information Register
0x01C4 0C04 - 0x01C4 0CFF	-	Reserved
0x01C4 0D00	PLLCTL	PLL Controller 2 Operations Control Register
0x01C4 0D04 - 0x01C4 0D0F	-	Reserved
0x01C4 0D10	PLLM	PLL Controller 2 Multiplier Control Register
0x01C4 0D14 - 0x01C4 0D17	-	Reserved
0x01C4 0D18	PLLDIV1	PLL Controller 2 Control-Divider 1 Register (SYSCLK1)
0x01C4 0D1C	PLLDIV2	PLL Controller 2 Control-Divider 2 Register (SYSCLK2)
0x01C4 0D20 - 0x01C4 0D2B	POSTDIV	PLL Controller 2 Post-Divider Control Register
0x01C4 0D2C	BPDIV	PLL Controller 2 Bypass Control-Divider Register (SYSCLKBP)

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PLL and Reset Controller Registers Memory Map (continued)

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x01C4 0D30 - 0x01C4 0D37	-	Reserved
0x01C4 0D38	PLLCMD	PLL Controller 2 Command Register
0x01C4 0D3C	PLLSTAT	PLL Controller 2 Status Register (Shows PLLCTRL Status)
0x01C4 0D40	ALNCTL	PLL Controller 2 Alignment Control Register (Indicates Which SYSCLKs Need to be Aligned for Proper Device Operation)
0x01C4 0D44	DCHANGE	PLL Controller 2 Divider Change Register (Indicates if SYSCLK Divide Ratio has Been Modified)
0x01C4 0D48	CKEN	PLL Controller 2 Clock Enable Register
0x01C4 0D4C	CKSTAT	PLL Controller 2 Clock Status Register (For All Clocks Except SYSCLKx)
0x01C4 0D50	SYSTAT	PLL Controller 2 System Clock Status 1 Register (Indicates SYSCLK on/off Status)
0x01C4 0D54 - 0x01C4 0FFF	-	Reserved

5.6.1 Clock PLL Considerations with External Clock Sources

If the internal oscillator is bypassed, to minimize the clock jitter a single clean power supply should power both the DM6446 device and the external clock oscillator circuit. The minimum CLKIN rise and fall times should also be observed. For the input clock timing requirements, see the *input and output clocks* electricals section.

Rise/fall times, duty cycles (high/low pulse durations), and the load capacitance of the external clock source must meet the device requirements in this data sheet (see the *electrical characteristics over recommended ranges of supply voltage and operating case temperature* table and the *input and output clocks* electricals section).

5.6.2 Clock PLL Electrical Data/Timing (Input and Output Clocks)

Table 5-12. Timing Requirements for MXI/CLKIN (-594) Devices(1)(2)(3)(4) (see Figure 5-10)

NO.			-594		UNIT
			MIN	MAX	
1	$t_{c(MXI)}$	Cycle time, MXI/CLKIN	$33.\overline{3}$	50	ns
2	$t_{w(MXIH)}$	Pulse duration, MXI/CLKIN high	0.45C	0.55C	ns
3	$t_{w(MXIL)}$	Pulse duration, MXI/CLKIN low	0.45C	0.55C	ns
4	$t_{t(MXI)}$	Transition time, MXI/CLKIN		0.05C	ns
5	$t_{J(MXI)}$	Period jitter, MXI/CLKIN		0.02C	ns

(1) The MXI/CLKIN frequency and PLL multiply factor should be chosen such that the resulting clock frequency is within the specific range for CPU operating frequency. For example, for a -594 speed device with a 27 MHz CLKIN frequency, the PLL multiply factor should be ≤ 22.
(2) The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.
(3) For more details on the PLL multiplier factors, see the *Documentation Support* section for ARM Subsystem User's Guide.
(4) C = CLKIN cycle time in ns. For example, when MXI/CLKIN frequency is 27 MHz, use C = $37.\overline{037}$ ns.

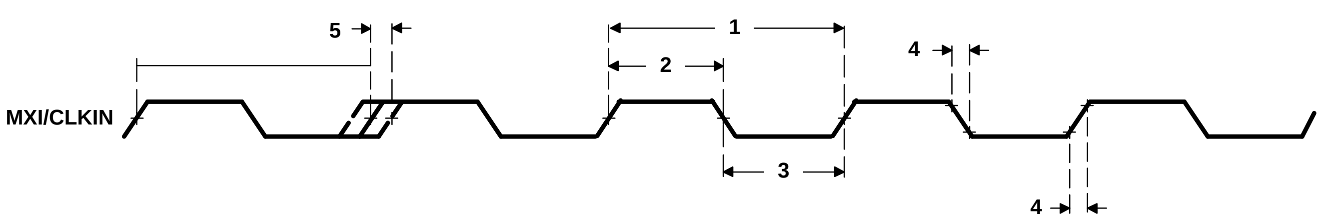

Figure 5-10. MXI/CLKIN Timing

Table 5-13. Timing Requirements for M24XI (-594) Devices[(1)(2)(3)] (see Figure 5-10)

NO.			-594			UNIT
			MIN	TYP	MAX	
1	$t_{c(M24XI)}$	Cycle time, M24XI		$41.\overline{6}$		ns
2	$t_{w(M24XIH)}$	Pulse duration, M24XI high	0.45C		0.55C	ns
3	$t_{w(M24XIL)}$	Pulse duration, M24XI low	0.45C		0.55C	ns
4	$t_{t(M24XI)}$	Transition time, M24XI			0.05C	ns
5	$t_{J(M24XI)}$	Period jitter, M24XI			0.02C	ns

(1) The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.
(2) For more details on the PLL, see the *Documentation Support* section for USB Peripheral Reference Guide.
(3) C = M24XI cycle time in ns. For example, when M24XI frequency is 24 MHz, use C = $41.\overline{6}$ ns.

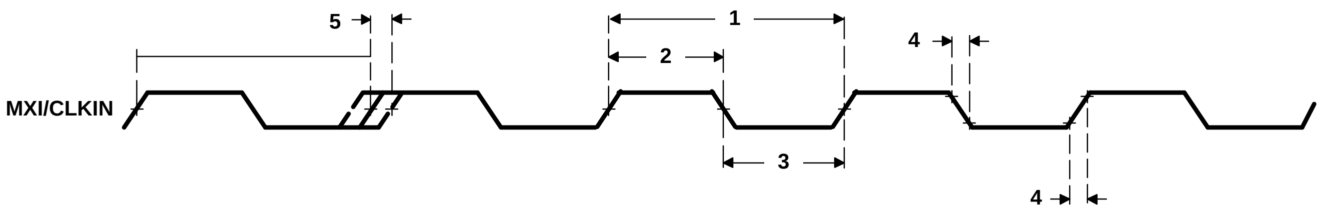

Figure 5-11. M24XI Timing

Table 5-14. Switching Characteristics Over Recommended Operating Conditions for CLKOUT0[(1)(2)] (see Figure 5-12)

NO.	PARAMETER		-594		UNIT
			MIN	MAX	
1	t_C	Cycle time, CLKOUT0	37.037	74.074	ns
2	$t_{w(CLKOUT0H)}$	Pulse duration, CLKOUT0 high	0.45P	0.55P	ns
3	$t_{w(CLKOUT0L)}$	Pulse duration, CLKOUT0 low	0.45P	0.55P	ns
4	$t_{t(CLKOUT0)}$	Transition time, CLKOUT0		0.05P	ns
5	$t_{d(CLKINH-CLKO0H)}$	Delay time, CLKIN/MXI high to CLKOUT0 high (divide-by-1 only)	1	8	ns
6	$t_{d(CLKINL-CLKO0L)}$	Delay time, CLKIN/MXI low to CLKOUT0 low (divide-by-1 only)	1	8	ns
7	$t_{d(CLKINH-CLKO0L)}$	Delay time, CLKIN/MXI high to CLKOUT0 low (divide-by-2 only)	1	8	ns
8	$t_{d(CLKINH-CLKO0H)}$	Delay time, CLKIN/MXI high to CLKOUT0 high (divide-by-2 only)	1	8	ns

(1) The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH}MIN.
(2) P = 1/CLKOUT0 clock frequency in nanoseconds (ns). For example, when CLKOUT0 frequency is 27 MHz, use P = 37.04 ns.

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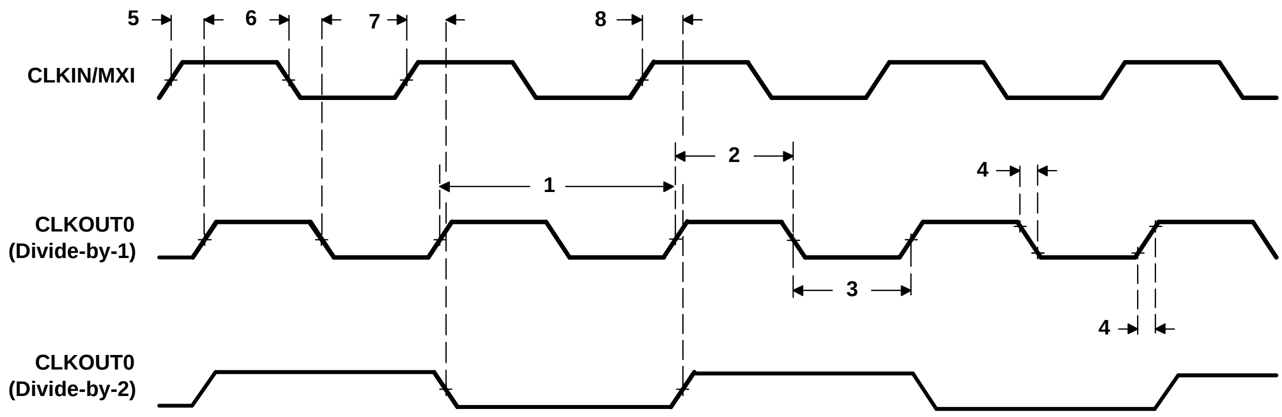

Figure 5-12. CLKOUT0 Timing

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Table 5-15. Switching Characteristics Over Recommended Operating Conditions for CLKOUT1[(1)(2)] (see Figure 5-13)

NO.	PARAMETER		-594		UNIT
			MIN	MAX	
1	t_C	Cycle time, CLKOUT1	41.667	83.33	
2	$t_{w(CLKOUT1H)}$	Pulse duration, CLKOUT1 high	0.45P	0.55P	ns
3	$t_{w(CLKOUT1L)}$	Pulse duration, CLKOUT1 low	0.45P	0.55P	ns
4	$t_{t(CLKOUT1)}$	Transition time, CLKOUT1		0.05P	ns
5	$t_{d(CLKINH-CLKO1H)}$	Delay time, CLKIN/MXI high to CLKOUT1 high (divide-by-1 only)	1	8	ns
6	$t_{d(CLKINL-CLKO1L)}$	Delay time, CLKIN/MXI low to CLKOUT1 low (divide-by-1 only)	1	8	ns
7	$t_{d(CLKINH-CLKO1L)}$	Delay time, CLKIN/MXI high to CLKOUT1 low (divide-by-2 only)	1	8	ns
8	$t_{d(CLKINH-CLKO1H)}$	Delay time, CLKIN/MXI high to CLKOUT1 high (divide-by-2 only)	1	8	ns

(1) The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH}MIN.
(2) P = 1/CLKOUT1 clock frequency in nanoseconds (ns). For example, when CLKOUT1 frequency is 24 MHz, use P = 41.$\bar{6}$ ns.

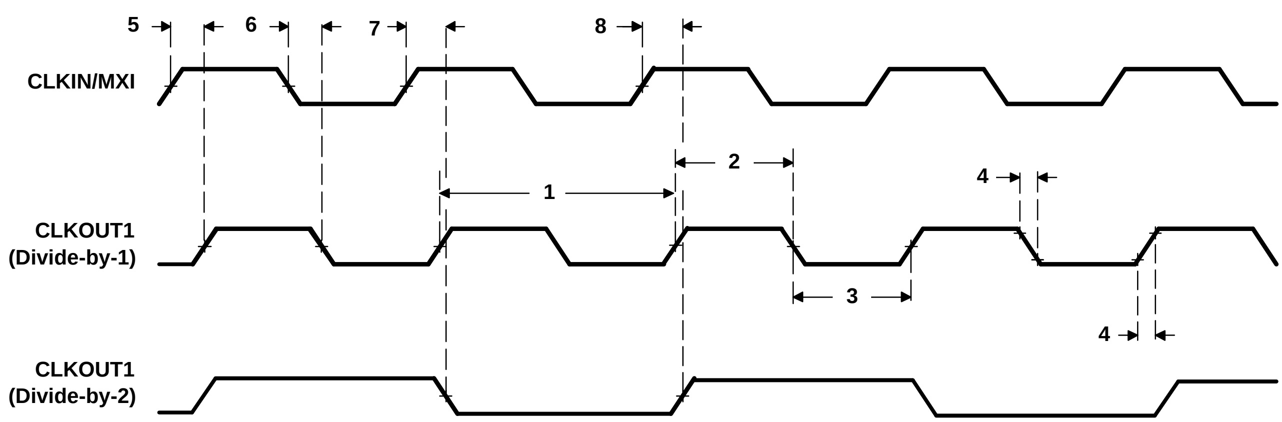

Figure 5-13. CLKOUT1 Timing

5.7 Interrupts

The DM6446 device has a large number of interrupts to service the needs of its many peripherals and subsystems. Both the ARM and C64x+ are capable of servicing these interrupts. All of the device interrupts are routed to the ARM interrupt controller with only a limited set routed to the C64x+ interrupt controller. The interrupts can be selectively enabled or disabled in either of the controllers. In typical applications, the ARM handles most of the peripheral interrupts and grants control, to the C64x+, of interrupts that are relevant to DSP algorithms. Also, the ARM and DSP can communicate with each other through interrupts.

5.7.1 MPU Interrupts

The ARM9 MPU core supports 2 direct interrupts: FIQ and IRQ. The DM6446 ARM interrupt controller prioritizes up to 64 interrupt requests from various peripherals and subsystems, which are listed in Table 5-16, and interrupts the MPU. Each interrupt is programmable for up to 8 levels of priority. There are 6 levels for IRQ and 2 levels for FIQ. Interrupts at the same priority level are serviced in order by the MPU Interrupt Number, with the lowest number having the highest priority. Table 5-17 shows the ARM interrupt controller registers and memory locations. For more details on ARM interrupt control, see the *Documentation Support* section for the ARM Subsystem User's Guide.

Table 5-16. DM6446 MPU Interrupts

MPU INTERRUPT NUMBER	ACRONYM	SOURCE	MPU INTERRUPT NUMBER	ACRONYM	SOURCE
0	VDINT0	VPSS CCDC 0	32	TINT0	Timer 0 – TINT12
1	VDINT1	VPSS CCDC 1	33	TINT1	Timer 0 – TINT34
2	VDINT2	VPSS CCDC 2	34	TINT2	Timer 1 – TINT12
3	HISTINT	VPSS Histogram	35	TINT3	Timer 1 – TINT34
4	H3AINT	VPSS AE/AWB/AF	36	PWMINT0	PWM 0
5	PRVUINT	VPSS Previewer	37	PWMINT1	PWM 1
6	RSZINT	VPSS Resizer	38	PWMINT2	PWM 2
7	-	Reserved	39	I2CINT	I2C
8	VENCINT	VPSS VPBE	40	UARTINT0	UART 0
9	ASQINT	VICP Sqr (ARM int)	41	UARTINT1	UART 1
10	IMXINT	VICP IMX	42	UARTINT2	UART 2
11	VLCDINT	VICP VLCD	43	SPINT0	SPI
12	-	Reserved	44	SPINT1	SPI
13	EMACINT	EMAC Memory Controller	45	-	Reserved
14	-	Reserved	46	DSP2ARM0	DSP Controller to ARM 0
15	-	Reserved	47	DSP2ARM1	DSP Controller to ARM 1
16	EDMA3CC_INT0	EDMA CC Region 0	48	GPIO0	GPIO 0
17	EDMA3CC_ERRINT	EDMA CC Error	49	GPIO1	GPIO 1
18	EDMA3CC_ERRINT0	EDMA TC 0 Error	50	GPIO2	GPIO 2
19	EDMA3CC_ERRINT1	EDMA TC 1 Error	51	GPIO3	GPIO 3
20	PSCINT	PSC ALLINT	52	GPIO4	GPIO 4
21	-	Reserved	53	GPIO5	GPIO 5
22	IDEINT	ATA / IDE	54	GPIO6	GPIO 6
23	-	Reserved	55	GPIO7	GPIO 7
24	ASPXINT	ASP Transmit	56	GPIOBNK0	GPIO Bank 0
25	ASPRINT	ASP Receive	57	GPIOBNK1	GPIO Bank 1
26	MMCINT	MMC	58	GPIOBNK2	GPIO Bank 2
27	SDIOINT	SD	59	GPIOBNK3	GPIO Bank 3

Table 5-16. DM6446 MPU Interrupts (continued)

MPU INTERRUPT NUMBER	ACRONYM	SOURCE	MPU INTERRUPT NUMBER	ACRONYM	SOURCE
28	-	Reserved	60	GPIOBNK4	GPIO Bank 4
29	DDRINT	DDR2 Memory Controller	61	COMMTX	ARMSS
30	EMIFAINT	EMIFA	62	COMMRX	ARMSS
31	VLQINT	VLYNQ	63	EMUINT	E2ICE

Table 5-17. ARM Interrupt Controller Registers

HEX ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01C4 8000	FIQ0	FIQ Interrupt Status 0 [Interrupt Status of INT[31:0] (If Mapped to FIQ)]
0x01C4 8004	FIQ1	FIQ Interrupt Status 1 [Interrupt Status of INT[63:32] (If Mapped to FIQ)]
0x01C4 8008	IRQ0	IRQ Interrupt Status 0 [Interrupt Status of INT[31:0] (If Mapped to IRQ)]
0x01C4 800C	IRQ1	IRQ Interrupt Status 1 [Interrupt Status of INT[63:32] (If Mapped to IRQ)]
0x01C4 8010	FIQENTRY	Entry Address [28:0] for Valid FIQ Interrupt
0x01C4 8014	IRQENTRY	Entry Address [28:0] for Valid IRQ Interrupt
0x01C4 8018	EINT0	Interrupt Enable Register 0
0x01C4 801C	EINT1	Interrupt Enable Register 1
0x01C4 8020	INCTL	Interrupt Operation Control Register
0x01C4 8024	EABASE	Interrupt Entry Table Base Address Register
0x01C4 8028 - 0x01C4 802F	-	Reserved
0x01C4 8030	INTPRI0	Interrupt 0-7 Priority Select
0x01C4 8034	INTPRI1	Interrupt 8-15 Priority Select
0x01C4 8038	INTPRI2	Interrupt 16-23 Priority Select
0x01C4 803C	INTPRI3	Interrupt 24-31 Priority Select
0x01C4 8040	INTPRI4	Interrupt 32-39 Priority Select
0x01C4 8044	INTPRI5	Interrupt 40-47 Priority Select
0x01C4 8048	INTPRI6	Interrupt 48-55 Priority Select
0x01C4 804C	INTPRI7	Interrupt 56-63 Priority Select
0x01C4 8050 - 0x01C4 83FF	-	Reserved

5.7.2 DSP Interrupts

The C64x+ DSP interrupt controller combines device events into 12 prioritized interrupts. The source for each of the 12 CPU interrupts is user programmable and is listed in Table 5-18. Also, the interrupt controller controls the generation of the CPU exception, NMI, and emulation interrupts and the generation of AEG events. Table 5-19 summarizes the C64x+ interrupt controller registers and memory locations. For more details on DSP interrupt control, see the *Documentation Support* section for the DSP Subsystem User's Guide.

Table 5-18. DM6446 DSP Interrupts

DSP INTERRUP T NUMBER	ACRONYM	SOURCE	DSP INTERRUP T NUMBER	ACRONYM	SOURCE
0	EVT0	C64x+ Int Ctl 0	64		Reserved
1	EVT1	C64x+ Int Ctl 1	65		Reserved

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Table 5-18. DM6446 DSP Interrupts (continued)

DSP INTERRUPT NUMBER	ACRONYM	SOURCE	DSP INTERRUPT NUMBER	ACRONYM	SOURCE
2	EVT2	C64x+ Int Ctl 2	66		Reserved
3	EVT3	C64x+ Int Ctl 3	67		Reserved
4	TINT0	Timer 0 – TINT12	68		Reserved
5	TINT1	Timer 0 – TINT34	69		Reserved
6	TINT2	Timer 1 – TINT12	70		Reserved
7	TINT3	Timer 1 – TINT34	71		Reserved
8		Reserved	72		Reserved
9	EMU_DTDMA	C64X+ ECM	73		Reserved
10		Reserved	74		Reserved
11	EMU_RTDXRX	C64x+ RTDX	75		Reserved
12	EMU_RTDXTX	C64x+ RTDX	76		Reserved
13	IDMAINT0	C64x+ EMC 0	77		Reserved
14	IDMAINT1	C64x+ EMC 1	78		Reserved
15		Reserved	79		Reserved
16	ARM2DSP0	ARM to DSP Controller 0	80		Reserved
17	ARM2DSP1	ARM to DSP Controller 1	81		Reserved
18	ARM2DSP2	ARM to DSP Controller 2	82		Reserved
19	ARM2DSP3	ARM to DSP Controller 3	83		Reserved
20	DSQINT	VICP Sqr (DSP int)	84		Reserved
21	IMXINT	VICP IMX	85		Reserved
22	VLCDINT	VICP VLCD	86		Reserved
23		Reserved	87		Reserved
24		Reserved	88		Reserved
25		Reserved	89		Reserved
26		Reserved	90		Reserved
27		Reserved	91		Reserved
28		Reserved	92		Reserved
29		Reserved	93		Reserved
30		Reserved	94		Reserved
31		Reserved	95		Reserved
32		Reserved	96	INTERR	C64x+ INT Ctl
33		Reserved	97	EMC_IDMAERR	C64x+ EMC
34		Reserved	98	PBISTINT	PBIST
35		Reserved	99	DFTINT	SYS DFT
36	EDMA3CC_INT1	EDMACC Interrupt Region 1	100	EFIINTA	C64x+ EFI A
37	EDMA3CC_ERRINT	EDMA CC Error	101	EFIITNB	C64x+ EFI B
38	EDMA3CC_ERRINT0	EDMA TC0 Error	102		Reserved
39	EDMA3CC_ERRINT1	EDMA TC1 Error	103		Reserved
40	PSCINT	PSC ALLINT	104		Reserved
41		Reserved	105		Reserved
42		Reserved	106		Reserved
43		Reserved	107		Reserved
44		Reserved	108		Reserved
45		Reserved	109		Reserved
46		Reserved	110		Reserved

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Table 5-18. DM6446 DSP Interrupts (continued)

DSP INTERRUPT NUMBER	ACRONYM	SOURCE	DSP INTERRUPT NUMBER	ACRONYM	SOURCE
47		Reserved	111		Reserved
48	ASPXINT	ASP Transmit	112	PMC_ED	C64x+ PMC
49	ASPRINT	ASP Receive	113		Reserved
50		Reserved	114		Reserved
51		Reserved	115		Reserved
52		Reserved	116	UMCED1	C64x+ UMC 1
53		Reserved	117	UMCED2	C64x+ UMC 2
54		Reserved	118	PDCERR	C64x+ PDC
55		Reserved	119	PVCINT	C64x+ PDC
56		Reserved	120	PMCCMPA	C64x+ PMC
57		Reserved	121	PMCDMPA	C64x+ PMC
58		Reserved	122	DMCCMPA	C64x+ DMC
59		Reserved	123	DMCDMPA	C64x+ DMC
60		Reserved	124	UMCCMPA	C64x+ UMC
61		Reserved	125	UMCDMPA	C64x+ UMC
62		Reserved	126	EMCCMPA	C64x+ EMC
63		Reserved	127	EMCDMPA	C64x+ EMC

Table 5-19. C64x+ Interrupt Controller Registers

HEX ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x0180 0000	EVTFLAG0	Event flag register 0
0x0180 0004	EVTFLAG1	Event flag register 1
0x0180 0008	EVTFLAG2	Event flag register 2
0x0180 000C	EVTFLAG3	Event flag register 3
0x0180 0020	EVTSET0	Event set register 0
0x0180 0024	EVTSET1	Event set register 1
0x0180 0028	EVTSET2	Event set register 2
0x0180 002C	EVTSET3	Event set register 3
0x0180 0040	EVTCLR0	Event clear register 0
0x0180 0044	EVTCLR1	Event clear register 1
0x0180 0048	EVTCLR2	Event clear register 2
0x0180 004C	EVTCLR3	Event clear register 3
0x0180 0080	EVTMASK0	Event mask register 0
0x0180 0084	EVTMASK1	Event mask register 1
0x0180 0088	EVTMASK2	Event mask register 2
0x0180 008C	EVTMASK3	Event mask register 3
0x0180 00C0	EXPMASK0	Exception mask register 0
0x0180 00C4	EXPMASK1	Exception mask register 1
0x0180 00C8	EXPMASK2	Exception mask register 2
0x0180 00CC	EXPMASK3	Exception mask register 3
0x0180 00A0	MEVTFLAG0	Masked event flag register 0
0x0180 00A4	MEVTFLAG1	Masked event flag register 1
0x0180 00A8	MEVTFLAG2	Masked event flag register 2
0x0180 00AC	MEVTFLAG3	Masked event flag register 3

Table 5-19. C64x+ Interrupt Controller Registers (continued)

HEX ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x0180 00E0	MEXPFLAG0	Masked exception flag register 0
0x0180 00E4	MEXPFLAG1	Masked exception flag register 1
0x0180 00E8	MEXPFLAG2	Masked exception flag register 2
0x0180 00EC	MEXPFLAG3	Masked exception flag register 3
0x0180 0104	INTMUX1	Interrupt mux register 1
0x0180 0108	INTMUX2	Interrupt mux register 2
0x0180 010C	INTMUX3	Interrupt mux register 3
0x0180 0140	AEGMUX0	Advanced event generator mux register 0
0x0180 0144	AEGMUX1	Advanced event generator mux register 1
0x0180 0180	INTXSTAT	Interrupt exception status
0x0180 0184	INTXCLR	Interrupt exception clear
0x0180 0188	INTDMASK	Dropped interrupt mask register
0x0180 01C0	EVTASRT	Event assert register

5.7.3 *ARM/DSP Communication Interrupts*

The INTGEN register is used for generating interrupts between the ARM and DSP. The INTGEN register format is shown in Figure 5-14. Table 5-20 describes the register bit fields. The ARM may generate an interrupt to the DSP by setting one of the four INTDSP[3:0] bits or the INTNMI bit. The interrupt bit automatically self clears and the corresponding DSP[3:0]STAT or NMISTAT bit is automatically set to indicate that the interrupt was generated. After servicing the interrupt, the DSP clears the status bit by writing ‘0’. The ARM may poll the status bit to determine when the DSP has completed servicing the interrupt. The DSP may generate an interrupt to the ARM in the same manner using the INTARM[1:0] bits and monitor ARM interrupt servicing via the ARM[1:0]STAT bits.

Figure 5-14. INTGEN Register

31–30	29	28	27–24	23	22	21	20	19–17	16
Reserved	ARM1 STAT	ARM0 STAT	Reserved	DSP3 STAT	DSP2 STAT	DSP1 STAT	DSP0 STAT	Reserved	NMI STAT
R-00	R/W-0	R/W-0	R-0000	R/W-0	R/W-0	R/W-0	R/W-0	R-000	R/W-0

15–14	13	12	11–8	7	6	5	4	3–1	0
Reserved	INT ARM1	INT ARM0	Reserved	INT DSP3	INT DSP2	INT DSP1	INT DSP0	Reserved	INT NMI
R-00	R/W-0	R/W-0	R-0000	R/W-0	R/W-0	R/W-0	R/W-0	R-000	R/W-0

LEGEND: R = Read, W = Write, n = value at reset

Table 5-20. INTGEN Register Bit Fields Descriptions

Name	Description
ARM1STAT	DSP to ARM Int1 Status/Clear (1)
ARM0STAT	DSP to ARM Int0 Status/Clear (1)
DSP3STAT	ARM to DSP Int3 Status/Clear (1)
DSP2STAT	ARM to DSP Int2 Status/Clear (1)
DSP1STAT	ARM to DSP Int1 Status/Clear (1)
DSP0STAT	ARM to DSP Int0 Status/Clear (1)
NMISTAT	DSP NMI Status/Clear (1)
INTARM1	DSP to ARM Int1 Set (2)

(1) Write '0' to clear. Writing '1' has no effect.
(2) Write '1' to generate the interrupt. The register bit automatically clears to a value of '0'. Writing a '0' has no effect.

Table 5-20. INTGEN Register Bit Fields Descriptions (continued)

Name	Description
INTARM0	DSP to ARM Int0 Set(2)
INTDSP3	ARM to DSP Int3 Set(2)
INTDSP2	ARM to DSP Int2 Set(2)
INTDSP1	ARM to DSP Int1 Set(2)
INTDSP0	ARM to DSP Int0 Set(2)
INTNMI	DSP NMI Set(2)

5.8 General-Purpose Input/Output (GPIO)

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, a write to an internal register can control the state driven on the output pin. When configured as an input, the state of the input is detectable by reading the state of an internal register. In addition, the GPIO peripheral can produce CPU interrupts and EDMA events in different interrupt/event generation modes. The GPIO peripheral provides generic connections to external devices. The GPIO pins are grouped into banks of 16 pins per bank (i.e., bank 0 consists of GPIO [0:15]).

The DM6446 GPIO peripheral supports the following:

- Up to 54 1.8v GPIO pins, GPIO[0:53]
- Up to 17 3.3v GPIO pins, GPIO3V[0:16] (GPIO[54:70])
- Interrupts:
  - Up to 8 unique GPIO[0:7] interrupts from Bank 0
  - 5 GPIO bank (aggregated) interrupt signals from each of the 5 banks of GPIOs
  - Interrupts can be triggered by rising and/or falling edge, specified for each interrupt capable GPIO signal
- DMA events:
  - Up to 8 unique GPIO DMA events from Bank 0
  - 5 GPIO bank (aggregated) DMA event signals from each of the 5 banks of GPIOs
- Set/clear functionality: Firmware writes 1 to corresponding bit position(s) to set or to clear GPIO signal(s). This allows multiple firmware processes to toggle GPIO output signals without critical section protection (disable interrupts, program GPIO, re-enable interrupts, to prevent context switching to anther process during GPIO programming).
- Separate Input/Output registers
- Output register in addition to set/clear so that, if preferred by firmware, some GPIO output signals can be toggled by direct write to the output register(s).
- Output register, when read, reflects output drive status. This, in addition to the input register reflecting pin status and open-drain I/O cell, allows wired logic be implemented.

The memory map for the GPIO registers is shown in Table 5-21. For more detailed information on GPIOs, see the *Documentation Support* section for the General-Purpose Input/Output (GPIO) Reference Guide.

5.8.1 GPIO Peripheral Register Description(s)

Table 5-21. GPIO Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C6 7000 - 0x01C6 7003	PID	Peripheral Indentification Register
0x01C6 7004	-	Reserved
0x01C6 7008	BINTEN	GPIO interrupt per-bank enable
GPIO Banks 0 and 1		
0x01C6 700C	-	Reserved
0x01C6 7010	DIR01	GPIO Banks 0 and 1 Direction Register (GPIO[0:31])
0x01C6 7014	OUT_DATA01	GPIO Banks 0 and 1Output Data Register (GPIO[0:31])
0x01C6 7018	SET_DATA01	GPIO Banks 0 and 1 Set Data Register (GPIO[0:31])
0x01C6 701C	CLR_DATA01	GPIO Banks 0 and 1clear data for banks 0 and 1 (GPIO[0:31])
0x01C6 7020	IN_DATA01	GPIO Banks 0 and 1 Input Data Register (GPIO[0:31])
0x01C6 7024	SET_RIS_TRIG01	GPIO Banks 0 and 1 Set Rising Edge Interrupt Register (GPIO[0:31])
0x01C6 7028	CLR_RIS_TRIG01	GPIO Banks 0 and 1Clear Rising Edge Interrupt Register (GPIO[0:31])
0x01C6 702C	SET_FAL_TRIG01	GPIO Banks 0 and 1Set Falling Edge Interrupt Register (GPIO[0:31])
0x01C6 7030	CLR_FAL_TRIG01	GPIO Banks 0 and 1Clear Falling edge Interrupt Register (GPIO[0:31])

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Table 5-21. GPIO Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C6 7034	INSTAT01	GPIO Banks 0 and 1 Interrupt Status Register (GPIO[0:31])
GPIO Banks 2 and 3		
0x01C6 7038	DIR23	GPIO Banks 2 and 3 Direction Register (GPIO[32:63])
0x01C6 703C	OUT_DATA23	GPIO Banks 2 and 3 Output Data Register (GPIO[32:63])
0x01C6 7040	SET_DATA23	GPIO Banks 2 and 3 Set Data Register (GPIO[32:63])
0x01C6 7044	CLR_DATA23	GPIO Banks 2 and 3 Clear Data Register (GPIO[32:63])
0x01C6 7048	IN_DATA23	GPIO Banks 2 and 3 Input Data Register (GPIO[32:63])
0x01C6 704C	SET_RIS_TRIG23	GPIO Banks 2 and 3 Set Rising Edge Interrupt Register (GPIO[32:63])
0x01C6 7050	CLR_RIS_TRIG23	GPIO Banks 2 and 3 Clear Rising Edge Interrupt Register (GPIO[32:63])
0x01C6 7054	SET_FAL_TRIG23	GPIO Banks 2 and 3 Set Falling Edge Interrupt Register (GPIO[32:63])
0x01C6 7058	CLR_FAL_TRIG23	GPIO Banks 2 and 3 Clear Falling Edge Onterrupt Register (GPIO[32:63])
0x01C6 705C	INSTAT23	GPIO Banks 2 and 3 Interrupt Status Register (GPIO[32:63])
GPIO Bank 4		
0x01C6 7060	DIR4	GPIO Bank 4 Direction Register (GPIO[64:70])
0x01C6 7064	OUT_DATA4	GPIO Bank 4 Output Data Register (GPIO[64:70])
0x01C6 7068	SET_DATA4	GPIO Bank 4 Set Data Register (GPIO[64:70])
0x01C6 706C	CLR_DATA4	GPIO Bank 4 Clear Data Register (GPIO[64:70])
0x01C6 7070	IN_DATA4	GPIO Bank 4 Input Data Register (GPIO[64:70])
0x01C6 7074	SET_RIS_TRIG4	GPIO Bank 4 Set Rising Edge Interrupt Register (GPIO[64:70])
0x01C6 7078	CLR_RIS_TRIG4	GPIO Bank 4 Clear Rising Edge Interrupt Register (GPIO[64:70])
0x01C6 707C	SET_FAL_TRIG4	GPIO Bank 4 Set Falling Edge Interrupt Register (GPIO[64:70])
0x01C6 7080	CLR_FAL_TRIG4	GPIO Bank 4 Clear Falling Edge Interrupt Register (GPIO[64:70])
0x01C6 7084	INSTAT4	GPIO Bank 4 Interrupt Status Register (GPIO[64:70])
0x01C6 7088 - 0x01C6 7FFF	-	Reserved

5.8.2 GPIO Peripheral Input/Output Electrical Data/Timing

Table 5-22. Timing Requirements for GPIO Inputs[(1)] (see Figure 5-15)

NO.			-594		UNIT
			MIN	MAX	
1	$t_{w(GPIH)}$	Pulse duration, GPIx high	52		ns
2	$t_{w(GPIL)}$	Pulse duration, GPIx low	52		ns

(1) The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have DM6446 recognize the GPIx changes through software polling of the GPIO register, the GPIx duration must be extended to allow DM6446 enough time to access the GPIO register through the internal bus.

Table 5-23. Switching Characteristics Over Recommended Operating Conditions for GPIO Outputs (see Figure 5-15)

NO.	PARAMETER		-594		UNIT
			MIN	MAX	
3	$t_{w(GPOH)}$	Pulse duration, GPOx high	26[(1)]		ns
4	$t_{w(GPOL)}$	Pulse duration, GPOx low	26[(1)]		ns

(1) This parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.

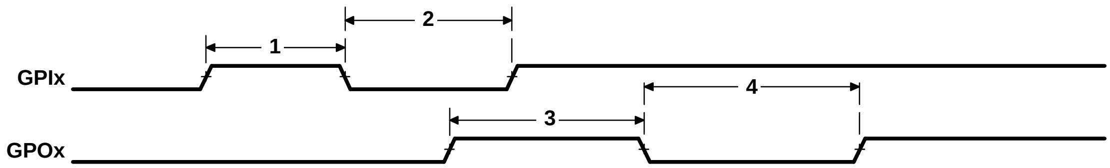

Figure 5-15. GPIO Port Timing

5.8.3 GPIO Peripheral External Interrupts Electrical Data/Timing

Table 5-24. Timing Requirements for External Interrupts(1) (see Figure 5-16)

NO.			-594 MIN	-594 MAX	UNIT
1	$t_{w(ILOW)}$	Width of the external interrupt pulse low	52		ns
2	$t_{w(IHIGH)}$	Width of the external interrupt pulse high	52		ns

(1) The pulse width given is sufficient to generate an interrupt or an EDMA event. However, if a user wants to have DM6446recognize the GPIO changes through software polling of the GPIO register, the GPIO duration must be extended to allow DM6446 enough time to access the GPIO register through the internal bus.

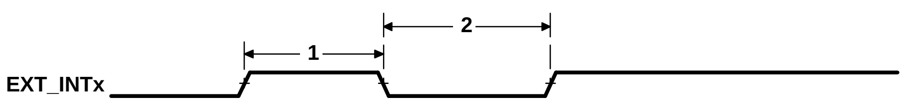

Figure 5-16. GPIO External Interrupt Timing

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5.9 Enhanced Direct Memory Access (EDMA) Controller

The EDMA controller handles all data transfers between memories and the device slave peripherals on the DM6446 device. These data transfers include cache servicing, non-cacheable memory accesses, user-programmed data transfers, and host accesses. These are summarized as follows:

- Transfer to/from on-chip memories
  - Coprocessor shared memory
  - DSP L1D memory
  - DSP L2 memory
  - ARM program/data RAM
- Transfer to/from external storage
  - DDR2 SDRAM
  - NAND flash
  - Asynchronous EMIF
  - Smart Media, SD, MMC, xD media storage
  - ATA/CF
- Transfer to/from peripherals/hosts
  - VLYNQ
  - ASP
  - SPI
  - PWM
  - UART

5.9.1 EDMA Channel Synchronization Events

The EDMA supports up to 64 EDMA channels which service peripheral devices and external memory. Table 5-25 lists the source of EDMA synchronization events associated with each of the programmable EDMA channels. For the DM6446 device, the association of an event to a channel is fixed; each of the EDMA channels has one specific event associated with it. These specific events are captured in the EDMA event registers (ER, ERH) even if the events are disabled by the EDMA event enable registers (EER, EERH). For more detailed information on the EDMA module and how EDMA events are enabled, captured, processed, linked, chained, and cleared, etc., see the *Document Support* section for the Enhanced Direct Memory Access (EDMA) Controller Reference Guide.

Table 5-25. DM6446 EDMA Channel Synchronization Events(1)

EDMA CHANNEL	EVENT NAME	EVENT DESCRIPTION
0-1		Reserved
2	XEVT	ASP Transmit Event
3	REVT	ASP Receive Event
4	HISTEVT	VPSS Histogram Event
5	H3AEVT	VPSS H3A Event
6	PRVUEVT	VPSS Previewer Event
7	RSZEVT	VPSS Resizer Event
8	IMXINT	VICP Interrupt
9	VLCDINT	VICP VLCD Interrupt
10	ASQINT	VICP ASQ Interrupt
11	DSQINT	VICP DSQ Interrupt

(1) In addition to the events shown in this table, each of the 64 channels can also be synchronized with the transfer completion or alternate transfer completion events. For more detailed information on EDMA event-transfer chaining, see the *Document Support* section for the Enhanced Direct Memory Access (EDMA) Controller Reference Guide.

Table 5-25. DM6446 EDMA Channel Synchronization Events (continued)

EDMA CHANNEL	EVENT NAME	EVENT DESCRIPTION
12-15		Reserved
16	SPIXEVT	SPI Transmit Event
17	SPIREVT	SPI Receive Event
18	URXEVT0	UART 0 Receive Event
19	UTXEVT0	UART 0 Transmit Event
20	URXEVT1	UART 1 Receive Event
21	UTXEVT1	UART 1 Transmit Event
22	URXEVT2	UART 2 Receive Event
23	UTXEVT2	UART 2 Transmit Event
24		Reserved
25		Reserved
26	MMCRXEVT	MMC Receive Event
27	MMCTXEVT	MMC Transmit Event
28	I2CREVT	I2C Receive Event
29	I2CXEVT	I2C Transmit Event
30-31		Reserved
32	GPINT0	GPIO 0 Interrupt
33	GPINT1	GPIO 1 Interrupt
34	GPINT2	GPIO 2 Interrupt
35	GPINT3	GPIO 3 Interrupt
36	GPINT4	GPIO 4 Interrupt
37	GPINT5	GPIO 5 Interrupt
38	GPINT6	GPIO 6 Interrupt
39	GPINT7	GPIO 7 Interrupt
40	GPBNKINT0	GPIO Bank 0 Interrupt
41	GPBNKINT1	GPIO Bank 1 Interrupt
42	GPBNKINT2	GPIO Bank 2 Interrupt
43	GPBNKINT3	GPIO Bank 3 Interrupt
44	GPBNKINT4	GPIO Bank 4 Interrupt
45-47		Reserved
48	TINT0	Timer 0 Interrupt
49	TINT1	Timer 1 Interrupt
50	TINT2	Timer 2 Interrupt
51	TINT3	Timer 3 Interrupt
52	PWM0	PWM 0 Event
53	PWM1	PWM 1 Event
54	PWM2	PWM 2 Event
55-63		Reserved

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5.9.2 EDMA Peripheral Register Descriptions

Table 5-26 lists the EDMA registers, their corresponding acronyms, and DM6446 device memory locations.

Table 5-26. DM6446 EDMA Registers

HEX ADDRESS	ACRONYM	REGISTER NAME
Channel Controller Registers		

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Table 5-26. DM6446 EDMA Registers (continued)

HEX ADDRESS	ACRONYM	REGISTER NAME
0x01c0 0000 - 0x01c0 0003		Reserved
0x01c0 0004	CCCFG	EDMA3CC Configuration Register
0x01c0 0008 - 0x01c0 01FF		Reserved
	Global Registers	
0x01c0 0200	QCHMAP0	QDMA Channel 0 Mapping to PaRAM Register
0x01c0 0204	QCHMAP1	QDMA Channel 1 Mapping to PaRAM Register
0x01c0 0208	QCHMAP2	QDMA Channel 2 Mapping to PaRAM Register
0x01c0 020C	QCHMAP3	QDMA Channel 3 Mapping to PaRAM Register
0x01c0 0210	QCHMAP4	QDMA Channel 4 Mapping to PaRAM Register
0x01c0 0214	QCHMAP5	QDMA Channel 5 Mapping to PaRAM Register
0x01c0 0218	QCHMAP6	QDMA Channel 6 Mapping to PaRAM Register
0x01c0 021C	QCHMAP7	QDMA Channel 7 Mapping to PaRAM Register
0x01c0 0240	DMAQNUM0	DMA Queue Number Register 0 (Channels 00 to 07)
0x01c0 0244	DMAQNUM1	DMA Queue Number Register 1 (Channels 08 to 15)
0x01c0 0248	DMAQNUM2	DMA Queue Number Register 2 (Channels 16 to 23)
0x01c0 024C	DMAQNUM3	DMA Queue Number Register 3 (Channels 24 to 31)
0x01c0 0250	DMAQNUM4	DMA Queue Number Register 4 (Channels 32 to 39)
0x01c0 0254	DMAQNUM5	DMA Queue Number Register 5 (Channels 40 to 47)
0x01c0 0258	DMAQNUM6	DMA Queue Number Register 6 (Channels 48 to 55)
0x01c0 025C	DMAQNUM7	DMA Queue Number Register 7 (Channels 56 to 63)
0x01c0 0260	QDMAQNUM	CC QDMA Queue Number
0x01c0 0280	–	Reserved
0x01c0 0284	QUEPRI	Queue Priority Register
0x01c0 0248 - 0x01c0 02FF	–	Reserved
0x01c0 0300	EMR	Event Missed Register
0x01c0 0304	EMRH	Event Missed Register High
0x01c0 0308	EMCR	Event Missed Clear Register
0x01c0 030C	EMCRH	Event Missed Clear Register High
0x01c0 0310	QEMR	QDMA Event Missed Register
0x01c0 0314	QEMCR	QDMA Event Missed Clear Register
0x01c0 0318	CCERR	EDMA3CC Error Register
0x01c0 031C	CCERRCLR	EDMA3CC Error Clear Register
0x01c0 0320	EEVAL	Error Evaluate Register
0x01c0 0340	DRAE0	DMA Region Access Enable Register for Region 0
0x01c0 0344	DRAEH0	DMA Region Access Enable Register High for Region 0
0x01c0 0348	DRAE1	DMA Region Access Enable Register for Region 1
0x01c0 034C	DRAEH1	DMA Region Access Enable Register High for Region 1
0x01c0 0350	DRAE2	DMA Region Access Enable Register for Region 2
0x01c0 0354	DRAEH2	DMA Region Access Enable Register High for Region 2
0x01c0 0358	DRAE3	DMA Region Access Enable Register for Region 3
0x01c0 035C	DRAEH3	DMA Region Access Enable Register High for Region 3
0x01c0 0360	–	Reserved
0x01c0 0364	–	Reserved
0x01c0 0368	–	Reserved
0x01c0 036C	–	Reserved
0x01c0 0370	–	Reserved
0x01c0 0374	–	Reserved

Table 5-26. DM6446 EDMA Registers (continued)

HEX ADDRESS	ACRONYM	REGISTER NAME
0x01c0 0378	–	Reserved
0x01c0 037C	–	Reserved
0x01c0 0380	QRAE0	QDMA Region Access Enable Register for Region 0
0x01c0 0384	QRAE1	QDMA Region Access Enable Register for Region 1
0x01c0 0388	QRAE2	QDMA Region Access Enable Register for Region 2
0x01c0 038C	QRAE3	QDMA Region Access Enable Register for Region 3
0x01c0 0390 - 0x01c0 039C	–	Reserved
0x01c0 0400	Q0E0	Event Q0 Entry 0 Register
0x01c0 0404	Q0E1	Event Q0 Entry 1 Register
0x01c0 0408	Q0E2	Event Q0 Entry 2 Register
0x01c0 040C	Q0E3	Event Q0 Entry 3 Register
0x01c0 0410	Q0E4	Event Q0 Entry 4 Register
0x01c0 0414	Q0E5	Event Q0 Entry 5 Register
0x01c0 0418	Q0E6	Event Q0 Entry 6 Register
0x01c0 041C	Q0E7	Event Q0 Entry 7 Register
0x01c0 0420	Q0E8	Event Q0 Entry 8 Register
0x01c0 0424	Q0E9	Event Q0 Entry 9 Register
0x01c0 0428	Q0E10	Event Q0 Entry 10 Register
0x01c0 042C	Q0E11	Event Q0 Entry 11 Register
0x01c0 0430	Q0E12	Event Q0 Entry 12 Register
0x01c0 0434	Q0E13	Event Q0 Entry 13 Register
0x01c0 0438	Q0E14	Event Q0 Entry 14 Register
0x01c0 043C	Q0E15	Event Q0 Entry 15 Register
0x01c0 0440	Q1E0	Event Q1 Entry 0 Register
0x01c0 0444	Q1E1	Event Q1 Entry 1 Register
0x01c0 0448	Q1E2	Event Q1 Entry 2 Register
0x01c0 044C	Q1E3	Event Q1 Entry 3 Register
0x01c0 0450	Q1E4	Event Q1 Entry 4 Register
0x01c0 0454	Q1E5	Event Q1 Entry 5 Register
0x01c0 0458	Q1E6	Event Q1 Entry 6 Register
0x01c0 045C	Q1E7	Event Q1 Entry 7 Register
0x01c0 0460	Q1E8	Event Q1 Entry 8 Register
0x01c0 0464	Q1E9	Event Q1 Entry 9 Register
0x01c0 0468	Q1E10	Event Q1 Entry 10 Register
0x01c0 046C	Q1E11	Event Q1 Entry 11 Register
0x01c0 0470	Q1E12	Event Q1 Entry 12 Register
0x01c0 0474	Q1E13	Event Q1 Entry 13 Register
0x01c0 0478	Q1E14	Event Q1 Entry 14 Register
0x01c0 047C	Q1E15	Event Q1 Entry 15 Register
0x01c0 0480 - 0x01c0 05FF		Reserved
0x01c0 0600	QSTAT0	Queue 0 Status Register
0x01c0 0604	QSTAT1	Queue 1 Status Register
0x01c0 0608 - 0x01c0 061F		Reserved
0x01c0 0620	QWMTHRA	Queue Watermark Threshold A Register for Q[3:0]
0x01c0 0624	–	Reserved
0x01c0 0640	CCSTAT	EDMA3CC Status Register
0x01c0 0644 - 0x01c0 0FFF		Reserved

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Table 5-26. DM6446 EDMA Registers (continued)

HEX ADDRESS	ACRONYM	REGISTER NAME
Global Channel Registers		
0x01c0 1000	ER	Event Register
0x01c0 1004	ERH	Event Register High
0x01c0 1008	ECR	Event Clear Register
0x01c0 100C	ECRH	Event Clear Register High
0x01c0 1010	ESR	Event Set Register
0x01c0 1014	ESRH	Event Set Register High
0x01c0 1018	CER	Chained Event Register
0x01c0 101C	CERH	Chained Event Register High
0x01c0 1020	EER	Event Enable Register
0x01c0 1024	EERH	Event Enable Register High
0x01c0 1028	EECR	Event Enable Clear Register
0x01c0 102C	EECRH	Event Enable Clear Register High
0x01c0 1030	EESR	Event Enable Set Register
0x01c0 1034	EESRH	Event Enable Set Register High
0x01c0 1038	SER	Secondary Event Register
0x01c0 103C	SERH	Secondary Event Register High
0x01c0 1040	SECR	Secondary Event Clear Register
0x01c0 1044	SECRH	Secondary Event Clear Register High
0x01c0 1048 - 0x01c0 104F		Reserved
0x01c0 1050	IER	Interrupt Enable Register
0x01c0 1054	IERH	Interrupt Enable Register High
0x01c0 1058	IECR	Interrupt Enable Clear Register
0x01c0 105C	IECRH	Interrupt Enable Clear Register High
0x01c0 1060	IESR	Interrupt Enable Set Register
0x01c0 1064	IESRH	Interrupt Enable Set Register High
0x01c0 1068	IPR	Interrupt Pending Register
0x01c0 106C	IPRH	Interrupt Pending Register High
0x01c0 1070	ICR	Interrupt Clear Register
0x01c0 1074	ICRH	Interrupt Clear Register High
0x01c0 1078	IEVAL	Interrupt Evaluate Register
0x01c0 1080	QER	QDMA Event Register
0x01c0 1084	QEER	QDMA Event Enable Register
0x01c0 1088	QEECR	QDMA Event Enable Clear Register
0x01c0 108C	QEESR	QDMA Event Enable Set Register
0x01c0 1090	QSER	QDMA Secondary Event Register
0x01c0 1094	QSECR	QDMA Secondary Event Clear Register
0x01c0 1098 - 0x01c0 1FFF		Reserved
Shadow Region 0 Channel Registers		
0x01c0 2000	ER	Event Register
0x01c0 2004	ERH	Event Register High
0x01c0 2008	ECR	Event Clear Register
0x01c0 200C	ECRH	Event Clear Register High
0x01c0 2010	ESR	Event Set Register
0x01c0 2014	ESRH	Event Set Register High
0x01c0 2018	CER	Chained Event Register
0x01c0 201C	CERH	Chained Event Register High

Table 5-26. DM6446 EDMA Registers (continued)

HEX ADDRESS	ACRONYM	REGISTER NAME
0x01c0 2020	EER	Event Enable Register
0x01c0 2024	EERH	Event Enable Register High
0x01c0 2028	EECR	Event Enable Clear Register
0x01c0 202C	EECRH	Event Enable Clear Register High
0x01c0 2030	EESR	Event Enable Set Register
0x01c0 2034	EESRH	Event Enable Set Register High
0x01c0 2038	SER	Secondary Event Register
0x01c0 203C	SERH	Secondary Event Register High
0x01c0 2040	SECR	Secondary Event Clear Register
0x01c0 2044	SECRH	Secondary Event Clear Register High
0x01c0 2048	-	Reserved
0x01c0 204C	-	Reserved
0x01c0 2050	IER	Interrupt Enable Register
0x01c0 2054	IERH	Interrupt Enable Register High
0x01c0 2058	IECR	Interrupt Enable Clear Register
0x01c0 205C	IECRH	Interrupt Enable Clear Register High
0x01c0 2060	IESR	Interrupt Enable Set Register
0x01c0 2064	IESRH	Interrupt Enable Set Register High
0x01c0 2068	IPR	Interrupt Pending Register
0x01c0 206C	IPRH	Interrupt Pending Register High
0x01c0 2070	ICR	Interrupt Clear Register
0x01c0 2074	ICRH	Interrupt Clear Register High
0x01c0 2078	IEVAL	Interrupt Evaluate Register
0x01c0 207C	-	Reserved
0x01c0 2080	QER	QDMA Event Register
0x01c0 2084	QEER	QDMA Event Enable Register
0x01c0 2088	QEECR	QDMA Event Enable Clear Register
0x01c0 208C	QEESR	QDMA Event Enable Set Register
0x01c0 2090	QSER	QDMA Secondary Event Register
0x01c0 2094	QSECR	QDMA Secondary Event Clear Register
0x01c0 2098 - 0x01c0 21FC	-	Reserved
Shadow Region 1 Channel Registers		
0x01c0 2200	ER	Event Register
0x01c0 2204	ERH	Event Register High
0x01c0 2208	ECR	Event Clear Register
0x01c0 220C	ECRH	Event Clear Register High
0x01c0 2210	ESR	Event Set Register
0x01c0 2214	ESRH	Event Set Register High
0x01c0 2218	CER	Chained Event Register
0x01c0 221C	CERH	Chained Event Register High
0x01c0 2220	EER	Event Enable Register
0x01c0 2224	EERH	Event Enable Register High
0x01c0 2228	EECR	Event Enable Clear Register
0x01c0 222C	EECRH	Event Enable Clear Register High
0x01c0 2230	EESR	Event Enable Set Register
0x01c0 2234	EESRH	Event Enable Set Register High
0x01c0 2238	SER	Secondary Event Register

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Table 5-26. DM6446 EDMA Registers (continued)

HEX ADDRESS	ACRONYM	REGISTER NAME
0x01c0 223C	SERH	Secondary Event Register High
0x01c0 2240	SECR	Secondary Event Clear Register
0x01c0 2244	SECRH	Secondary Event Clear Register High
0x01c0 2248	-	Reserved
0x01c0 224C	-	Reserved
0x01c0 2250	IER	Interrupt Enable Register
0x01c0 2254	IERH	Interrupt Enable Register High
0x01c0 2258	IECR	Interrupt Enable Clear Register
0x01c0 225C	IECRH	Interrupt Enable Clear Register High
0x01c0 2260	IESR	Interrupt Enable Set Register
0x01c0 2264	IESRH	Interrupt Enable Set Register High
0x01c0 2268	IPR	Interrupt Pending Register
0x01c0 226C	IPRH	Interrupt Pending Register High
0x01c0 2270	ICR	Interrupt Clear Register
0x01c0 2274	ICRH	Interrupt Clear Register High
0x01c0 2278	IEVAL	Interrupt Evaluate Register
0x01c0 227C	-	Reserved
0x01c0 2280	QER	QDMA Event Register
0x01c0 2284	QEER	QDMA Event Enable Register
0x01c0 2288	QEECR	QDMA Event Enable Clear Register
0x01c0 228C	QEESR	QDMA Event Enable Set Register
0x01c0 2290	QSER	QDMA Secondary Event Register
0x01c0 2294	QSECR	QDMA Secondary Event Clear Register
0x01c0 2298 - 0x01c0 23FC	-	Reserved
Shadow Region 2 Channel Registers		
0x01c0 2400	ER	Event Register
0x01c0 2404	ERH	Event Register High
0x01c0 2408	ECR	Event Clear Register
0x01c0 240C	ECRH	Event Clear Register High
0x01c0 2410	ESR	Event Set Register
0x01c0 2414	ESRH	Event Set Register High
0x01c0 2418	CER	Chained Event Register
0x01c0 241C	CERH	Chained Event Register High
0x01c0 2420	EER	Event Enable Register
0x01c0 2424	EERH	Event Enable Register High
0x01c0 2428	EECR	Event Enable Clear Register
0x01c0 242C	EECRH	Event Enable Clear Register High
0x01c0 2430	EESR	Event Enable Set Register
0x01c0 2434	EESRH	Event Enable Set Register High
0x01c0 2438	SER	Secondary Event Register
0x01c0 243C	SERH	Secondary Event Register High
0x01c0 2440	SECR	Secondary Event Clear Register
0x01c0 2444	SECRH	Secondary Event Clear Register High
0x01c0 2448	-	Reserved
0x01c0 244C	-	Reserved
0x01c0 2450	IER	Interrupt Enable Register
0x01c0 2454	IERH	Interrupt Enable Register High

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Table 5-26. DM6446 EDMA Registers (continued)

HEX ADDRESS	ACRONYM	REGISTER NAME
0x01c0 2458	IECR	Interrupt Enable Clear Register
0x01c0 245C	IECRH	Interrupt Enable Clear Register High
0x01c0 2460	IESR	Interrupt Enable Set Register
0x01c0 2464	IESRH	Interrupt Enable Set Register High
0x01c0 2468	IPR	Interrupt Pending Register
0x01c0 246C	IPRH	Interrupt Pending Register High
0x01c0 2470	ICR	Interrupt Clear Register
0x01c0 2474	ICRH	Interrupt Clear Register High
0x01c0 2478	IEVAL	Interrupt Evaluate Register
0x01c0 247C	-	Reserved
0x01c0 2480	QER	QDMA Event Register
0x01c0 2484	QEER	QDMA Event Enable Register
0x01c0 2488	QEECR	QDMA Event Enable Clear Register
0x01c0 248C	QEESR	QDMA Event Enable Set Register
0x01c0 2490	QSER	QDMA Secondary Event Register
0x01c0 2494	QSECR	QDMA Secondary Event Clear Register
0x01c0 2498 - 0x01c0 25FC	-	Reserved
Shadow Region 3 Channel Registers		
0x01c0 2600	ER	Event Register
0x01c0 2604	ERH	Event Register High
0x01c0 2608	ECR	Event Clear Register
0x01c0 260C	ECRH	Event Clear Register High
0x01c0 2610	ESR	Event Set Register
0x01c0 2614	ESRH	Event Set Register High
0x01c0 2618	CER	Chained Event Register
0x01c0 261C	CERH	Chained Event Register High
0x01c0 2620	EER	Event Enable Register
0x01c0 2624	EERH	Event Enable Register High
0x01c0 2628	EECR	Event Enable Clear Register
0x01c0 262C	EECRH	Event Enable Clear Register High
0x01c0 2630	EESR	Event Enable Set Register
0x01c0 2634	EESRH	Event Enable Set Register High
0x01c0 2638	SER	Secondary Event Register
0x01c0 263C	SERH	Secondary Event Register High
0x01c0 2640	SECR	Secondary Event Clear Register
0x01c0 2644	SECRH	Secondary Event Clear Register High
0x01c0 2648	-	Reserved
0x01c0 264C	-	Reserved
0x01c0 2650	IER	Interrupt Enable Register
0x01c0 2654	IERH	Interrupt Enable Register High
0x01c0 2658	IECR	Interrupt Enable Clear Register
0x01c0 265C	IECRH	Interrupt Enable Clear Register High
0x01c0 2660	IESR	Interrupt Enable Set Register
0x01c0 2664	IESRH	Interrupt Enable Set Register High
0x01c0 2668	IPR	Interrupt Pending Register
0x01c0 266C	IPRH	Interrupt Pending Register High
0x01c0 2670	ICR	Interrupt Clear Register

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Table 5-26. DM6446 EDMA Registers (continued)

HEX ADDRESS	ACRONYM	REGISTER NAME
0x01c0 2674	ICRH	Interrupt Clear Register High
0x01c0 2678	IEVAL	Interrupt Evaluate Register
0x01c0 267C	-	Reserved
0x01c0 2680	QER	QDMA Event Register
0x01c0 2684	QEER	QDMA Event Enable Register
0x01c0 2688	QEECR	QDMA Event Enable Clear Register
0x01c0 268C	QEESR	QDMA Event Enable Set Register
0x01c0 2690	QSER	QDMA Secondary Event Register
0x01c0 2694	QSECR	QDMA Secondary Event Clear Register
0x01c0 2698 - 0x01c0 27FC	-	Reserved
0x01c0 2800 - 0x01c0 29FC	-	Reserved
0x01c0 2A00 - 0x01c0 2BFC	-	Reserved
0x01c0 2C00 - 0x01c0 2DFC	-	Reserved
0x01c0 2E00 - 0x01c0 2FFC	-	Reserved
0x01c0 2FFD - 0x01c0 3FFF	-	Reserved
0x01c0 4000 - 0x01c0 4FFF	-	Parameter Set RAM (see Table 5-27)
0x01c0 5000 - 0x01c0 7FFF	-	Reserved
0x01c0 8000 - 0x01c0 FFFF	-	Reserved
Transfer Controller 0 Registers		
0x01c1 0000	-	Reserved
0x01c1 0004	TCCFG	EDMA3 TC0 Configuration Register
0x01c1 0008 - 0x01c1 00FF	-	Reserved
0x01c1 0100	TCSTAT	EDMA3 TC0 Channel Status Register
0x01c1 0104 - 0x01c1 0110	-	Reserved
0x01c1 0114 - 0x01c1 011F	-	Reserved
0x01c1 0120	ERRSTAT	EDMA3 TC0 Error Status Register
0x01c1 0124	ERREN	EDMA3 TC0 Error Enable Register
0x01c1 0128	ERRCLR	EDMA3 TC0 Error Clear Register
0x01c1 012C	ERRDET	EDMA3 TC0 Error Details Register
0x01c1 0130	ERRCMD	EDMA3 TC0 Error Interrupt Command Register
0x01c1 0134 - 0x01c1 013F	-	Reserved
0x01c1 0140	RDRATE	EDMA3 TC0 Read Rate Register
0x01c1 0144 - 0x01c1 01FF	-	Reserved
0x01c1 0200 - 0x01c1 023F	-	Reserved
0x01c1 0240	SAOPT	EDMA3 TC0 Source Active Options Register
0x01c1 0244	SASRC	EDMA3 TC0 Source Active Source Address Register
0x01c1 0248	SACNT	EDMA3 TC0 Source Active Count Register
0x01c1 024C	SADST	EDMA3 TC0 Source Active Destination Address Register
0x01c1 0250	SABIDX	EDMA3 TC0 Source Active Source B-Index Register
0x01c1 0254	SAMPPRXY	EDMA3 TC0 Source Active Memory Protection Proxy Register
0x01c1 0258	SACNTRLD	EDMA3 TC0 Source Active Count Reload Register
0x01c1 025C	SASRCBREF	EDMA3 TC0 Source Active Source Address B-Reference Register
0x01c1 0260	SADSTBREF	EDMA3 TC0 Source Active Destination Address B-Reference Register
0x01c1 0264 - 0x01c1 027F	-	Reserved
0x01c1 0280	DFCNTRLD	EDMA3 TC0 Destination FIFO Set Count Reload Register
0x01c1 0284	DFSRCBREF	EDMA3 TC0 Destination FIFO Set Source Address B-Reference Register

Table 5-26. DM6446 EDMA Registers (continued)

HEX ADDRESS	ACRONYM	REGISTER NAME
0x01c1 0288	DFDSTBREF	EDMA3 TC0 Destination FIFO Set Destination Address B-Reference Register
0x01c1 028C - 0x01c1 02FF	-	Reserved
0x01c1 0300	DFOPT0	EDMA3 TC0 Destination FIFO Options Register 0
0x01c1 0304	DFSRC0	EDMA3 TC0 Destination FIFO Source Address Register 0
0x01c1 0308	DFCNT0	EDMA3 TC0 Destination FIFO Count Register 0
0x01c1 030C	DFDST0	EDMA3 TC0 Destination FIFO Destination Address Register 0
0x01c1 0310	DFBIDX0	EDMA3 TC0 Destination FIFO BIDX Register 0
0x01c1 0314	DFMPPRXY0	EDMA3 TC0 Destination FIFO Memory Protection Proxy Register 0
0x01c1 0318 - 0x01c1 033F	-	Reserved
0x01c1 0340	DFOPT1	EDMA3 TC0 Destination FIFO Options Register 1
0x01c1 0344	DFSRC1	EDMA3 TC0 Destination FIFO Source Address Register 1
0x01c1 0348	DFCNT1	EDMA3 TC0 Destination FIFO Count Register 1
0x01c1 034C	DFDST1	EDMA3 TC0 Destination FIFO Destination Address Register 1
0x01c1 0350	DFBIDX1	EDMA3 TC0 Destination FIFO BIDX Register 1
0x01c1 0354	DFMPPRXY1	EDMA3 TC0 Destination FIFO Memory Protection Proxy Register 1
0x01c1 0358 - 0x01c1 037F	-	Reserved
0x01c1 0380	DFOPT2	EDMA3 TC0 Destination FIFO Options Register 2
0x01c1 0384	DFSRC2	EDMA3 TC0 Destination FIFO Source Address Register 2
0x01c1 0388	DFCNT2	EDMA3 TC0 Destination FIFO Count Register 2
0x01c1 038C	DFDST2	EDMA3 TC0 Destination FIFO Destination Address Register 2
0x01c1 0390	DFBIDX2	EDMA3 TC0 Destination FIFO BIDX Register 2
0x01c1 0394	DFMPPRXY2	EDMA3 TC0 Destination FIFO Memory Protection Proxy Register 2
0x01c1 0398 - 0x01c1 03BF	-	Reserved
0x01c1 03C0	DFOPT3	EDMA3 TC0 Destination FIFO Options Register 3
0x01c1 03C4	DFSRC3	EDMA3 TC0 Destination FIFO Source Address Register 3
0x01c1 03C8	DFCNT3	EDMA3 TC0 Destination FIFO Count Register 3
0x01c1 03CC	DFDST3	EDMA3 TC0 Destination FIFO Destination Address Register 3
0x01c1 03D0	DFBIDX3	EDMA3 TC0 Destination FIFO BIDX Register 3
0x01c1 03D4	DFMPPRXY3	EDMA3 TC0 Destination FIFO Memory Protection Proxy Register 3
0x01c1 03D8 - 0x01c1 03FF	-	Reserved
Transfer Controller 1 Registers		
0x01c1 0400	-	Reserved
0x01c1 0404	TCCFG	EDMA3 TC1 Configuration Register
0x01c1 0408 - 0x01c1 04FF	-	Reserved
0x01c1 0500	TCSTAT	EDMA3 TC1 Channel Status Register
0x01c1 0504 - 0x01c1 0510	-	Reserved
0x01c1 0514 - 0x01c1 051F	-	Reserved
0x01c1 0520	ERRSTAT	EDMA3 TC1 Error Status Register
0x01c1 0524	ERREN	EDMA3 TC1 Error Enable Register
0x01c1 0528	ERRCLR	EDMA3 TC1 Error Clear Register
0x01c1 052C	ERRDET	EDMA3 TC1 Error Details Register
0x01c1 0530	ERRCMD	EDMA3 TC1 Error Interrupt Command Register
0x01c1 0534 - 0x01c1 053F	-	Reserved
0x01c1 0540	RDRATE	EDMA3 TC1 Read Rate Register
0x01c1 0544 - 0x01c1 05FF	-	Reserved
0x01c1 0600 - 0x01c1 063F	-	Reserved

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Table 5-26. DM6446 EDMA Registers (continued)

HEX ADDRESS	ACRONYM	REGISTER NAME
0x01c1 0640	SAOPT	EDMA3 TC1 Source Active Options Register
0x01c1 0644	SASRC	EDMA3 TC1 Source Active Source Address Register
0x01c1 0648	SACNT	EDMA3 TC1 Source Active Count Register
0x01c1 064C	SADST	EDMA3 TC1 Source Active Destination Address Register
0x01c1 0650	SABIDX	EDMA3 TC1 Source Active Source B-Index Register
0x01c1 0654	SAMPPRXY	EDMA3 TC1 Source Active Memory Protection Proxy Register
0x01c1 0658	SACNTRLD	EDMA3 TC1 Source Active Count Reload Register
0x01c1 065C	SASRCBREF	EDMA3 TC1 Source Active Source Address B-Reference Register
0x01c1 0660	SADSTBREF	EDMA3 TC1 Source Active Destination Address B-Reference Register
0x01c1 0664 - 0x01c1 067F	-	Reserved
0x01c1 0680	DFCNTRLD	EDMA3 TC1 Destination FIFO Set Count Reload Register
0x01c1 0684	DFSRCBREF	EDMA3 TC1 Destination FIFO Set Source Address B-Reference Register
0x01c1 0688	DFDSTBREF	EDMA3 TC1 Destination FIFO Set Destination Address B-Reference Register
0x01c1 068C - 0x01c1 06FF	-	Reserved
0x01c1 0700	DFOPT0	EDMA3 TC1 Destination FIFO Options Register 0
0x01c1 0704	DFSRC0	EDMA3 TC1 Destination FIFO Source Address Register 0
0x01c1 0708	DFCNT0	EDMA3 TC1 Destination FIFO Count Register 0
0x01c1 070C	DFDST0	EDMA3 TC1 Destination FIFO Destination Address Register 0
0x01c1 0710	DFBIDX0	EDMA3 TC1 Destination FIFO BIDX Register 0
0x01c1 0714	DFMPPRXY0	EDMA3 TC1 Destination FIFO Memory Protection Proxy Register 0
0x01c1 0718 - 0x01c1 073F	-	Reserved
0x01c1 0740	DFOPT1	EDMA3 TC1 Destination FIFO Options Register 1
0x01c1 0744	DFSRC1	EDMA3 TC1 Destination FIFO Source Address Register 1
0x01c1 0748	DFCNT1	EDMA3 TC1 Destination FIFO Count Register 1
0x01c1 074C	DFDST1	EDMA3 TC1 Destination FIFO Destination Address Register 1
0x01c1 0750	DFBIDX1	EDMA3 TC1 Destination FIFO BIDX Register 1
0x01c1 0754	DFMPPRXY1	EDMA3 TC1 Destination FIFO Memory Protection Proxy Register 1
0x01c1 0758 - 0x01c1 077F	-	Reserved
0x01c1 0780	DFOPT2	EDMA3 TC1 Destination FIFO Options Register 2
0x01c1 0784	DFSRC2	EDMA3 TC1 Destination FIFO Source Address Register 2
0x01c1 0788	DFCNT2	EDMA3 TC1 Destination FIFO Count Register 2
0x01c1 078C	DFDST2	EDMA3 TC1 Destination FIFO Destination Address Register 2
0x01c1 0790	DFBIDX2	EDMA3 TC1 Destination FIFO BIDX Register 2
0x01c1 0794	DFMPPRXY2	EDMA3 TC1 Destination FIFO Memory Protection Proxy Register 2
0x01c1 0798 - 0x01c1 07BF	-	Reserved
0x01c1 07C0	DFOPT3	EDMA3 TC1 Destination FIFO Options Register 3
0x01c1 07C4	DFSRC3	EDMA3 TC1 Destination FIFO Source Address Register 3
0x01c1 07C8	DFCNT3	EDMA3 TC1 Destination FIFO Count Register 3
0x01c1 07CC	DFDST3	EDMA3 TC1 Destination FIFO Destination Address Register 3
0x01c1 07D0	DFBIDX3	EDMA3 TC1 Destination FIFO BIDX Register 3
0x01c1 07D4	DFMPPRXY3	EDMA3 TC1 Destination FIFO Memory Protection Proxy Register 3
0x01c1 07D8 - 0x01c1 07FF	-	Reserved

Table 5-27 shows an abbreviation of the set of registers which make up the parameter set for each of 128 EDMA events. Each of the parameter register sets consist of 8 32-bit word entries. Table 5-28 shows the parameter set entry registers with relative memory address locations within each of the parameter sets.

Table 5-27. EDMA Parameter Set RAM

HEX ADDRESS RANGE	DESCRIPTION
0x01c0 4000 - 0x01c0 401F	Parameters Set 0 (8 32-bit words)
0x01c0 4020 - 0x01c0 403F	Parameters Set 1 (8 32-bit words)
0x01c0 4040 - 0x01c0 405F	Parameters Set 2 (8 32-bit words)
0x01c0 4060 - 0x01c0 407F	Parameters Set 3 (8 32-bit words)
0x01c0 4080 - 0x01c0 409F	Parameters Set 4 (8 32-bit words)
0x01c0 40A0 - 0x01c0 40BF	Parameters Set 5 (8 32-bit words)
...	...
0x01c0 4FC0 - 0x01c0 4FDF	Parameters Set 127 (8 32-bit words)
0x01c0 4FE0 - 0x01c0 4FFF	Parameters Set 128 (8 32-bit words)

Table 5-28. Parameter Set Entries

HEX OFFSET ADDRESS WITHIN THE PARAMETER SET	ACRONYM	PARAMETER ENTRY
0x0000	OPT	Option
0x0004	SRC	Source Address
0x0008	A_B_CNT	A Count, B Count
0x000C	DST	Destination Address
0x0010	SRC_DST_BIDX	Source B Index, Destination B Index
0x0014	LINK_BCNTRLD	Link Address, B Count Reload
0x0018	SRC_DST_CIDX	Source C Index, Destination C Index
0x001C	CCNT	C Count

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5.10 External Memory Interface (EMIF)

DM6446 supports several memory and external device interfaces, including:

- Asynchronous EMIF (EMIFA) for interfacing to NOR Flash, SRAM, etc.
- NAND Flash
- ATA/CF

5.10.1 Asynchronous EMIF (EMIFA)

The DM6446 Asynchronous EMIF (EMIFA) provides an 8-bit or 16-bit data bus, an address bus width up to 24-bits, and 4 dedicated chip selects, along with memory control signals. These signals are multiplexed between three peripherals:

- EMIFA and NAND interfaces
- ATA/CF
- Host Port Interface

5.10.1.1 NAND (NAND, SmartMedia, xD)

The EMIFA interface provides both the asynchronous EMIF and NAND interfaces. Four chip selects are provided and each are individually configurable to provide either EMIFA or NAND support. The NAND features supported are as follows.

- NAND flash on up to 4 asynchronous chip selects.
- 8 and 16-bit data bus widths.
- Programmable cycle timings.
- Performs ECC calculation.
- NAND Mode also supports SmartMedia/SSFDC (Solid State Floppy Disk Controller) and xD memory cards
- ARM ROM supports booting of the DM6446 ARM processor from NAND flash located at CS0

The memory map for EMIFA and NAND registers is shown in Table 5-29. For more details on the EMIFA and NAND interfaces, see the *Documentation Support* for the DM6446 Asynchronous External Memory Interface (EMIF) User's Guide.

Table 5-29. EMIFA/NAND Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01E0 0000 - 0x01E0 0003		Reserved
0x01E0 0004	AWCCR	Asynchronous Wait Cycle Configuration Register
0x01E0 0008 - 0x01E0 000F		Reserved
0x01E0 0010	A1CR	Asynchronous 1 Configuration Register (CS2 Space)
0x01E0 0014	A2CR	Asynchronous 2 Configuration Register (CS3 Space)
0x01E0 0018	A3CR	Asynchronous 3 Configuration Register (CS4 Space)
0x01E0 001C	A4CR	Asynchronous 4 Configuration Register (CS5 Space)
0x01E0 0020 - 0x01E0 003F	-	Reserved
0x01E0 0040	EIRR	EMIF Interrupt Raw Register
0x01E0 0044	EIMR	EMIF Interrupt Mask Register
0x01E0 0048	EIMSR	EMIF Interrupt Mask Set Register
0x01E0 004C	EIMCR	EMIF Interrupt Mask Clear Register
0x01E0 0050 - 0x01E0 005F	-	Reserved
0x01E0 0060	NANDFCR	NAND Flash Control Register
0x01E0 0064	NANDFSR	NAND Flash Status Register
0x01E0 0070	NANDF1ECC	NAND Flash 1 ECC Register (CS2 Space)
0x01E0 0074	NANDF2ECC	NAND Flash 2 ECC Register (CS3 Space)

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Table 5-29. EMIFA/NAND Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01E0 0078	NANDF3ECC	NAND Flash 3 ECC Register (CS4 Space)
0x01E0 007C	NANDF4ECC	NAND Flash 4 ECC Register (CS5 Space)
0x01E0 0080 - 0x01E0 0FFF	-	Reserved

5.10.1.2 EMIFA Electrical Data/Timing

Table 5-30. Timing Requirements for Asynchronous Memory Cycles for EMIFA Module(1)(2) (see Figure 5-17 and Figure 5-18)

NO.			-594		UNIT
			MIN	MAX	
READS and WRITES					
2	$t_{w(EM\_WAIT)}$	Pulse duration, EM_WAIT assertion and deassertion	2E ± TBD		ns
READS					
12	$t_{su(EMDV-EMOEH)}$	Setup time, EM_D[15:0] valid before EM_OE high	E		ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EM_D[15:0] valid after EM_OE high	0		ns
14	$t_{d(EMOEL-EMWAIT)}$	Delay time from EM_OE low to EM_WAIT asserted	(RST-2) * E - TBD		ns
WRITES					
28	$t_{d(EMWEL-EMWAIT)}$	Delay time from EM_WE low to EM_WAIT asserted	(WST-2) * E - TBD		ns

(1) RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEW = Maximum External Wait. These parameters are programmed via the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers.
(2) E = 6 x DSP period in ns for EMIFA. For example, when running the DSP CPU at 594 MHz, use E = 10.1 ns.

Table 5-31. Switching Characteristics Over Recommended Operating Conditions for Asynchronous Memory Cycles for EMIFA Module(1)(2) (see Figure 5-17 and Figure 5-18)

NO.	PARAMETER		-594		UNIT
			MIN	MAX	
READS and WRITES					
1	$t_{d(TURNAROUND)}$	Turn around time	0	(TA + 1) * E ± TBD	ns
READS					
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)	3E ± TBD	92 * E ± TBD	ns
		EMIF read cycle time (EW = 1)	3E ± TBD	4188 * E ± TBD	ns
4	$t_{su(EMCSL-EMOEL)}$	Output setup time, EM_CS[5:2] low to EM_OE low (SS = 0)	E ± TBD	(RS + 1) * E ± TBD	ns
		Output setup time, EM_CS[5:2] low to EM_OE low (SS = 1)	0		ns
5	$t_{h(EMOEH-EMCSH)}$	Output hold time, EM_OE high to EM_CS[5:2] high (SS = 0)	E ± TBD	(RH + 1) * E ± TBD	ns
		Output hold time, EM_OE high to EM_CS[5:2] high (SS = 1)	0		ns
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, EM_BA[1:0] valid to EM_OE low	E ± TBD	(RS + 1) * E ± TBD	ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, EM_OE high to EM_BA[1:0] invalid	E ± TBD	(RH + 1) * E ± TBD	ns
8	$t_{su(EMBAV-EMOEL)}$	Output setup time, EM_A[21:0] valid to EM_OE low	E ± TBD	(RS + 1) * E ± TBD	ns
9	$t_{h(EMOEH-EMBAIV)}$	Output hold time, EM_OE high to EM_A[21:0] invalid	E ± TBD	(RH + 1) * E ± TBD	ns

(1) RS = Read setup, RST = Read STrobe, RH = Read Hold, WS = Write Setup, WST = Write STrobe, WH = Write Hold, TA = Turn Around, EW = Extend Wait mode, SS = Select Strobe mode. These parameters are programmed via the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers.
(2) E = 6 x DSP period in ns for EMIFA. For example, when running the DSP CPU at 594 MHz, use E = 10.1 ns.

Table 5-31. Switching Characteristics Over Recommended Operating Conditions for Asynchronous Memory Cycles for EMIFA Module (see Figure 5-17 and Figure 5-18) (continued)

NO.	PARAMETER		-594 MIN	-594 MAX	UNIT
10	$t_{w(EMOEL)}$	$\overline{EM\_OE}$ active low width (EW = 0)	E ± TBD	(RST + 1) * E ± TBD	ns
		$\overline{EM\_OE}$ active low width (EW = 1)	3E ± TBD	(RST + 4087) * E ± TBD	ns
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EM_WAIT deasserted to $\overline{EM\_OE}$ high		4E ± TBD	ns
		WRITES			
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)	3E ± TBD	92 * E ± TBD	ns
		EMIF write cycle time (EW = 1)	3E ± TBD	4188 * E ± TBD	ns
16	$t_{su(EMCSL-EMWEL)}$	Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_WE}$ low (SS = 0)	E ± TBD	(WS + 1) * E ± TBD	ns
		Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_WE}$ low (SS = 1)	0		ns
17	$t_{h(EMWEH-EMCSH)}$	Output hold time, $\overline{EM\_WE}$ high to $\overline{EM\_CS[5:2]}$ high (SS = 0)	E ± TBD	(WH + 1) * E ± TBD	ns
		Output hold time, $\overline{EM\_WE}$ high to $\overline{EM\_CS[5:2]}$ high (SS = 1)	0		ns
18	$t_{su(EMRNW-EMWEL)}$	Output setup time, EM_R/$\overline{W}$ valid to $\overline{EM\_WE}$ low	E ± TBD	(WS + 1) * E ± TBD	ns
19	$t_{h(EMWEH-EMRNW)}$	Output hold time, $\overline{EM\_WE}$ high to EM_R/$\overline{W}$ invalid	E ± TBD	(WH + 1) * E ± TBD	ns
20	$t_{su(EMBAV-EMWEL)}$	Output setup time, $\overline{EM\_BA[1:0]}$ valid to $\overline{EM\_WE}$ low	E ± TBD	(WS + 1) * E ± TBD	ns
21	$t_{h(EMWEH-EMBAIV)}$	Output hold time, $\overline{EM\_WE}$ high to $\overline{EM\_BA[1:0]}$ invalid	E ± TBD	(WH + 1) * E ± TBD	ns
22	$t_{su(EMAV-EMWEL)}$	Output setup time, $\overline{EM\_A[21:0]}$ valid to $\overline{EM\_WE}$ low	E ± TBD	(WS + 1) * E ± TBD	ns
23	$t_{h(EMWEH-EMAIV)}$	Output hold time, $\overline{EM\_WE}$ high to $\overline{EM\_A[21:0]}$ invalid	E ± TBD	(WH + 1) * E ± TBD	ns
24	$t_{w(EMWEL)}$	$\overline{EM\_WE}$ active low width (EW = 0)	E ± TBD	(WST + 1) * E ± TBD	ns
		$\overline{EM\_WE}$ active low width (EW = 1)	3E ± TBD	(WST + 4097) * E ± TBD	
25	$t_{d(EMWAITH-EMWEH)}$	Delay time from EM_WAIT deasserted to $\overline{EM\_WE}$ high		4E ± TBD	ns
26	$t_{su(EMDV-EMWEL)}$	Output setup time, $\overline{EM\_D[15:0]}$ valid to $\overline{EM\_WE}$ low	E ± TBD	(WS + 1) * E ± TBD	ns
27	$t_{h(EMWEH-EMDIV)}$	Output hold time, $\overline{EM\_WE}$ high to $\overline{EM\_D[15:0]}$ invalid	E ± TBD	(WH + 1) * E ± TBD	ns

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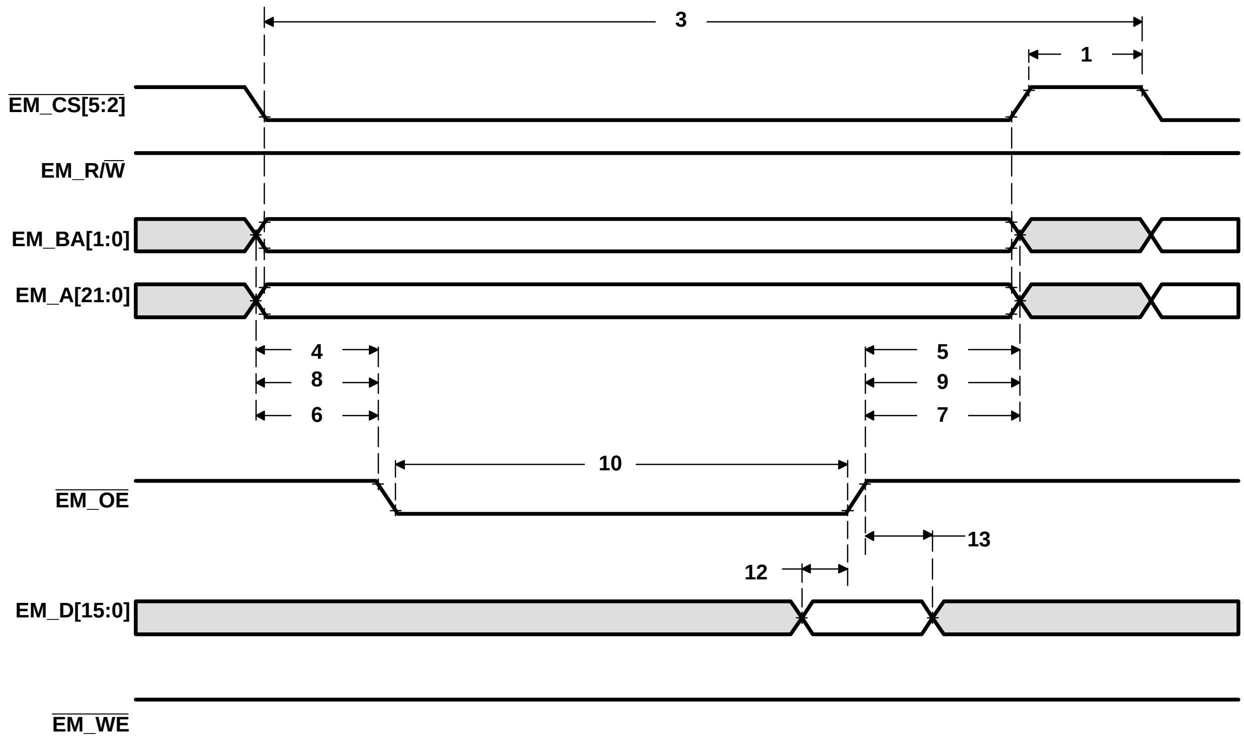

Figure 5-17. Asynchronous Memory Read Timing for EMIF

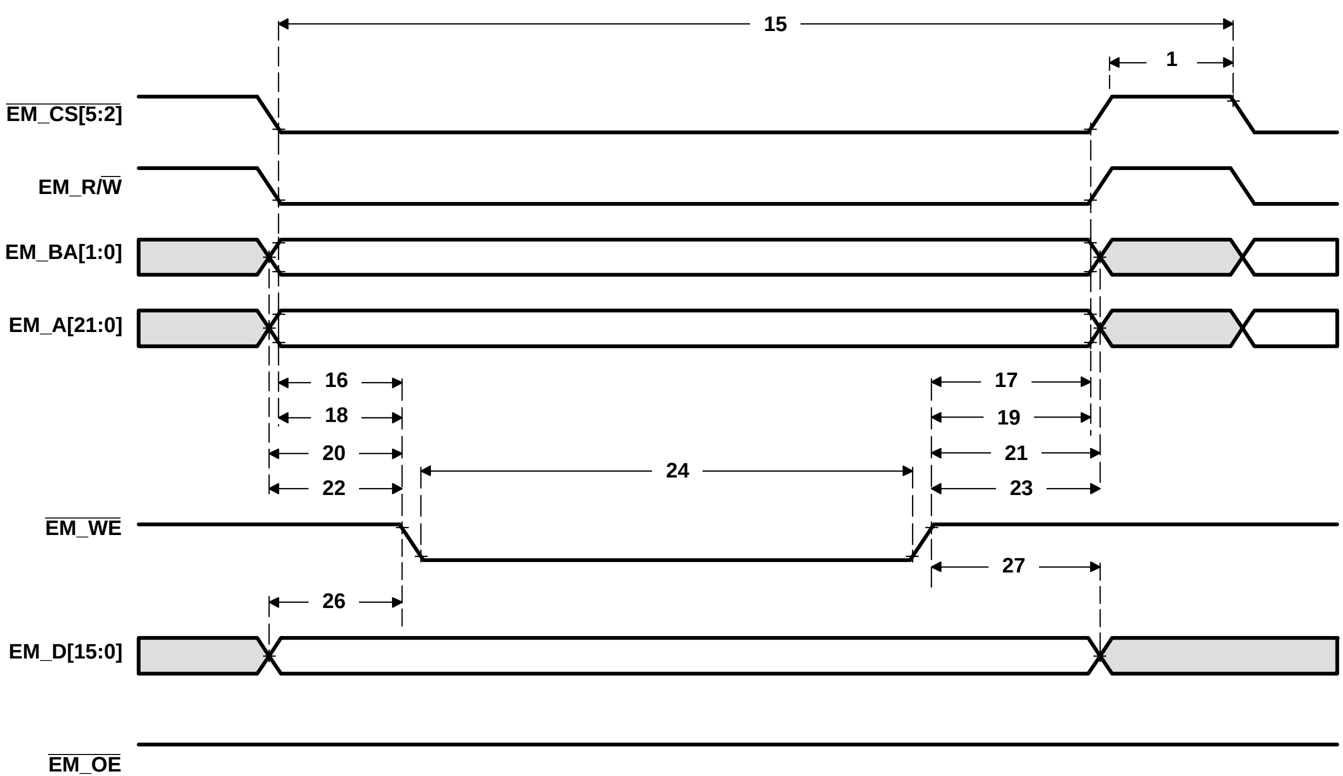

Figure 5-18. Asynchronous Memory Write Timing for EMIF

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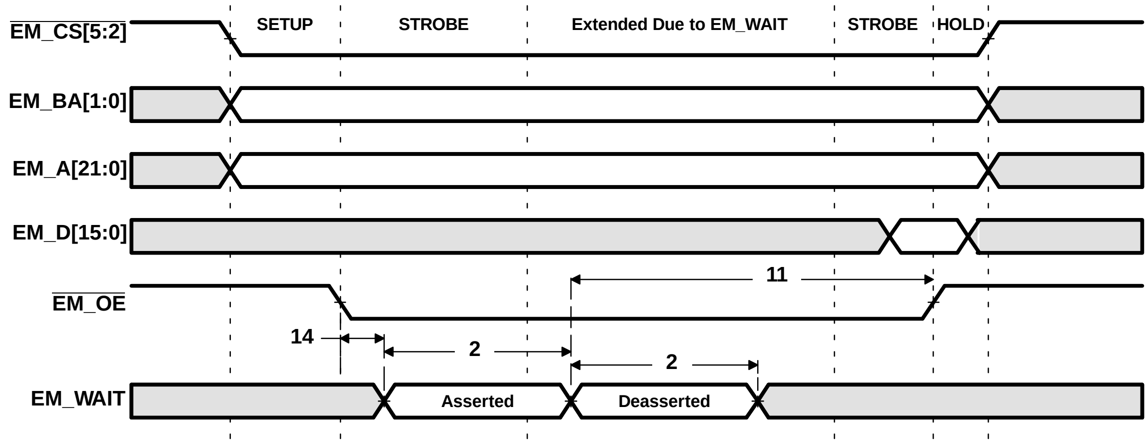

Figure 5-19. EM_WAIT Read Timing Requirements

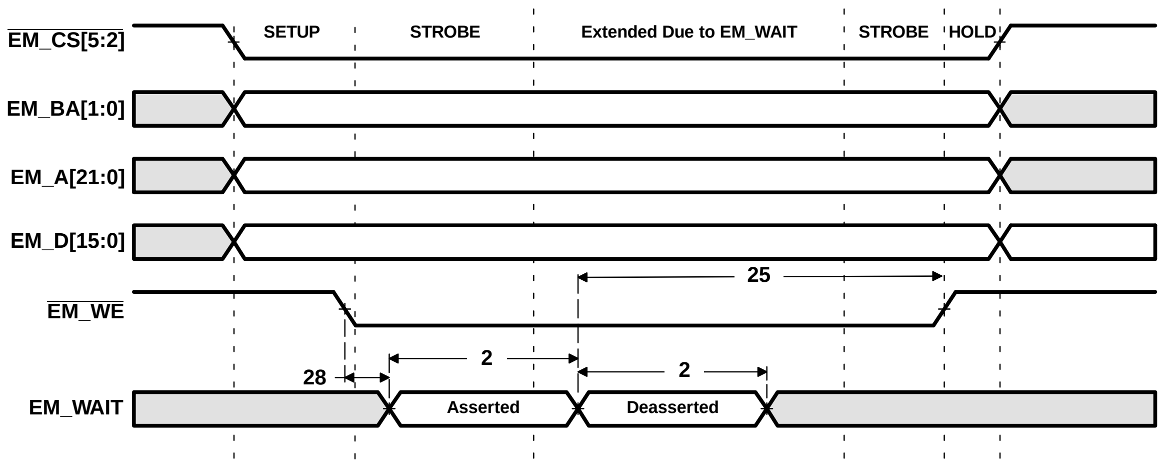

Figure 5-20. EM_WAIT Write Timing Requirements

5.10.2 DDR2 Memory Controller

The DDR2 Memory Controller is a dedicated interface to DDR2 SDRAM. It supports JESD79D-2A standard compliant DDR2 SDRAM Devices and can interface to either 16-bit or 32-bit DDR2 SDRAM devices. For details on the DDR2 Memory Controller, see the *Document Support* section.

DDR2 SDRAM plays a key role in a DaVinci-based system. Such a system is expected to require a significant amount of high-speed external memory for:

- Buffering of input image data from sensors or video sources
- Intermediate buffering for processing/resizing of image data in the VPFE
- Numerous OSD display buffers
- Intermediate buffering for large raw Bayer data image files while performing image processing functions
- Buffering for intermediate data while performing video encode and decode functions
- Storage of executable code for both the ARM and DSP

A memory map of the DDR2 Memory Controller registers is shown in Table 5-32.

Table 5-32. DDR2 Memory Controller Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C4 004C	DDRVTPER	DDR2 VTP Enable Register
0x01C4 2030	DDRVTPR	DDR2 VTP Register
0x2000 0000 - 0x2000 0003	-	Reserved
0x2000 0004	SDRSTAT	SDRAM Status Register
0x2000 0008	SDBCR	SDRAM Bank Configuration Register
0x2000 000C	SDRCR	SDRAM Refresh Control Register
0x2000 0010	SDTIMR	SDRAM Timing Register
0x2000 0014	SDTIMR2	SDRAM Timing Register 2
0x2000 0020	VBPR	Peripheral Bus Burst Priority Register
0x2000 0024 - 0x2000 00BF	-	Reserved
0x2000 00C0	IRR	Interrupt Raw Register
0x2000 00C4	IMR	Interrupt Masked Register
0x2000 00C8	IMSR	Interrupt Mask Set Register
0x2000 00CC	IMCR	Interrupt Mask Clear Register
0x2000 00D0 - 0x2000 00E3	-	Reserved
0x2000 00E4	DDRPHYCR	DDR PHY Control Register
0x2000 00E8 - 0x2000 7FFF	-	Reserved

5.10.2.1 DDR2 Memory Controller Electrical Data/Timing

TI only supports board designs that follow the guidelines outlined in the *Implementing DDR2 PCB Layout on the DM644x DMSoC* application report (literature number SPRAAC5).

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5.11 ATA/CF

The ATA/CF peripheral supports the following features:

- PIO, multiword DMA, and Ultra ATA 33/66/100/133
- Up to mode 4 timings on PIO mode
- Up to mode 2 timings on multiword DMA
- Up to mode 6 timings on Ultra ATA
- Full scatter gather DMA capability
- Can be configured as Primary or Secondary controller
- SpeedSelect feature allows timing parameters to be reprogrammed to support any ATA timing mode at any clock frequency.
- Supports TrueIDE mode for Compact Flash.

In addition, the Host IDE Controller supports multiword DMA and Ultra DMA data transfers between external IDE/ATAPI devices and a system memory bus interface. The ATA timing and control registers are compatible to the Intel register set in the PIIX family. The ATA perpheral has full scatter gather DMA capability, which is compatible with Intel scatter gather DMA function on the PIIX chipset.

5.11.1 ATA/CF Peripheral Register Description(s)

The ATA registers are shown in Table 5-33.

Table 5-33. ATA Register Memory Map

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
		ATA Bus Master Interface DMA Engine Registers
0x01C6 6000	BMICP	Primary IDE Channel DMA Control Register
0x01C6 6002	BMISP	Primary IDE Channel DMA Status Register
0x01C6 6004	BMIDTP	Primary IDE Channel DMA Descriptor Table Pointer Register
0x01C6 6008	-	Reserved
0x01C6 600A	-	Reserved
0x01C6 600C	-	Reserved
		ATA Configuration Registers
0x01C6 6040	IDETIMP	Primary IDE Channel Timing Register
0x01C6 6042	-	Reserved
0x01C6 6044	-	Reserved
0x01C6 6045	-	Reserved
0x01C6 6047	IDESTAT	IDE Controller Status Register
0x01C6 6048	UDMACTL	Ultra-DMA Control Register
0x01C6 604A	-	Reserved
0x01C6 6050	MISCCTL	Miscellaneous Control Register
0x01C6 6054	REGSTB	Task File Register Strobe Timing Register
0x01C6 6058	REGRCVR	Task File Register Recovery Timing Register
0x01C6 605C	DATSTB	Data Register Access PIO Strobe Timing Register
0x01C6 6060	DATRCVR	Data Register Access PIO Recovery Timing Register
0x01C6 6064	DMASTB	Multiword DMA Strobe Timing Register
0x01C6 6068	DMARCVR	Multiword DMA Recovery Timing Register
0x01C6 606C	UDMASTB	Ultra-DMA Strobe Timing Register
0x01C6 6070	UDMATRP	Ultra-DMA Ready-to-Pause Timing Register
0x01C6 6074	UDMATENV	Ultra-DMA Timing Envelope Register
0x01C6 6078	IORDYTMP	Primary IO Ready Timer Configuration Register

ATA Register Memory Map (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C6 607C - 0x01C6 67FF	-	Reserved

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5.11.2 ATA/CF Electrical Data/Timing

5.11.2.1 ATA/CF PIO Data Transfer AC Timing

Table 5-34. Timings for ATA/CF Module --- PIO Data Transfer (see Figure 5-21)

NO.			-594			UNIT
			MODE	MIN	MAX	
1	t_0	Cycle time	0	600		ns
			1	383		ns
			2	240		ns
			3	180		ns
			4	120		ns
2	t_1	Address valid to $\overline{\text{DIOW}}$/ $\overline{\text{DIOR}}$ setup	0	70		ns
			1	50		ns
			2	30		ns
			3	30		ns
			4	25		ns
3	t_2	$\overline{\text{DIOW}}$/ $\overline{\text{DIOR}}$ pulse duration low	0: 16-bit	165		ns
			0: 8-bit	290		
			1: 16-bit	125		ns
			1: 8-bit	290		
			2: 16-bit	100		ns
			2: 8-bit	290		
			3: 16-bit	80		ns
			3: 8-bit	80		
			4: 16-bit	70		ns
			4: 8-bit	70		
4	t_{2i}	$\overline{\text{DIOW}}$/$\overline{\text{DIOR}}$ recovery time, pulse duration high	0	–		ns
			1	–		ns
			2	–		ns
			3	70		ns
			4	25		ns
5	t_3	$\overline{\text{DIOW}}$ data setup time, DD[15:0] valid before $\overline{\text{DIOW}}$ rising edge	0	60		ns
			1	45		ns
			2	30		ns
			3	30		ns
			4	20		ns
6	t_4	$\overline{\text{DIOW}}$ data hold time, DD[15:0] vaild after $\overline{\text{DIOW}}$ rising edge	0	30		ns
			1	20		ns
			2	15		ns
			3	10		ns
			4	10		ns
7	t_5	$\overline{\text{DIOR}}$ data setup time, DD[15:0] valid before $\overline{\text{DIOR}}$ rising edge	0	50		ns
			1	35		ns
			2	20		ns
			3	20		ns
			4	20		ns

Table 5-34. Timings for ATA/CF Module --- PIO Data Transfer (see Figure 5-21) (continued)

NO.			-594			UNIT
			MODE	MIN	MAX	
8	t_6	$\overline{\text{DIOR}}$ data hold time, DD[15:0] valid after $\overline{\text{DIOR}}$ rising edge	0	5		ns
			1	5		ns
			2	5		ns
			3	5		ns
			4	5		ns
9	t_{6Z}	Output data 3-state, DD[15:0] 3-state after $\overline{\text{DIOR}}$ rising edge	0		30	ns
			1		30	ns
			2		30	ns
			3		30	ns
			4		30	ns
10	t_9	$\overline{\text{DIOW}}$/$\overline{\text{DIOR}}$ to address valid hold	0	20		ns
			1	15		ns
			2	10		ns
			3	10		ns
			4	10		ns
11	t_{RD}	Read data setup time, DD[15:0] valid before $\overline{\text{IORDY}}$ active	0	0		ns
			1	0		ns
			2	0		ns
			3	0		ns
			4	0		ns
12	t_A	$\overline{\text{IORDY}}$ setup	0		35	ns
			1		35	ns
			2		35	ns
			3		35	ns
			4		35	ns
13	t_B	$\overline{\text{IORDY}}$ pulse width	0		1250	ns
			1		1250	ns
			2		1250	ns
			3		1250	ns
			4		1250	ns
14	t_C	$\overline{\text{IORDY}}$ assertion to release	0		5	ns
			1		5	ns
			2		5	ns
			3		5	ns
			4		5	ns

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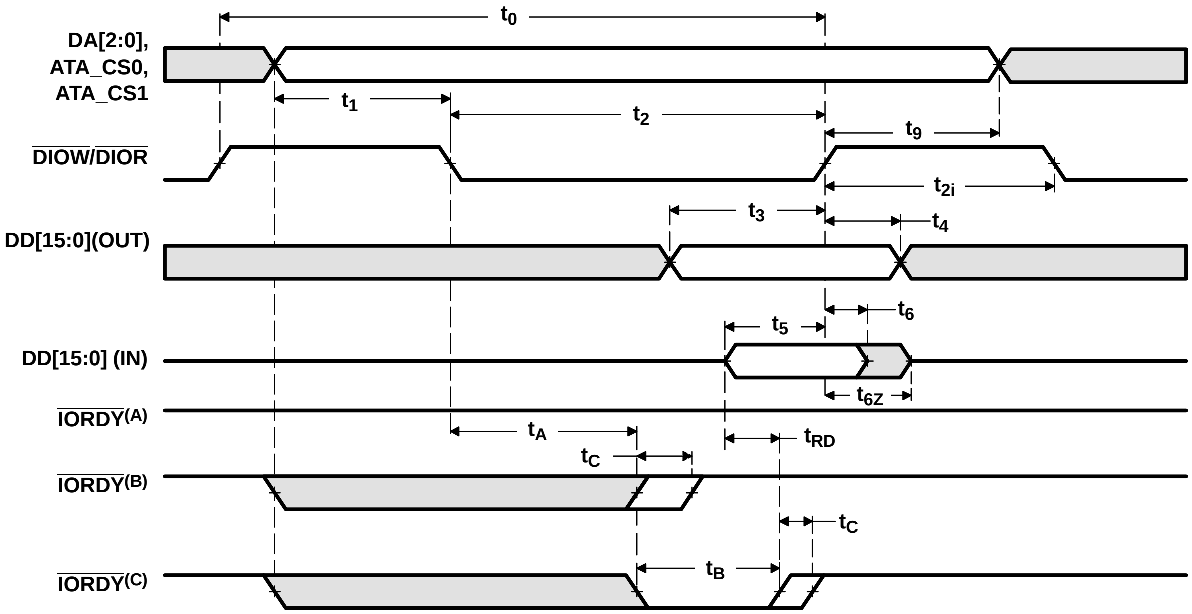

A. $\overline{\text{IORDY}}$ is not negated for transfer (no wait generated)
B. $\overline{\text{IORDY}}$ is negative but is re-assert before t_A (no wait is generated)
C. $\overline{\text{IORDY}}$ is negative before t_A and remains asserted until t_B; data is driven valid at t_{RD} (wait is generated)

Figure 5-21. ATA/CF PIO Data Transfer Timing

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5.11.2.2 ATA/CF Multiword DMA Timing

Table 5-35. Timings for ATA/CF Module --- Multiword DMA AC Timing (see Figure 5-22)

NO.			-594			UNIT
			MODE	MIN	MAX	
1	t_0	Cycle time	0	480		ns
			1	150		ns
			2	120		ns
2	t_D	DIOW/DIOR active low pulse duration	0	215		ns
			1	80		ns
			2	70		ns
3	t_E	DIOR data access, DIOR falling edge to DD[15:0] valid	0		150	ns
			1		60	ns
			2		50	ns
4	t_F	DIOR data hold time, DD[15:0] valid after DIOR rising edge	0	5		ns
			1	5		ns
			2	5		ns
5	t_G	DIOW/DIOR data setup time, DD[15:0] valid before DIOW/DIOR rising edge	0	100		ns
			1	30		ns
			2	20		ns
6	t_H	DIOW data hold time, DD[15:0] valid after DIOW rising edge	0	20		ns
			1	15		ns
			2	10		ns
7	t_I	DMACK to DIOW/DIOR setup	0	0		ns
			1	0		ns
			2	0		ns
8	t_J	DIOW/DIOR to DMACK hold	0	20		ns
			1	5		ns
			2	5		ns
9	t_{KR}	DIOR negated pulse width	0	50		ns
			1	50		ns
			2	25		ns
10	t_{KW}	DIOW negated pulse width	0	215		ns
			1	50		ns
			2	25		ns
11	t_{LR}	DIOR to DMARQ delay	0		120	ns
			1		45	ns
			2		35	ns
12	t_{LW}	DIOW to DMARQ delay	0		40	ns
			1		40	ns
			2		35	ns
13	t_M	ATA_CSx valid to DIOW/DIOR setup	0	50		ns
			1	30		ns
			2	25		ns
14	t_N	ATA_CSx valid after DIOW/DIOR rising edge hold	0	15		ns
			1	10		ns
			2	10		ns

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Table 5-35. Timings for ATA/CF Module --- Multiword DMA AC Timing (see Figure 5-22) (continued)

NO.			-594			UNIT
			MODE	MIN	MAX	
15	t_Z	DMACK to read data (DD[15:0]) released	0	20		ns
			1	25		ns
			2	25		ns

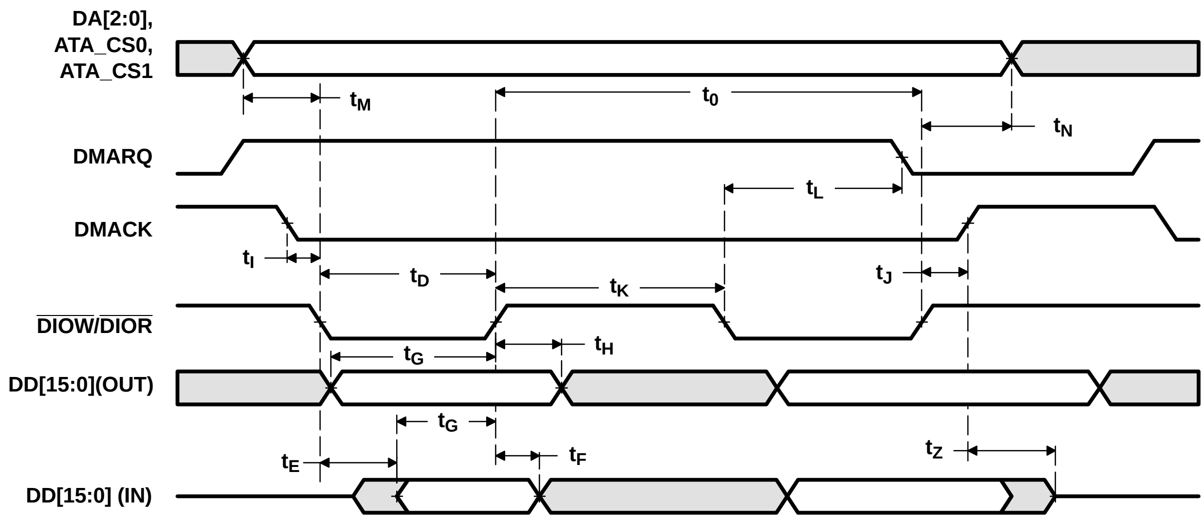

Figure 5-22. ATA/CF Multiword DMA Timing

5.11.2.3 ATA/CF Ultra DMA Timing

Table 5-36. Timings for ATA/CF Module --- Ultra DMA AC Timing (see Figure 5-23 through Figure 5-32)

NO.			-594			UNIT
			MODE	MIN	MAX	
1	$t_{2CYCTYP}$	Typical sustained average two cycle time	0	240		ns
			1	160		ns
			2	120		ns
			3	90		ns
			4	60		ns
2	t_{CYC}	Cycle time, Strobe edge to Strobe edge	0	112		ns
			1	73		ns
			2	54		ns
			3	39		ns
			4	25		ns
3	t_{2CYC}	Two cycle time, rising to rising edge or falling to falling edge	0	230		ns
			1	153		ns
			2	115		ns
			3	86		ns
			4	57		ns
4	t_{DS}	Data setup at recipient, data valid before STROBE edge	0	15		ns
			1	10		ns
			2	7		ns
			3	7		ns
			4	5		ns
5	t_{DH}	Data hold at recipient, data valid after STROBE edge	0	5		ns
			1	5		ns
			2	5		ns
			3	5		ns
			4	5		ns
6	t_{DVS}	Data valid setup time at sender, data valid before STROBE at sender	0	70		ns
			1	48		ns
			2	31		ns
			3	20		ns
			4	6.7		ns
7	t_{DVH}	Data valid hold time at sender, data valid after STROBE at sender	0	6.2		ns
			1	6.2		ns
			2	6.2		ns
			3	6.2		ns
			4	6.2		ns
8	t_{CS}	CRC word setup time at device	0	15		ns
			1	10		ns
			2	7		ns
			3	7		ns
			4	5		ns

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Table 5-36. Timings for ATA/CF Module --- Ultra DMA AC Timing (see Figure 5-23 through Figure 5-32) (continued)

NO.			-594			UNIT
			MODE	MIN	MAX	
9	t_{CH}	CRC word hold time device	0	5		ns
			1	5		ns
			2	5		ns
			3	5		ns
			4	5		ns
10	t_{CVS}	CRC word valid setup time at host, CRC valid before DMACK negation	0	70		ns
			1	48		ns
			2	31		ns
			3	20		ns
			4	6.7		ns
11	t_{CVH}	CRC word valid hold time at sender, CRC valid after DMACK negation	0	6.2		ns
			1	6.2		ns
			2	6.2		ns
			3	6.2		ns
			4	6.2		ns
12	t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing	0	0		ns
			1	0		ns
			2	0		ns
			3	0		ns
			4	0		ns
13	t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing	0	70		ns
			1	48		ns
			2	31		ns
			3	20		ns
			4	6.7		ns
14	t_{FS}	First STROBE time	0		230	ns
			1		200	ns
			2		170	ns
			3		130	ns
			4		120	ns
15	t_{LI}	Limited interlock time	0	0	150	ns
			1	0	150	ns
			2	0	150	ns
			3	0	100	ns
			4	0	100	ns
16	t_{MLI}	Interlock time with minimum	0	20		ns
			1	20		ns
			2	20		ns
			3	20		ns
			4	20		ns
17	t_{UI}	Unlimited interlock time	0	0		ns
			1	0		ns
			2	0		ns
			3	0		ns
			4	0		ns

Table 5-36. Timings for ATA/CF Module --- Ultra DMA AC Timing (see Figure 5-23 through Figure 5-32) (continued)

NO.			-594			UNIT
			MODE	MIN	MAX	
18	t_{AZ}	Maximum time allowed for output drivers to release	0		10	ns
			1		10	ns
			2		10	ns
			3		10	ns
			4		10	ns
19	t_{ZAH}	Minimum delay time required for output	0	20		ns
			1	20		ns
			2	20		ns
			3	20		ns
			4	20		ns
20	t_{ZAD}	Minimum delay time for driver to assert or negate (from released)	0	0		ns
			1	0		ns
			2	0		ns
			3	0		ns
			4	0		ns
21	t_{ENV}	Envelope time, DMACK to STOP and DMACK to HDMARDY during in-burst initiation and from DMACK to STOP during data out burst initiation	0	20	70	ns
			1	20	70	ns
			2	20	70	ns
			3	20	55	ns
			4	20	55	ns
22	t_{RFS}	Ready-to-final-STROBE time	0		75	ns
			1		70	ns
			2		60	ns
			3		60	ns
			4		60	ns
23	t_{RP}	Ready to pause time (time that recipient shall wait to pause after negating HDMARDY)	0	160		ns
			1	125		ns
			2	100		ns
			3	100		ns
			4	100		ns
24	t_{IORDYZ}	Maximum time before releasing $\overline{\text{IORDY}}$	0		20	ns
			1		20	ns
			2		20	ns
			3		20	ns
			4		20	ns
25	t_{ZIORDY}	Minimum time before driving $\overline{\text{IORDY}}$	0	0		ns
			1	0		ns
			2	0		ns
			3	0		ns
			4	0		ns
26	t_{ACK}	Setup and hold time for DMACK (before assertion or negation)	0	20		ns
			1	20		ns
			2	20		ns
			3	20		ns
			4	20		ns

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Table 5-36. Timings for ATA/CF Module --- Ultra DMA AC Timing (see Figure 5-23 through Figure 5-32) (continued)

NO.			-594			UNIT
			MODE	MIN	MAX	
27	t_{SS}	STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	0	50		ns
			1	50		ns
			2	50		ns
			3	50		ns
			4	50		ns

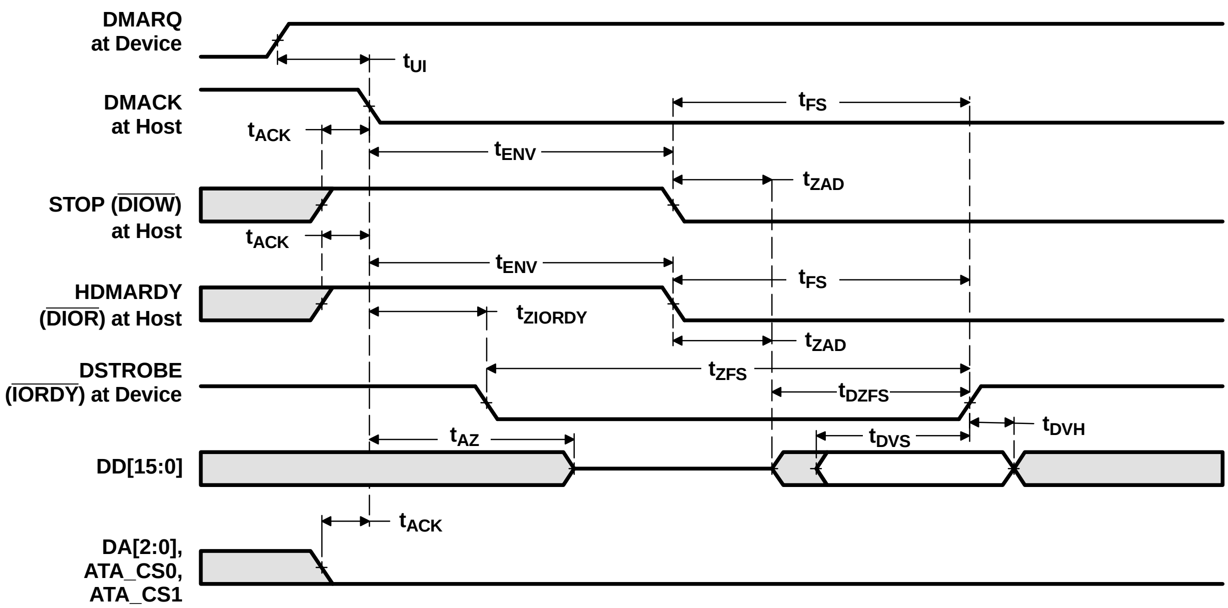
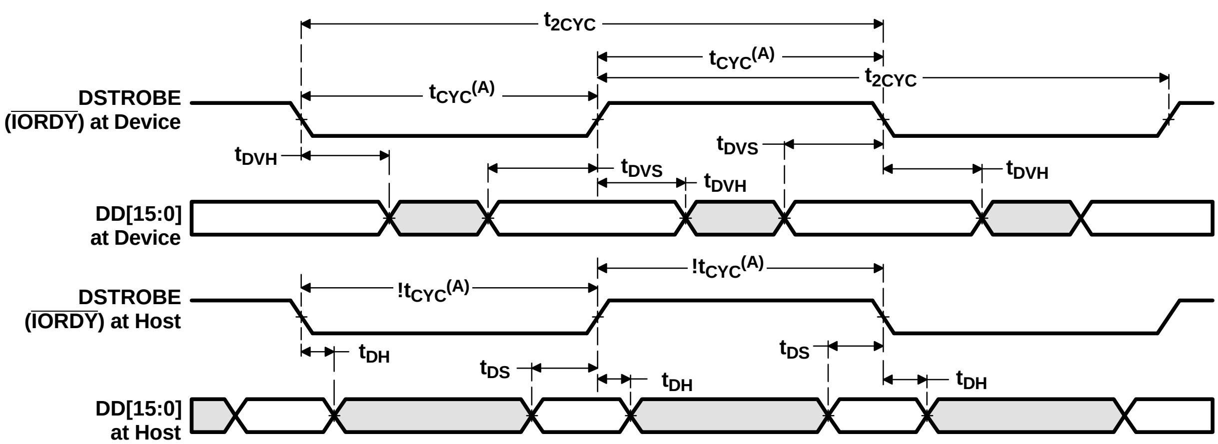


Figure 5-23. ATA/CF Initiating an Ultra DMA Data-In Burst Timing



A. While DSTROBE (IORDY) timing is t_{CYC} at the device, it may be different at the host due to propagation delay differences on the cable.

Figure 5-24. ATA/CF Sustained Ultra DMA Data-In Data Transfer Timing

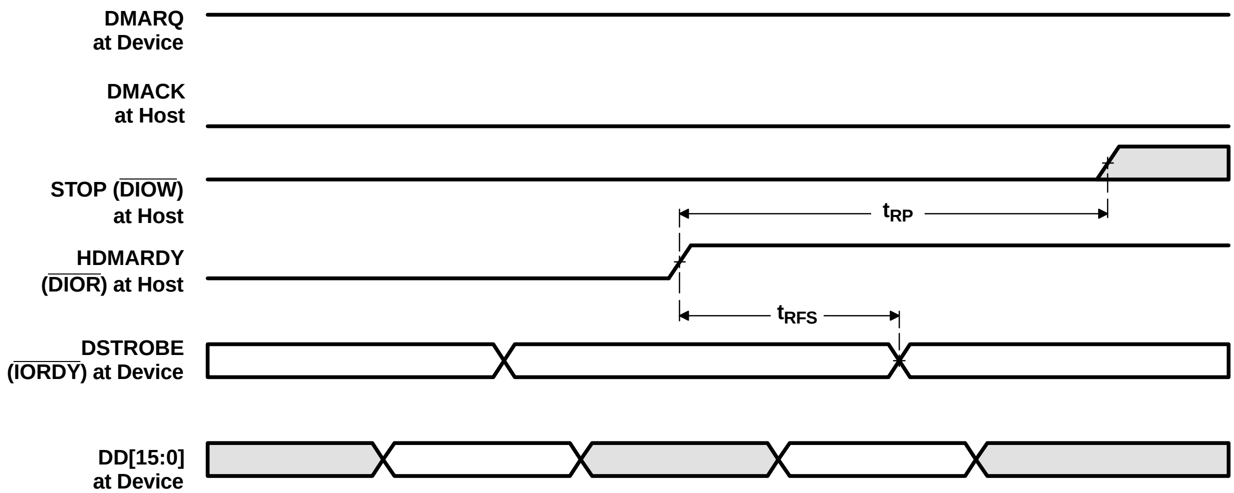


Figure 5-25. ATA/CF Host Pausing an Ultra DMA Data-In Burst Timing

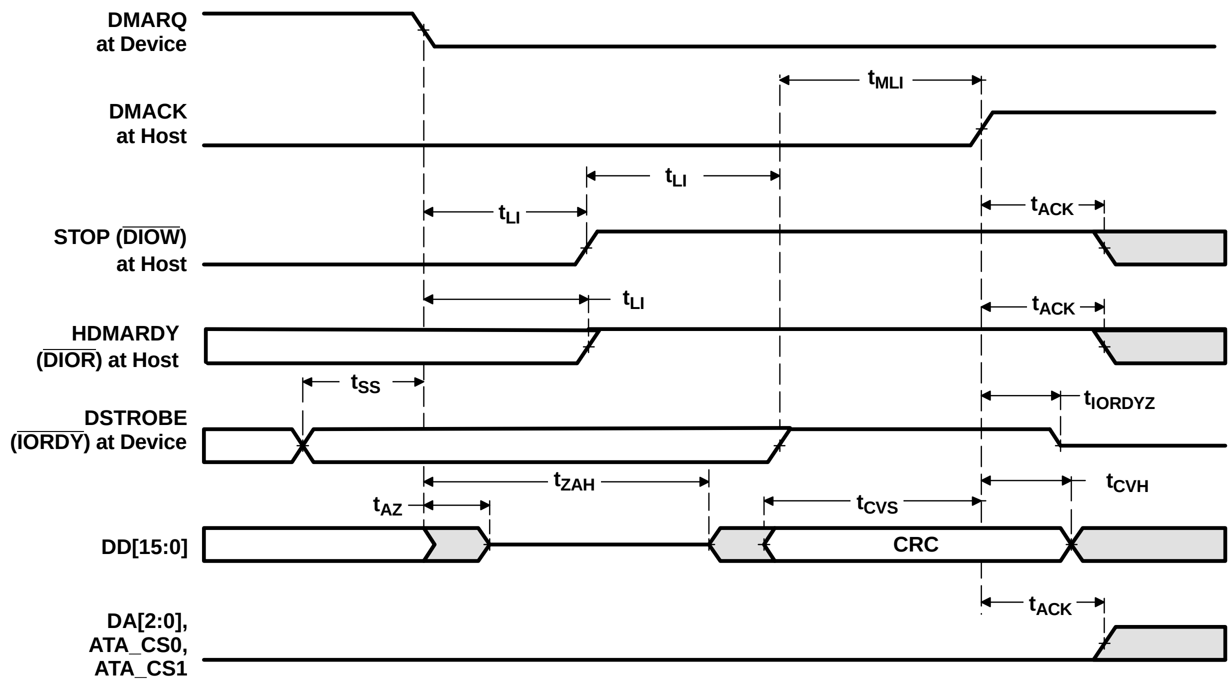


Figure 5-26. ATA/CF Device Terminating an Ultra DMA Data-In Burst Timing

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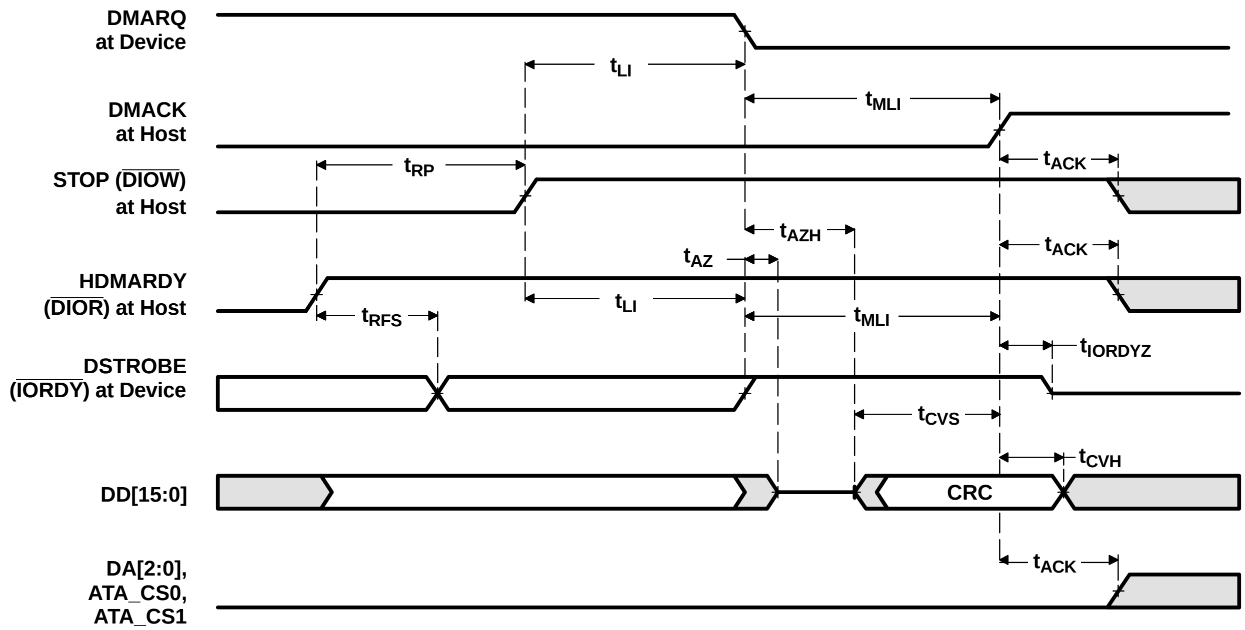


Figure 5-27. ATA/CF Host Terminating an Ultra DMA Data-In Burst Timing

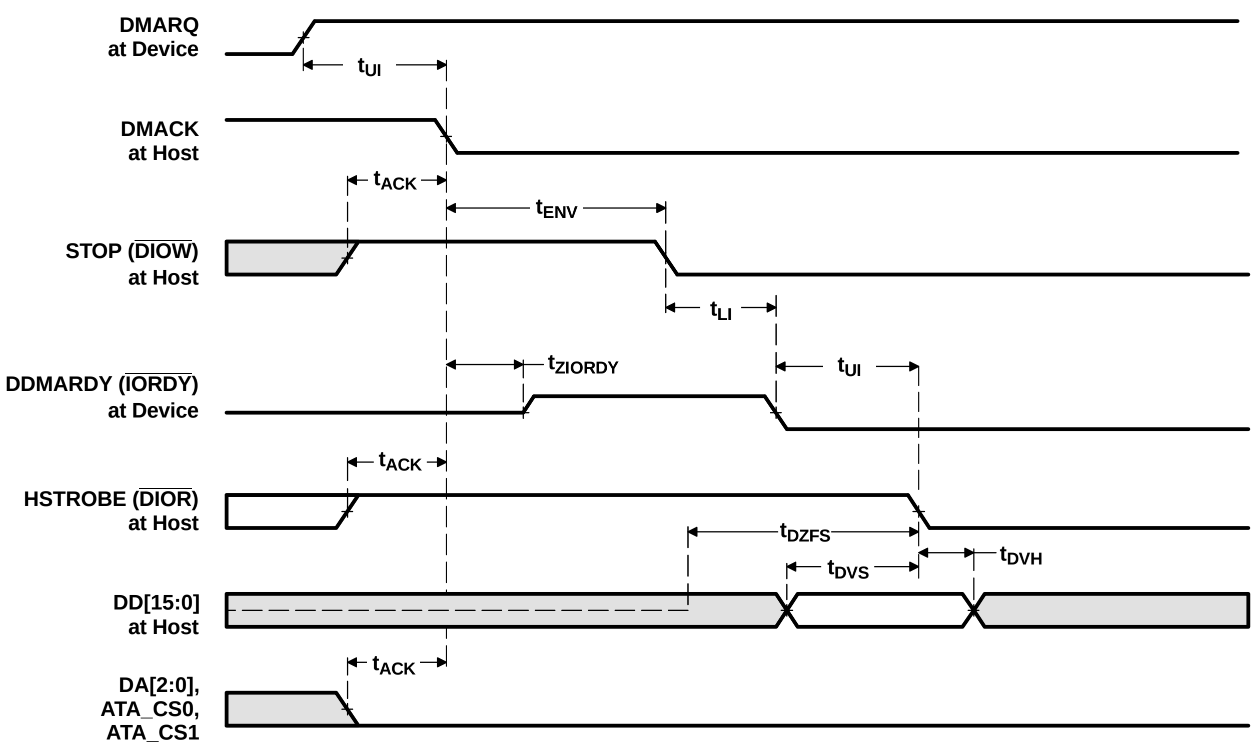
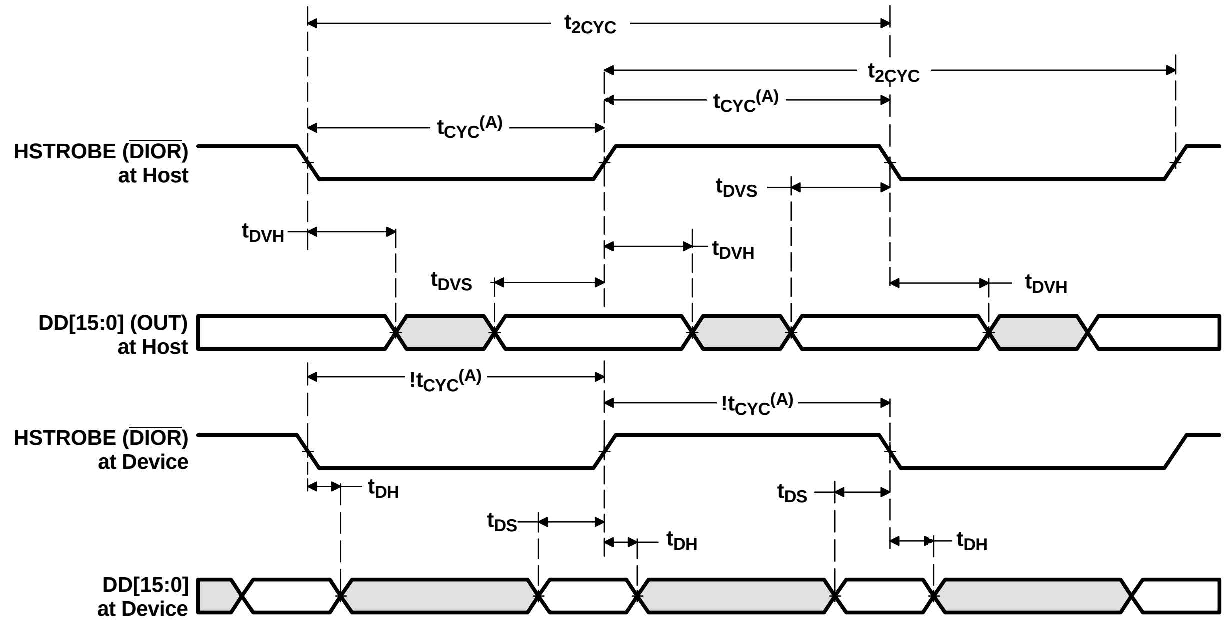


Figure 5-28. ATA/CF Initiating an Ultra DMA Data-Out Burst Timing



A. While HSTROBE (DIOR) timing is t_{CYC} at the host, it may be different at the device due to propagation delay differences on the cable.

Figure 5-29. ATA/CF Sustained Ultra DMA Data-Out Transfer Timing

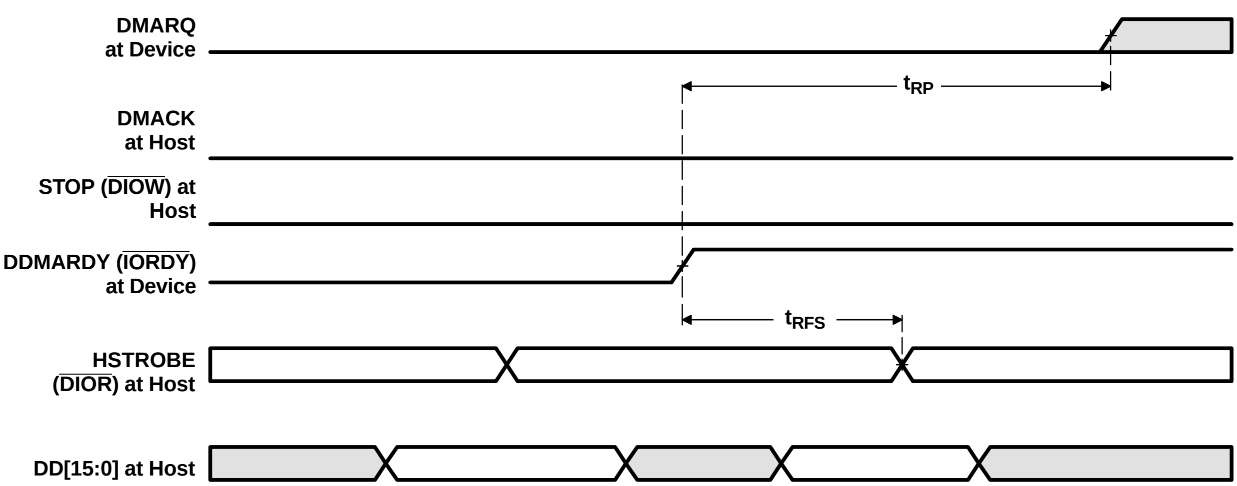


Figure 5-30. ATA/CF Device Pausing an Ultra DMA Data-Out Burst Timing

PRODUCT PREVIEW

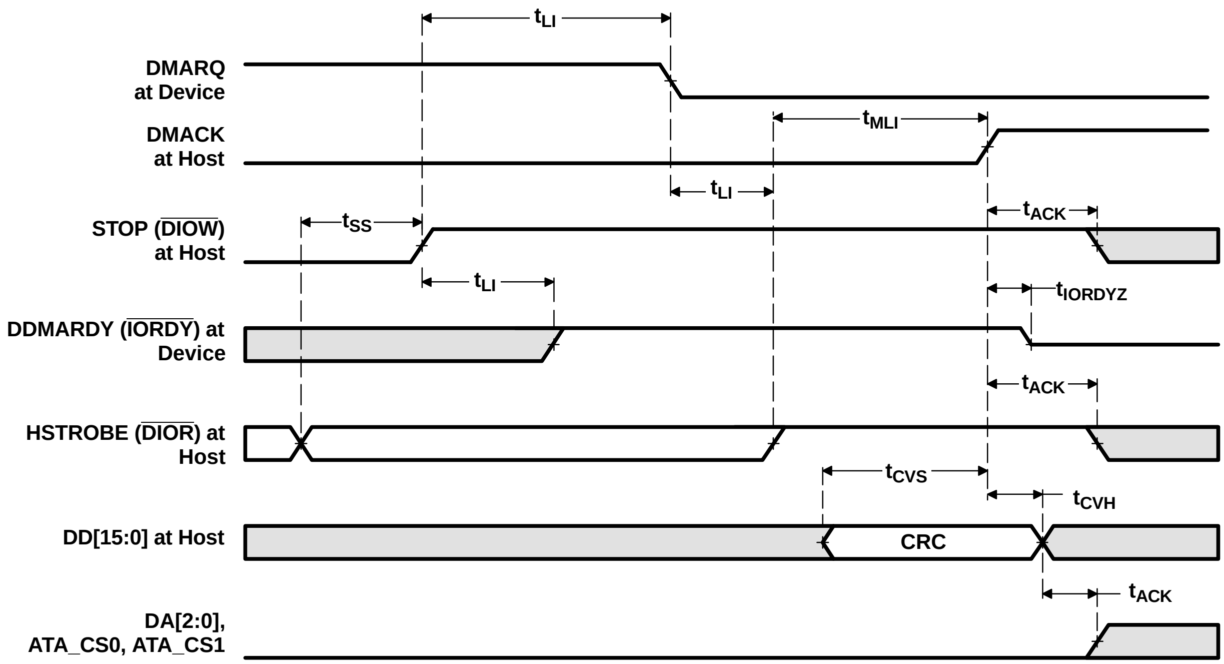


Figure 5-31. ATA/CF Host Terminating an Ultra DMA Data-Out Burst Timing

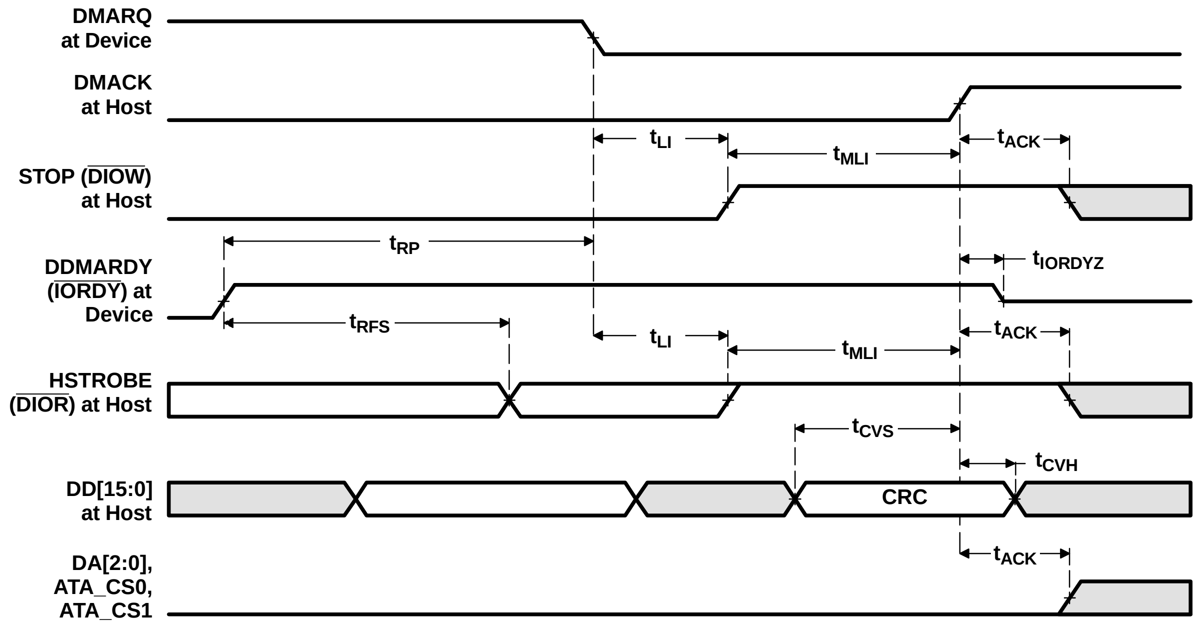


Figure 5-32. ATA/CF Device Terminating an Ultra DMA Data-Out Burst Timing

5.11.2.4 ATA/CF HDDIR Timing

Figure 5-33 through Figure 5-36 show the behavior of HDDIR for the different types of transfers.

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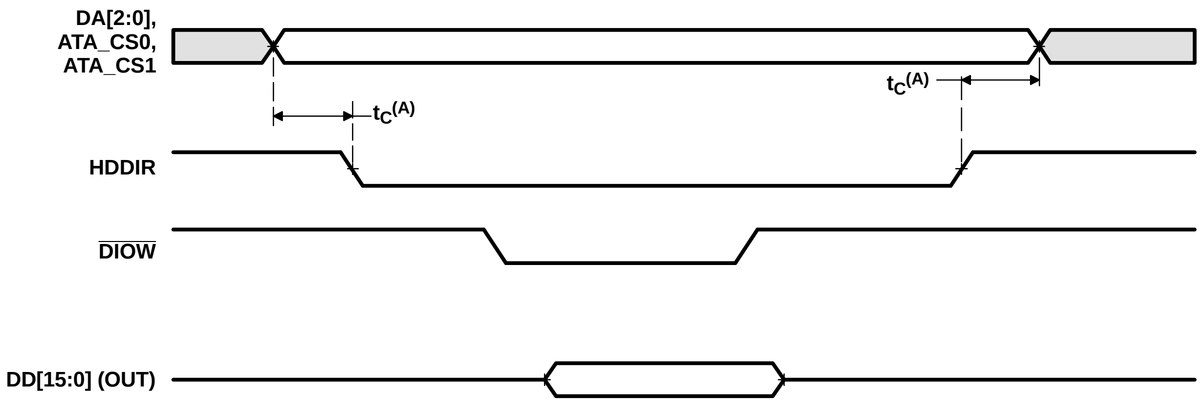
Table 5-37. Timing Requirements for HDDIR[(1)]

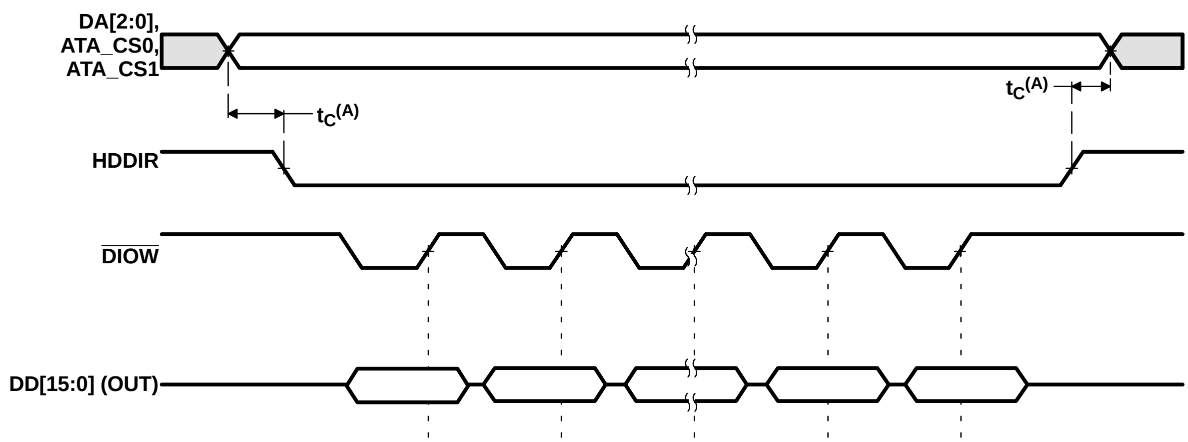
NO.			-594		UNIT
			MIN	MAX	
1	t_c	Cycle time, ATA_CS[1:0] to HDDIR low	E		ns

(1) E = ATA clock cycle



A. $t_C \geq$ one cycle

Figure 5-33. ATA/CF HDDIR Taskfile Write/Single PIO Write Timing



A. $t_C \geq$ one cycle

Figure 5-34. ATA/CF HDDIR PIO Postwrite Start Timing

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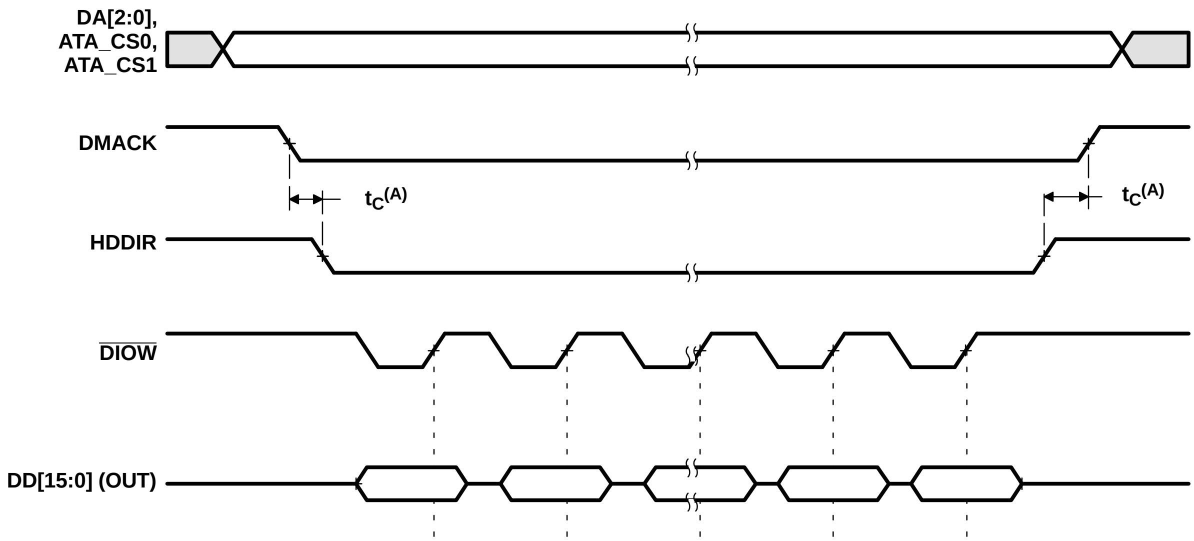
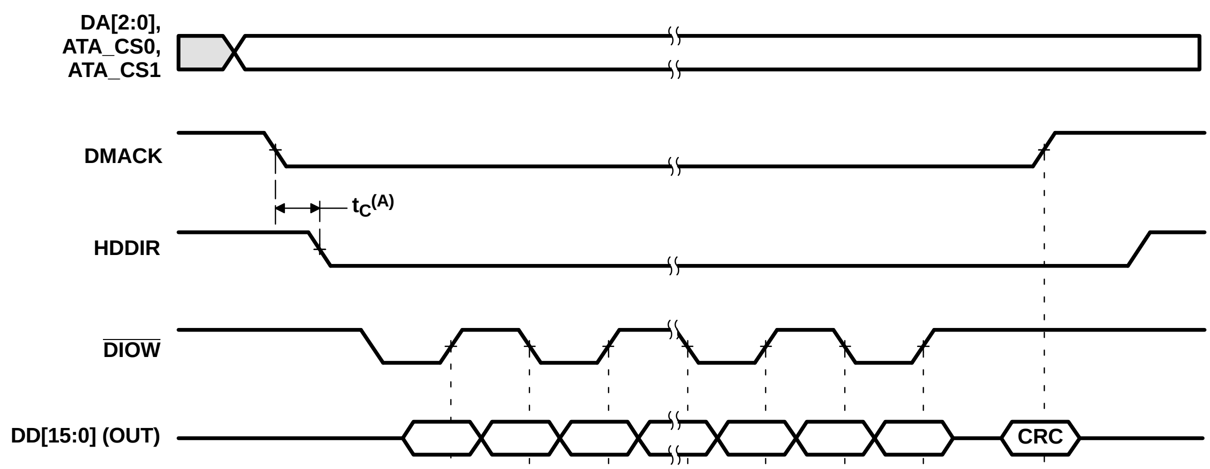


A. $t_C \geq$ one cycle

Figure 5-35. ATA/CF HDDIR Multiword DMA Write Transfer Timing



A. $t_C \geq$ one cycle

Figure 5-36. ATA/CF HDDIR Ultra DMA Write Transfer Timing

5.12 MMC/SD

The DM6446 MMC/SD Controller has following features:

- MultiMediaCard (MMC).
- Secure Digital (SD) Memory Card.
- MMC/SD protocol support.
- SDIO protocol support.
- Programmable clock frequency.
- 256 bit Read/Write FIFO to lower system overhead.
- Slave DMA transfer capability.

The MMC/SD register memory mapping is shown in Table 5-38.

5.12.1 MMC/SD Peripheral Description(s)

Table 5-38. MMC/SD Register Descriptions

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01E1 0000	MMCCTL	MMC Control Register
0x01E1 0004	MMCCLK	MMC Memory Clock Control Register
0x01E1 0008	MMCST0	MMC Status Register 0
0x01E1 000C	MMCST1	MMC Status Register 1
0x01E1 0010	MMCIM	MMC Interrupt Mask Register
0x01E1 0014	MMCTOR	MMC Response Time-Out Register
0x01E1 0018	MMCTOD	MMC Data Read Time-Out Register
0x01E1 001C	MMCBLEN	MMC Block Length Register
0x01E1 0020	MMCNBLK	MMC Number of Blocks Register
0x01E1 0024	MMCNBLC	MMC Number of Blocks Counter Register
0x01E1 0028	MMCDRR	MMC Data Receive Register
0x01E1 002C	MMCDXR	MMC Data Transmit Register
0x01E1 0030	MMCCMD	MMC Command Register
0x01E1 0034	MMCARGHL	MMC Argument Register
0x01E1 0038	MMCRSP01	MMC Response Register 0 and 1
0x01E1 003C	MMCRSP23	MMC Response Register 2 and 3
0x01E1 0040	MMCRSP45	MMC Response Register 4 and 5
0x01E1 0044	MMCRSP67	MMC Response Register 6 and 7
0x01E1 0048	MMCDRSP	MMC Data Response Register
0x01E1 004C - 0x01E1 004F	-	Reserved
0x01E1 0050	MMCCIDX	MMC Command Index Register
0x01E1 0054 - 0x01E1 0063	-	Reserved
0x01E1 0064	SDIOCTL	SDIO Control Register
0x01E1 0068	SDIOST0	SDIO Status Register 0
0x01E1 006C	SDIOIEN	SDIO Interrupt Enable Register
0x01E1 0070	SDIOIST	SDIO Interrupt Status Register
0x01E1 0074	MMCFIFOCTL	MMC FIFO Control Register
0x01E1 0078 - 0x01E1 FFFF	-	Reserved

5.12.2 MMC/SD Electrical Data/Timing

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Table 5-39. Timing Requirements for MMC/SD Module (see Figure 5-38 and Figure 5-40)

NO.			-594				UNIT
			FAST MODE		STANDARD MODE		
			MIN	MAX	MIN	MAX	
3	$t_{su(DATV-CLKH)}$	Setup time, SD_DATx valid before SD_CLK high	6		5		ns
4	$t_{h(CLKH-DATV)}$	Hold time, SD_DATx valid after SD_CLK high	2.5		5		ns

Table 5-40. Switching Characteristics Over Recommended Operating Conditions for MMC/SD Module(1) (see Figure 5-37 through Figure 5-40)

NO.	PARAMETER		-594				UNIT
			FAST MODE		STANDARD MODE		
			MIN	MAX	MIN	MAX	
7	$f_{(CLK)}$	Operating frequency, SD_CLK	0	50	0	25	MHz
8	$f_{(CLK\_ID)}$	Indentification mode frequency, SD_CLK	0	400	0	400	KHz
9	$t_{W(CLKL)}$	Pulse width, SD_CLK low	7		10		ns
10	$t_{W(CLKH)}$	Pulse width, SD_CLK high	7		10		ns
11	$t_{r(CLK)}$	Rise time, SD_CLK		3		10	
12	$t_{f(CLK)}$	Fall time, SD_CLK		3		10	
13	$t_{d(CLKLL-CMD)}$	Delay time, SD_CLK low to SD_CMD transition	-7.5	4	-7.5	14	ns
14	$t_{dis(CLKL-DAT)}$	Disable time, SD_CLK low to SD_DATx transition	-7.5	4	-7.5	14	ns

(1) P = Period of SD_CLK in nanoseconds (ns).

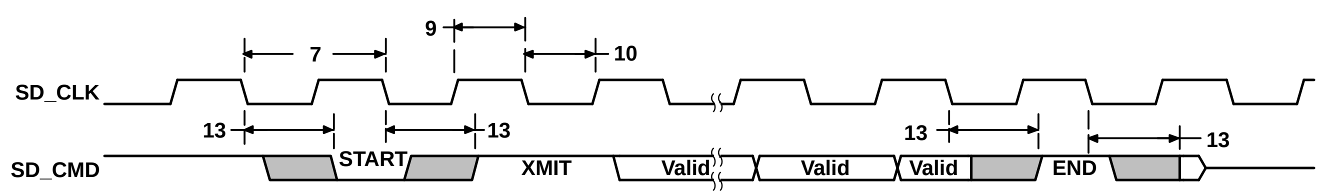

Figure 5-37. MMC/SD Host Command Timing

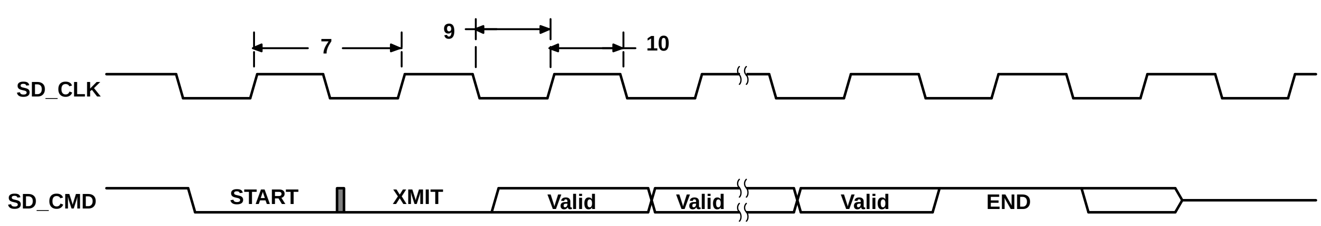

Figure 5-38. MMC/SD Card Response Timing

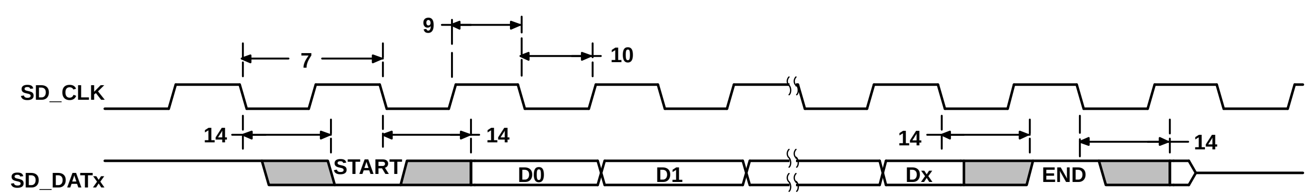

Figure 5-39. MMC/SD Host Write Timing

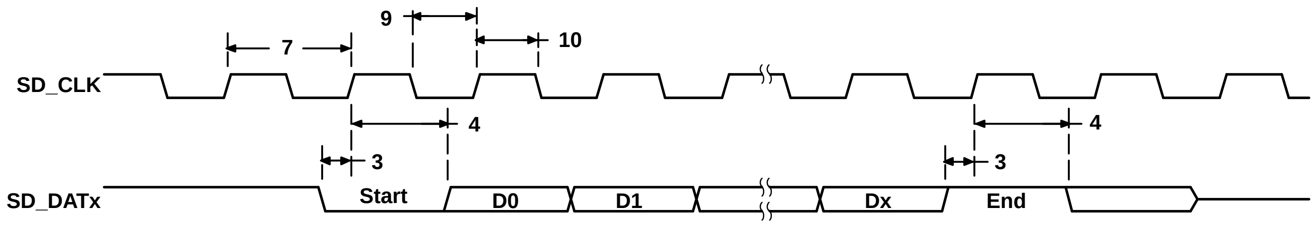

Figure 5-40. MMC/SD Host Read and Card CRC Status Timing

5.13 Video Processing Sub-System (VPSS) Overview

The DM6446 Video Processing Sub-System (VPSS) provides a Video Processing Front End (VPFE) input interface for external imaging peripherals (i.e., image sensors, video decoders, etc.) and a Video Processing Back End (VPBE) output interface for display devices, such as analog SDTV displays, digital LCD panels, HDTV video encoders, etc.

Note: The VPSS module is supported with Linux Application Peripheral Interfaces (APIs) commonly used by video application developers. Video for Linux 2 or V4L2 uses APIs commonly used for video capture. The typical use cases of the VPSS Video Front-End (VPFE) have been ported to this Linux API structure. V4L2 supports standard video interfaces such as: BT.656 and Y/C mode. Other modules within the VPSS VPFE for example, the Preview Engine, H3A, and Histogram are *not* currently supported within the software APIs. The VPSS Back-End (VPBE) uses FBDev/DirectFB as the APIs. Certain functionalities within the VPBE have not been implemented in the FBDev/DirectFB APIs. For modes/functions not implemented in software, it is user's responsibility to modify the software drivers/APIs.

The VPSS register memory mapping is shown in Table 5-41.

Table 5-41. VPSS Register Descriptions

HEX ADDRESS RANGE	REGISTER ACRONYM	Description
0x01C7 3400	PID	Peripheral Revision and Class Information
0x01C7 3404	PCR	VPSS Control Register
0x01C7 3408	-	Reserved
0x01C7 3508	SDR_REG_EXP	SDRAM Non Real-Time Read Request Expand
0x01C7 350C - 0x01C7 3FFF	-	Reserved

5.13.1 Video Processing Front-End (VPFE)

The Video Processing Front-End (VPFE) consists of the CCD Controller (CCDC), Preview Engine, Resizer, Hardware 3A (H3A) Statistic Generator, and Histogram blocks. Together, these modules provide DM6446 with a powerful and flexible front-end interface. These modules are briefly described below:

- The CCDC provides an interface to image sensors and digital video sources.
- The Preview Engine is a parameterized hardwired image processing block which is used for converting RAW color data from a Bayer pattern to YUV4:2:2.
- The Resizer module re-sizes the input image data to the desired display or video encoding resolution
- The H3A module provides control loops for Auto Focus (AF), Auto White Balance (AWB) and Auto Exposure (AE).
- The Histogram module bins input color pixels, depending on the amplitude, and provides statistics required to implement various 3A (AE/AF/AWB) algorithms and tune the final image/video output.

The VPFE register memory mapping is shown in Table 5-42.

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Table 5-42. VPFE Register Descriptions

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C7 0400 – 0x01C7 07FF	CCDC	VPFE – CCD Controller
0x01C7 0800 – 0x01C7 0BFF	PREV	VPFE – Preview Engine/Image Signal Processor
0x01C7 0C00 – 0x01C7 09FF	RESZ	VPFE – Resizer
0x01C7 1000 – 0x01C7 13FF	HIST	VPFE – Histogram
0x01C7 1400 – 0x01C7 17FF	H3A	VPFE – Hardware 3A (Auto-Focus/WB/Exposure)
0x01C7 3400 – 0x01C7 3FFF	VPSS	VPSS Shared Buffer Logic Registers

5.13.1.1 CCD Controller (CCDC)

The CCDC receives raw image/video data from sensors (CMOS or CCD) or YUV video data in numerous formats from video decoder devices. The following features are supported by the CCDC module.

- Conventional Bayer pattern formats.
- Generates HD/VD timing signals and field ID to an external timing generator or can synchronize to an external timing generator.
- Interface to progressive and interlaced sensors.
- Up to 75 MHz sensor clock in the normal mode of operation (1.05v).
- REC656/CCIR-656 standard (YCbCr 422 format, either 8- or 16-bit).
- YCbCr 422 format, either 8- or 16-bit with discrete H and VSYNC signals.
- Up to 16-bit input.
- Optical black clamping signal generation.
- Shutter signal control.
- Digital clamping and black level compensation.
- 10-bit to 8-bit A-law compression.
- Low-pass filter prior to writing to SDRAM. If this filter is enabled, 2 pixels each in the left and right edges of each line are cropped from the output.
- Output range from 16-bits to 8-bits wide (8-bits wide allows for 50% saving in storage area).
- Downsampling via programmable culling patterns.
- Control output to the DDR2 via an external write enable signal.
- Up to 16K pixels (image size) in both the horizontal and vertical direction.

The CCDC register memory mapping is shown in Table 5-43.

Table 5-43. CCDC Register Descriptions

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x01C7 0400	PID	Peripheral Revision and Class Information
0x01C7 0404	PCR	Peripheral Control Register
0x01C7 0408	SYN_MODE	SYNC and Mode Set Register
0x01C7 040C	HD_VD_WID	HD and VD Signal Width
0x01C7 0410	PIX_LINES	Number of Pixels in a Horizontal Line and Number of Lines in a Frame
0x01C7 0414	HORZ_INFO	Horizontal Pixel Information
0x01C7 0418	VERT_START	Vertical Line - Settings for the Starting Pixel
0x01C7 041C	VERT_LINES	Number of Vertical Lines
0x01C7 0420	CULLING	Culling Information in Horizontal and Vertical Directions
0x01C7 0424	HSIZE_OFF	Horizontal Size
0x01C7 0428	SDOFST	SDRAM/DDRAM Line Offset
0x01C7 042C	SDR_ADDR	SDRAM Address
0x01C7 0430	CLAMP	Optical Black Clamping Settings

Table 5-43. CCDC Register Descriptions (continued)

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x01C7 0434	DCSUB	DC Clamp
0x01C7 0438	COLPTN	CCD Color Pattern
0x01C7 043C	BLKCMP	Black Compensation
0x01C7 0440	-	Reserved
0x01C7 0444	-	Reserved
0x01C7 0448	VDINT	VD Interrupt Timing
0x01C7 044C	ALAW	A-Law Setting
0x01C7 0450	REC656IF	REC656 Interface
0x01C7 0454	CCDCFG	CCD Configuration
0x01C7 0458	FMTCFG	Data Reformatter/Video Port Configuration
0x01C7 045C	FMT_HORZ	Data Reformatter/Video Input Interface Horizontal Information
0x01C7 0460	FMT_VERT	Data Reformatter/Video Input Interface Vertical Information
0x01C7 0464	FMT_ADDR0	Address Pointer 0 Setup
0x01C7 0468	FMT_ADDR1	Address Pointer 1 Setup
0x01C7 046C	FMT_ADDR2	Address Pointer 2 Setup
0x01C7 0470	FMT_ADDR3	Address Pointer 3 Setup
0x01C7 0474	FMT_ADDR4	Address Pointer 4 Setup
0x01C7 0478	FMT_ADDR5	Address Pointer 5 Setup
0x01C7 047C	FMT_ADDR6	Address Pointer 6 Setup
0x01C7 0480	FMT_ADDR7	Address Pointer 7 Setup
0x01C7 0484	PRGEVEN_0	Program Entries 0-7 for Even Line
0x01C7 0488	RRGEVEN_1	Program Entries 8-15 for Even Line
0x01C7 048C	PRGGODD_0	Program Entries 0-7 for Odd Line
0x01C7 0490	PRGGODD_1	Program Entries 8-15 for Odd Line
0x01C7 0494	VP_OUT	Video Port Output Settings

5.13.1.2 Preview Engine

The preview engine transforms raw unprocessed image/video data from a sensor (CMOS or CCD) into YCbCr 422 data. The output of the preview engine is used for both video compression and external display devices such as a NTSC/PAL analog encoder or a digital LCD. The following features are supported by the preview engine.

- Accepts conventional Bayer pattern formats.
- Input image/video data from either the CCD/CMOS controller or the SDRAM/DDRAM.
- Output width up to 1280 pixels wide.
- Automatic/mandatory cropping of pixels/lines when edge processing is performed. If all the corresponding modules are enabled, a total of 14 pixels per line (7 left most and 7 right most) and 8 lines (4 top most and 4 bottom most) will not be output.
- Simple horizontal averaging (by factors of 2, 4, or 8) to handle input widths that are greater than 1280 (plus the cropped number) pixels wide.
- Dark frame capture to DDR2.
- Dark frame subtraction for every input raw data frame, fetched from DDR2, pixel-by-pixel to improve video quality.
- Lens shading compensation. Each input pixel is multiplied with a corresponding 8-bit gain value and the result is right shifted by a programmable parameter (0-7 bits).
- A-law decompression to transform non-linear 8-bit data to 10-bit linear data. This feature allows data in DDR2 to be 8-bits, which saves 50% of the area if the input to the preview engine is from the DDR2.
- Horizontal median filter for reducing temperature induced noise in pixels.

- Programmable noise filter that operates on a 3x3 grid of the same color (effectively, this is a five line storage requirement).
- Digital gain and white balance (color separate gain for white balance).
- Programmable CFA interpolation that operates on a 5x5 grid.
- Conventional Bayer pattern RGB and complementary color sensors.
- Support for an image that is downsampled by 2x in the horizontal direction (with and without phase correction). In this case, the image is 2/3 populated instead of the conventional 1/3 colors.
- Support for an image that is downsampled by 2x in both the horizontal and vertical direction. In this case, the image is fully populated instead of the conventional 1/3 colors.
- Programmable RGB-to-RGB blending matrix (9 coefficients for the 3x3 matrix).
- Fully programmable gamma correction (1024 entries for each color held in an on-chip RAM).
- Programmable color conversion (RGB to YUV) coefficients (9 coefficients for the 3x3 matrix).
- Luminance enhancement (non-linear) and chrominance suppression & offset.

The Preview Engine register memory mapping is shown in Table 5-44.

Table 5-44. Preview Engine Register Descriptions

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x01C7 0800	PID	Peripheral Revision and Class Information
0x01C7 0804	PCR	Peripheral Control Register
0x01C7 0808	HORZ_INFO	Horizontal Information/Setup
0x01C7 080C	VERT_INFO	Vertical Information/Setup
0x01C7 0810	RSDR_ADDR	Read Address From SDRAM
0x01C7 0814	RADR_OFFSET	Line Offset for the Read Data
0x01C7 0818	DSDR_ADDR	Dark Frame Address From SDRAM
0x01C7 081C	DRKF_OFFSET	Line Offset for the Dark Frame Data
0x01C7 0820	WSDR_ADDR	Write Address to the SDRAM
0x01C7 0824	WADD_OFFSET	Line Offset for the Write Data
0x01C7 0828	AVE	Input Formatter/Averager
0x01C7 082C	HMED	Horizontal Median Filter
0x01C7 0830	NF	Noise Filter
0x01C7 0834	WB_DGAIN	White Balance Digital Gain
0x01C7 0838	WBGAIN	White Balance Coefficients
0x01C7 083C	WBSEL	White Balance Coefficients Selection
0x01C7 0840	CFA	CFA Register
0x01C7 0844	BLKADJOFF	Black Adjustment Offset
0x01C7 0848	RGB_MAT1	RGB2RGB Blending Matrix Coefficients
0x01C7 084C	RGB_MAT2	RGB2RGB Blending Matrix Coefficients
0x01C7 0850	RGB_MAT3	RGB2RGB Blending Matrix Coefficients
0x01C7 0854	RGB_MAT4	RGB2RGB Blending Matrix Coefficients
0x01C7 0858	RGB_MAT5	RGB2RGB Blending Matrix Coefficients
0x01C7 085C	RGB_OFF1	RGB2RGB Blending Matrix Offsets
0x01C7 0860	RGB_OFF2	RGB2RGB Blending Matrix Offsets
0x01C7 0864	CSC0	Color Space Conversion Coefficients
0x01C7 0868	CSC1	Color Space Conversion Coefficients
0x01C7 086C	CSC2	Color Space Conversion Coefficients
0x01C7 0870	CSC_OFFSET	Color Space Conversion Offsets
0x01C7 0874	CNT_BRT	Contrast and Brightness Settings
0x01C7 0878	CSUP	Chrominance Supression Settings

Table 5-44. Preview Engine Register Descriptions (continued)

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x01C7 087C	SETUP_YC	Maximum/Minimum Y and C Settings
0x01C7 0880	SET_TBL_ADDRESS	Setup Table Addresses
0x01C7 0884	SET_TBL_DATA	Setup Table Data

5.13.1.3 Resizer

The resizer module can accept input image/video data from either the preview engine or DDR2. The output of the resizer module is sent to DDR2. The following features are supported by the resizer module.

- An output width up to 1280 horizontal pixels.
- Input from external DDR2.
- Up to 4x upsampling (digital zoom).
- Bi-cubic interpolation (4-tap horizontal, 4-tap vertical) can be implemented with the programmable filter coefficients.
- 8 phases of filter coefficients.
- Optional bi-linear interpolation for the chrominance components.
- Up to 1/4x downsampling
- 4-tap horizontal and 4-tap vertical filter coefficients (with 8-phases) for 1x to 1/2x downsampling
- 1/2x to 1/4x downsampling, for 7-tap mode with 4-phases.
- Resizing either YUV 422 packed data (16-bits) or color separate data (8-bit data within DDR) that is contiguous.
- Separate/independent resizing factor for the horizontal and vertical directions.
- Upsampling and downsampling ratios that are available are: 256/N, with N ranging from 64 to 1024.
- Programmable luminance sharpening after the horizontal resizing and before the vertical resizing step.

The Resizer register memory mapping is shown in Table 5-45.

Table 5-45. Resizer Register Descriptions

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x01C7 0C00	PID	Peripheral Revision and Class Information
0x01C7 0C04	PCR	Peripheral Control Register
0x01C7 0C08	RSZ_CNT	Resizer Control Bits
0x01C7 0C0C	OUT_SIZE	Output Width and Height After Resizing
0x01C7 0C10	IN_START	Input Starting Information
0x01C7 0C14	IN_SIZE	Input Width and Height Before Resizing
0x01C7 0C18	SDR_INADD	Input SDRAM Address
0x01C7 0C1C	SDR_INOFF	SDRAM Offset for the Input Line
0x01C7 0C20	SDR_OUTADD	Output SDRAM Address
0x01C7 0C24	SDR_OUTOFF	SDRAM Offset for the Output Line
0x01C7 0C28	HFILT10	Horizontal Filter Coefficients 1 and 0
0x01C7 0C2C	HFILT32	Horizontal Filter Coefficients 3 and 2
0x01C7 0C30	HFILT54	Horizontal Filter Coefficients 5 and 4
0x01C7 0C34	HFILT76	Horizontal Filter Coefficients 7 and 6
0x01C7 0C38	HFILT98	Horizontal Filter Coefficients 9 and 8
0x01C7 0C3C	HFILT1110	Horizontal Filter Coefficients 11 and 10
0x01C7 0C40	HFILT1312	Horizontal Filter Coefficients 13 and 12
0x01C7 0C44	HFILT1514	Horizontal Filter Coefficients 15 and 14
0x01C7 0C48	HFILT1716	Horizontal Filter Coefficients 17 and 16

Table 5-45. Resizer Register Descriptions (continued)

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x01C7 0C4C	HFILT1918	Horizontal Filter Coefficients 19 and 18
0x01C7 0C50	HFILT2120	Horizontal Filter Coefficients 21 and 20
0x01C7 0C54	HFILT2322	Horizontal Filter Coefficients 23 and 22
0x01C7 0C58	HFILT2524	Horizontal Filter Coefficients 25 and 24
0x01C7 0C5C	HFILT2726	Horizontal Filter Coefficients 27 and 26
0x01C7 0C60	HFILT2928	Horizontal Filter Coefficients 29 and 28
0x01C7 0C64	HFILT3130	Horizontal Filter Coefficients 31 and 30
0x01C7 0C68	VFILT10	Vertical Filter Coefficients 1 and 0
0x01C7 0C6C	VFILT32	Vertical Filter Coefficients 3 and 2
0x01C7 0C70	VFILT54	Vertical Filter Coefficients 5 and 4
0x01C7 0C74	VFILT76	Vertical Filter Coefficients 7 and 6
0x01C7 0C78	VFILT98	Vertical Filter Coefficients 9 and 8
0x01C7 0C7C	VFILT1110	Vertical Filter Coefficients 11 and 10
0x01C7 0C80	VFILT1312	Vertical Filter Coefficients 13 and 12
0x01C7 0C84	VFILT1514	Vertical Filter Coefficients 15 and 14
0x01C7 0C88	VFILT1716	Vertical Filter Coefficients 17 and 16
0x01C7 0C8C	VFILT1918	Vertical Filter Coefficients 19 and 18
0x01C7 0C90	VFILT2120	Vertical Filter Coefficients 21 and 20
0x01C7 0C94	VFILT2322	Vertical Filter Coefficients 23 and 22
0x01C7 0C98	VFILT2524	Vertical Filter Coefficients 25 and 24
0x01C7 0C9C	VFILT2726	Vertical Filter Coefficients 27 and 26
0x01C7 0CA0	VFILT2928	Vertical Filter Coefficients 29 and 28
0x01C7 0CA4	VFILT3130	Vertical Filter Coefficients 31 and 30
0x01C7 0CA8	YENH	Luminance Enhancer

5.13.1.4 Hardware 3A (H3A)

The Hardware 3A (H3A) module provides control loops for Auto Focus, Auto White Balance and Auto Exposure. There are 2 main components of the H3A module:

- Auto Focus (AF) Engine
- Auto Exposure (AE) & Auto White Balance (AWB) Engine

The AF engine extracts and filters the red, green, and blue data from the input image/video data and provides either the accumulation or peaks of the data in a specified region. The specified region is a two dimensional block of data and is referred to as a “paxel” for the case of AF.

The AE/AWB Engine accumulates the values and checks for saturated values in a sub sampling of the video data. In the case of the AE/AWB, the two-dimensional block of data is referred to as a “window”. The number, dimensions, and starting position of the AF paxels and the AE/AWB windows are separately programmable.

The H3A register memory mapping is shown in Table 5-46.

Table 5-46. H3A Register Descriptions

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x01C7 1400	PID	Peripheral Revision and Class Information
0x01C7 1404	PCR	Peripheral Control Register
0x01C7 1408	AFPAX1	Setup for the AF Engine Paxel Configuration
0x01C7 140C	AFPAX2	Setup for the AF Engine Paxel Configuration
0x01C7 1410	AFPAXSTART	Start Position for AF Engine Paxels

Table 5-46. H3A Register Descriptions (continued)

0x01C7 1414	AFIIRSH	Start Position for IIRSH
0x01C7 1418	AFBUFST	SDRAM/DDRAM Start Address for AF Engine
0x01C7 141C	AFCOEF010	IIR Filter Coefficient Data for SET 0
0x01C7 1420	AFCOEF032	IIR Filter Coefficient Data for SET 0
0x01C7 1424	AFCOEFF054	IIR Filter Coefficient Data for SET 0
0x01C7 1428	AFCOEFF076	IIR Filter Coefficient Data for SET 0
0x01C7 142C	AFCOEFF098	IIR Filter Coefficient Data for SET 0
0x01C7 1430	AFCOEFF0010	IIR Filter Coefficient Data for SET 0
0x01C7 1434	AFCOEF110	IIR Filter Coefficient Data for SET 1
0x01C7 1438	AFCOEF132	IIR Filter Coefficient Data for SET 1
0x01C7 143C	AFCOEFF154	IIR Filter Coefficient Data for SET 1
0x01C7 1440	AFCOEFF176	IIR Filter Coefficient Data for SET 1
0x01C7 1444	AFCOEFF198	IIR Filter Coefficient Data for SET 1
0x01C7 1448	AFCOEFF1010	IIR Filter Coefficient Data for SET 1
0x01C7 144C	AEWWIN1	Configuration for AE/AWB Windows
0x01C7 1450	AEWINSTART	Start Position for AE/AWB Windows
0x01C7 1454	AEWINBLK	Start Position and Height for Black Line of AE/AWB Windows
0x01C7 1458	AEWSUBWIN	Configuration for Subsample Data in AE/AWB Window
0x01C7 145C	AEWBUFST	SDRAM/DDRAM Start Address for AE/AWB Engine

5.13.1.4.1 Auto Focus (AF) Engine

The following features are supported by the Auto Focus (AF) Engine.

- Peak Mode in a Paxel (a Paxel is defined as a two dimensional block of pixels).
- Accumulate the maximum Focus Value of each line in a Paxel
- Accumulation/Sum Mode (instead of Peak mode).
- Accumulate Focus Value in a Paxel.
- Up to 36 Paxels in the horizontal direction and up to 128 Paxels in the vertical direction.
- Programmable width and height for the Paxel. All paxels in the frame will be of same size.
- Programmable red, green, and blue position within a 2x2 matrix.
- Separate horizontal start for paxel and filtering.
- Programmable vertical line increments within a paxel.
- Parallel IIR filters configured in a dual-biquad configuration with individual coefficients (2 filters with 11 coefficients each). The filters are intended to compute the sharpness/peaks in the frame to focus on.

5.13.1.4.2 Auto Exposure (AE) and Auto White Balance (AWB) Engine

The following features are supported by the Auto Exposure (AE) and Auto White Balance (AWB) Engine.

- Accumulate clipped pixels along with all non-saturated pixels.
- Up to 36 horizontal windows.
- Up to 128 vertical windows.
- Programmable width and height for the windows. All windows in the frame will be of same size.
- Separate vertical start coordinate and height for a black row of paxels that is different than the remaining color paxels.
- Programmable Horizontal Sampling Points in a window.
- Programmable Vertical Sampling Points in a window.

5.13.1.5 Histogram

The histogram module accepts raw image/video data and bins the pixels on a value (and color separate) basis. The value of the pixel itself is not stored, but each bin contains the number of pixels that are within the appropriate set range. The source of the raw data for the histogram is typically a CCD/CMOS sensor (via the CCDC module) or optionally from DDR2. The following features are supported by the histogram module.

- Up to four regions/areas.
- Separate horizontal/vertical start and end position for each region.
- Pixels from overlapping regions are accumulated into the highest priority region. The priority is: region0 > region1 > region2 > region3.
- Interface to conventional Bayer pattern. Each region can accumulate either 3 or 4 colors.
- 32, 64, 128, or 256 bins per color per region.
- 32, 64, or 128 bins per color for 2 regions.
- 32 or 64 bins per color for 3 or 4 regions.
- Automatic clear of histogram RAM after an ARM read.
- Saturation of the pixel count if the count exceeds the maximum value (each memory location is 20-bit wide).
- Downshift ranging from 0 to 7 bits (maximum bin range 128).
- The last bin (highest range of values) will accumulate any value that is higher than the lower bound.

The Histogram register memory mapping is shown in Table 5-47.

Table 5-47. Histogram Register Descriptions

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x01C7 1000	PID	Peripheral Revision and Class Information Register
0x01C7 1004	PCR	Peripheral Control Register
0x01C7 1008	HIST_CNT	Histogram Control Bits Register
0x01C7 100C	WB_GAIN	White/Channel Balance Settings Register
0x01C7 1010	R0_HORZ	Region 0 Horizontal Information Register
0x01C7 1014	R0_VERT	Region 0 Vertical Information Register
0x01C7 1018	R1_HORZ	Region 1 Horizontal Information Register
0x01C7 101C	R1_VERT	Region 1 Vertical Information Register
0x01C7 1020	R2_HORZ	Region 2 Horizontal Information Register
0x01C7 1024	R2_VERT	Region 2 Vertical Information Register
0x01C7 1028	R3_HORZ	Region 3 Horizontal Information Register
0x01C7 102C	R3_VERT	Region 3 Vertical Information Register
0x01C7 1030	HIST_ADDR	Histogram Address for Data to be Read Register
0x01C7 1034	HIST_DATA	Histogram Data That is Read From the Memory Register
0x01C7 1038	RADD	Read Address From SDRAM/DDRAM Register
0x01C7 103C	RADD_OFF	Read Address Offset for Each Line in the SDRAM/DDRAM Register
0x01C7 1040	H_V_INFO	Horizontal/Vertical Information Register (Horizontal/Vertical Number of Pixels When Data is Read From SDRAM/DDRAM Information Register)

5.13.1.6 VPFE Electrical Data/Timing

Table 5-48. Timing Requirements for VPFE PCLK Master/Slave Mode (see Figure 5-41)

NO.				-594 MIN	-594 MAX	UNIT
1	$t_{c(PCLK)}$	Cycle time, PCLK	Normal Mode	13.33	100	ns
			Turbo Mode	10.204	100	ns
2	$t_{w(PCLKH)}$	Pulse duration, PCLK high	Normal Mode	5.7		ns
			Turbo Mode	4.4		ns
3	$t_{w(PCLKL)}$	Pulse duration, PCLK low	Normal Mode	5.7		ns
			Turbo Mode	4.4		ns
4	$t_{t(PCLK)}$	Transition time, PCLK			3	ns

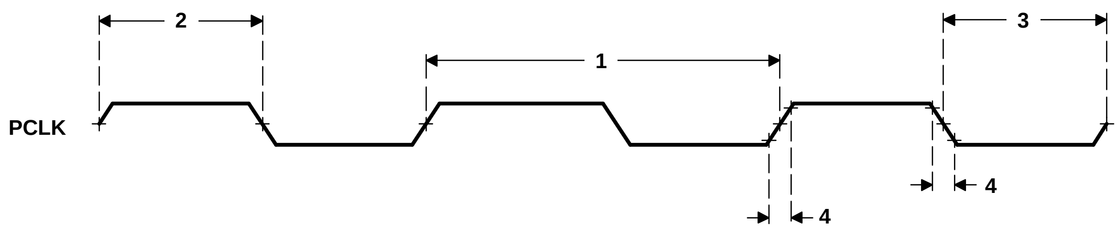

Figure 5-41. VPFE PCLK Timing

Table 5-49. Timing Requirements for VPFE (CCD) Slave Mode(1) (see Figure 5-42)

NO.			-594 MIN	-594 MAX	UNIT
5	$t_{su(CCDV-PCLK)}$	Setup time, CCD valid before PCLK edge	3		ns
6	$t_{h(PCLK-CCDV)}$	Hold time, CCD valid after PCLK edge	2		ns
7	$t_{su(HDV-PCLK)}$	Setup time, HD valid before PCLK edge	3		ns
8	$t_{h(PCLK-HDV)}$	Hold time, HD valid after PCLK edge	2		ns
9	$t_{su(VDV-PCLK)}$	Setup time, VD valid before PCLK edge	3		ns
10	$t_{h(PCLK-VDV)}$	Hold time, VD valid after PCLK edge	2		ns
11	$t_{su(C\_WEV-PCLK)}$	Setup time, $\overline{C\_WE}$ valid before PCLK edge	3		ns
12	$t_{h(PCLK-C\_WEV)}$	Hold time, $\overline{C\_WE}$ valid after PCLK edge	2		ns
13	$t_{su(C\_FIELDV-PCLK)}$	Setup time, C_FIELD valid before PCLK edge	3		ns
14	$t_{h(PCLK-C\_FIELDV)}$	Hold time, C_FIELD valid after PCLK edge	2		ns

(1) The VPFE may be configured to operate in either positive or negative edge clocking mode. When in positive edge clocking mode the rising edge of PCLK is referenced. When in negative edge clocking mode the falling edge of PCLK is referenced.

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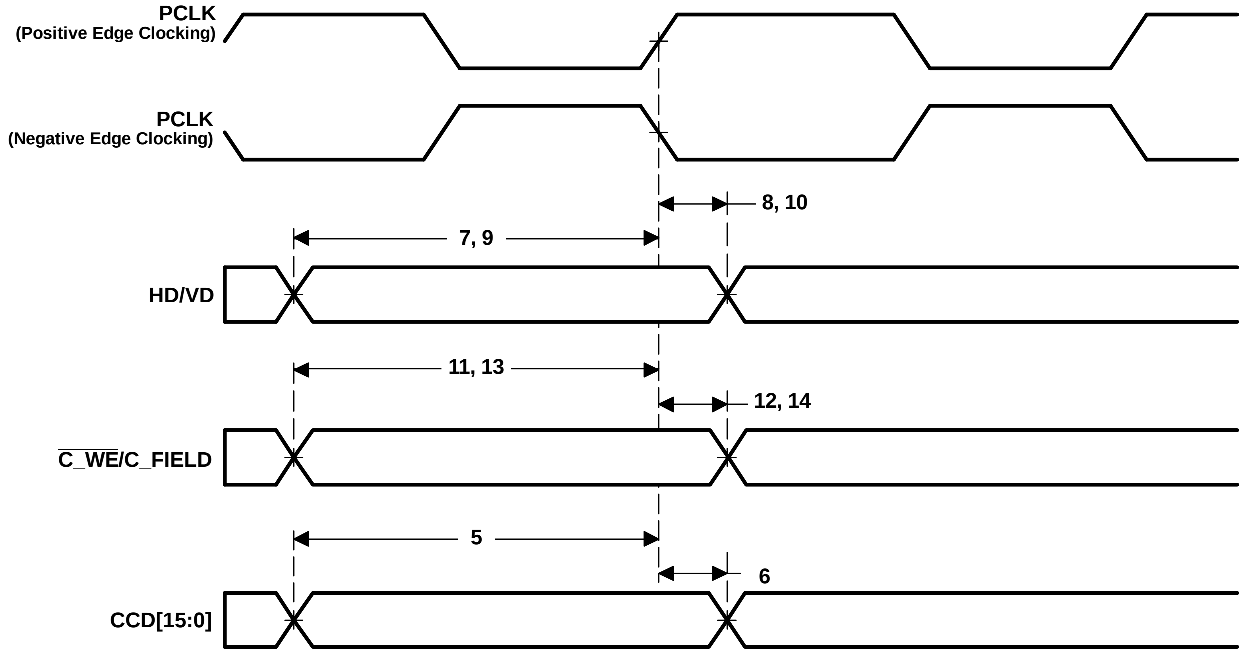

Figure 5-42. VPFE (CCD) Slave Mode Input Data Timing

Table 5-50. Timing Requirements for VPFE (CCD) Master Mode[(1)] (see Figure 5-43)

NO.			-594		UNIT
			MIN	MAX	
15	$t_{su(CCDV-PCLK)}$	Setup time, CCD valid before PCLK edge	3		ns
16	$t_{h(PCLK-CCDV)}$	Hold time, CCD valid after PCLK edge	2		ns
23	$t_{su(CWEV-PCLK)}$	Setup time, C_WE valid before PCLK edge	3		ns
24	$t_{h(PCLK-CWEV)}$	Hold time, C_WE valid after PCLK edge	2		ns

(1) The VPFE may be configured to operate in either positive or negative edge clocking mode. When in positive edge clocking mode the rising edge of PCLK is referenced. When in negative edge clocking mode the falling edge of PCLK is referenced.

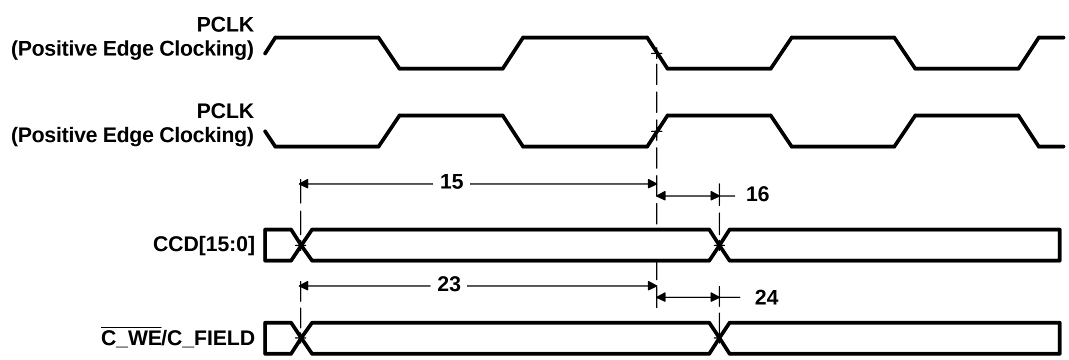

Figure 5-43. VPFE (CCD) Master Mode Input Data Timing

Table 5-51. Switching Characteristics Over Recommended Operating Conditions for VPFE (CCD) Master

Table 5-51. Switching Characteristics Over Recommended Operating Conditions for VPFE (CCD) Master Mode (see Figure 5-44) (continued)

Mode (see Figure 5-44)

NO.	PARAMETER		-594		UNIT
			MIN	MAX	
17	$t_{d(HDV-PCLKL)}$	Delay time, HD valid to PCLK low	0.5	8	ns
18	$t_{d(PCLKL-HDIV)}$	Delay time, PCLK low to HD invalid	0.5	8	ns
19	$t_{d(VDV-PCLKL)}$	Delay time, VD valid to PCLK low	0.5	8	ns
20	$t_{d(PCLKL-VDIV)}$	Delay time, PCLK low to VD invalid	0.5	8	ns
21	$t_{d(C\_FIELDV-PCLKL)}$	Delay time, C_FIELD valid to PCLK low	0.5	8	ns
22	$t_{d(PCLKL-C\_FIELDIV)}$	Delay time, PCLK low to C_FIELD invalid	0.5	8	ns

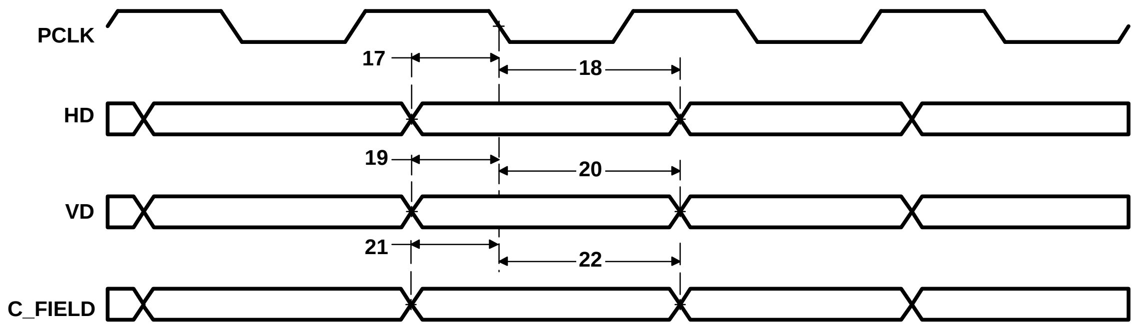

Figure 5-44. VPFE (CCD) Master Mode Control Output Data Timing

5.13.2 Video Processing Back-End (VPBE)

The Video Processing Back-End (VPBE) consists of the On-Screen Display (OSD) module, the Video Encoder (VENC) including the Digital LCD (DLCD) and Analog (i.e., DAC) interfaces. The video encoder generates analog video output. The DLCD controller generates digital RGB/YCbCr data output and timing signals.

The VPBE register memory mapping is shown in Table 5-52.

Table 5-52. VPBE Register Descriptions

Address	Register	Description
0x01C7 2780	PID	Peripheral Revision and Class Information Register
0x01C7 2784	PCR	Peripheral Control Register

5.13.2.1 On-Screen Display (OSD)

The major function of the OSD module is to gather and blend video data and display/bitmap data before feeding it to the Video Encoder (VENC) in YCbCr format. The video and display data is read from an external memory, typically DDR2. The OSD is programmed via control and parameter registers. The following are the primary features that are supported by the OSD.

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- Simultaneous display of two video windows and two OSD windows (VIDWIN0/VIDWIN1 and OSDWIN0/OSDWIN1).
  - Separate enable for each window
  - Programmable width, height, and base starting coordinates for each window
  - External memory address and offset registers for each window
  - Support for x2 and x4 zoom in both the horizontal and vertical direction
  - OSDWIN1 can be used as an attribute window for OSDWIN0
  - Attribute window blinking intervals
  - Field/frame mode for the windows (interlaced/progressive)
  - Eight step blending process between the OSD and video windows
  - Transparency support for the OSD and video data (when a bitmap pixel is zero, there will be no blending for that corresponding video pixel)
  - Resize from VGA to NTSC/PAL (640x480 to 720x576) for both the OSD and video windows
  - Reads in YCbCr data in 422 format from external memory, with the capability for swapping the order of the CbCr component in the 32-bit word (this is relevant to the two video windows)
  - Support for a ping-pong buffer scheme that can be used for VIDWIN0 (allows for video data to be accessed from two different locations in DDR2)
  - Each OSD window (either one, but not both at the same time) is capable of reading in RGB data (16-bit data with six bits for the green and five bits each for the red and blue colors) instead of bitmap data in YCbCr format restricted to a maximum of 8-bits
  - The OSD bitmap data width is selectable between 1, 2, 4, or 8-bits.
  - Each OSD window supports 16 entries for the bitmap (to index into a 256 entry RAM/ROM CLUT table).
  - Indirect support for 24-bit RGB input data (which will be transformed into 16-bit YCbCr video window data) via the wrapper interface in the VPBE.
- Support for a rectangular cursor window and a programmable background color selection.
  - Programmable color palette with the ability to select between a RAM/ROM table with support for 256 colors.
  - The width, height, and color of the cursor is programmable.
  - The display priority is: Rectangular-Cursor > OSDWIN1 > OSDWIN0 > VIDWIN1 > VIDWIN0 > background color
- Support for attenuation of the YCbCr values for the REC601 standard.

The following restrictions exist in the OSD module.

- Both the OSD windows and VIDWIN1 should be fully contained inside VIDWIN0.
- When one of the OSD windows is set in RGB mode, it cannot overlap with VIDWIN1.
- The OSD cannot support more than 256 color entries in the CLUT RAM/ROM. Some applications require higher number of entries, and one workaround is to use VIDWIN1 as an overlay mimicking the OSD window. Another option is to use the RGB mode for one of the OSD windows which allows for a total of 16-bits for the R, G, and B colors (64K colors).
- The OSD can only read YCbCr in 422 interleaved format for the video windows. Other formats, either color separate storage or 444/420 interleaved data is not supported.
- If the vertical resize filter is enabled for either of the video windows, the maximum horizontal window dimension cannot be greater than 720 currently.
- It is not possible to use both of the CLUT ROMs at the same time. However, one window can use RAM while another uses ROM.
- The 24-bit RGB input mode is only valid for one of the two video windows (programmable) and does not apply to the OSD windows.

The OSD register memory mapping is shown in Table 5-53.

Table 5-53. OSD Register Descriptions

Address	Register	Description
0x01C7 2600	MODE	OSD Mode Register
0x01C7 2604	VIDWINMD	Video Window Mode Setup
0x01C7 2608	OSDWIN0MD	OSD Window Mode Setup
0x01C7 260C	OSDWIN1MD	OSD Window 1 Mode Setup (when used as a second OSD window)
0x01C7 260C	OSDATRMD	OSD Attribute Window Mode Setup (when used as an attribute window)
0x01C7 2610	RECTCUR	Rectangular Cursor Setup
0x01C7 2614	RSV0	Reserved
0x01C7 2618	VIDWIN0OFST	Video Window 0 Offset
0x01C7 261C	VIDWIN1OFST	Video Window 1 Offset
0x01C7 2620	OSDWIN0OFST	OSD Window 0 Offset
0x01C7 2624	OSDWIN1OFST	OSD Window 1 Offset
0x01C7 2628	RSV1	Reserved
0x01C7 262C	VIDWIN0ADR	Video Window 0 Address
0x01C7 2630	VIDWIN1ADR	Video Window 1 Address
0x01C7 2634	RSV2	Reserved
0x01C7 2638	OSDWIN0ADR	OSD Window 0 Address
0x01C7 263C	OSDWIN1ADR	OSD Window 1 Address
0x01C7 2640	BASEPX	Base Pixel X
0x01C7 2644	BASEPY	Base Pixel Y
0x01C7 2648	VIDWIN0XP	Video Window 0 X-Position
0x01C7 264C	VIDWIN0YP	Video Window 0 Y-Position
0x01C7 2650	VIDWIN0XL	Video Window 0 X-Size
0x01C7 2654	VIDWIN0YL	Video Window 0 Y-Size
0x01C7 2658	VIDWIN1XP	Video Window 1 X-Position
0x01C7 265C	VIDWIN1YP	Video Window 1 Y-Position
0x01C7 2660	VIDWIN1XL	Video Window 1 X-Size
0x01C7 2664	VIDWIN1YL	Video Window 1 Y-Size
0x01C7 2668	OSDWIN0XP	OSD Bitmap Window 0 X-Position
0x01C7 266C	OSDWIN0YP	OSD Bitmap Window 0 Y-Position
0x01C7 2670	OSDWIN0XL	OSD Bitmap Window 0 X-Size
0x01C7 2674	OSDWIN0YL	OSD Bitmap Window 0 Y-Size
0x01C7 2678	OSDWIN1XP	OSD Bitmap Window 1 X-Position
0x01C7 267C	OSDWIN1YP	OSD Bitmap Window 1 Y-Position
0x01C7 2680	OSDWIN1XL	OSD Bitmap Window 1 X-Size
0x01C7 2684	OSDWIN1YL	OSD Bitmap Window 1 Y-Size
0x01C7 2688	CURXP	Rectangular Cursor Window X-Position
0x01C7 268C	CURYP	Rectangular Cursor Window Y-Position
0x01C7 2690	CURXL	Rectangular Cursor Window X-Size
0x01C7 2694	CURYL	Rectangular Cursor Window Y-Size
0x01C7 2698	RSV3	Reserved
0x01C7 269C	RSV4	Reserved
0x01C7 26A0	W0BMP01	Window 0 Bitmap Value to Palette Map 0/1
0x01C7 26A4	W0BMP23	Window 0 Bitmap Value to Palette Map 2/3
0x01C7 26A8	W0BMP45	Window 0 Bitmap Value to Palette Map 4/5
0x01C7 26AC	W0BMP67	Window 0 Bitmap Value to Palette Map 6/7
0x01C7 26B0	W0BMP89	Window 0 Bitmap Value to Palette Map 8/9

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Table 5-53. OSD Register Descriptions (continued)

0x01C7 26B4	W0BMPAB	Window 0 Bitmap Value to Palette Map A/B
0x01C7 26B8	W0BMPCD	Window 0 Bitmap Value to Palette Map C/D
0x01C7 26BC	W0BMPEF	Window 0 Bitmap Value to Palette Map E/F
0x01C7 26C0	W1BMP01	Window 1 Bitmap Value to Palette Map 0/1
0x01C7 26C4	W1BMP23	Window 1 Bitmap Value to Palette Map 2/3
0x01C7 26C8	W1BMP45	Window 1 Bitmap Value to Palette Map 4/5
0x01C7 26CC	W1BMP67	Window 1 Bitmap Value to Palette Map 6/7
0x01C7 26D0	W1BMP89	Window 1 Bitmap Value to Palette Map 8/9
0x01C7 26D4	W1BMPAB	Window 1 Bitmap Value to Palette Map A/B
0x01C7 26D8	W1BMPCD	Window 1 Bitmap Value to Palette Map C/D
0x01C7 26DC	W1BMPEF	Window 1 Bitmap Value to Palette Map E/F
0x01C7 26E0	-	Reserved
0x01C7 26E4	MISCCTL	Miscellaneous Control
0x01C7 26E8	RSV5	Reserved
0x01C7 26EC	CLUTRAMYCB	CLUT RAMYCB Setup
0x01C7 26F0	CLUTRAMCR	CLUT RAM Setup
0x01C7 26F4	TRANSPVAL	CLUT RAM Setup
0x01C7 26F8	RSV6	Reserved
0x01C7 26FC	PPVWIN0ADR	Ping-Pong Video Window 0 Address

5.13.2.2 Video Encoder (VENC)

Analog/DACs interface of the Video Encoder (VENC) supports the following features.

- Master Clock Input - 27MHz (x2 Upsampling)
- SDTV Support
  - Composite NTSC-M, PAL-B/D/G/H/I
  - S-Video (Y/C)
  - Component YPbPr (SMPTE/EBU N10, Betacam, MII)
  - RGB
  - Non-Interlace
  - CGMS/WSS
  - Line 21 Closed Caption Data Encoding
  - Chroma Low Pass Filter 1.5MHz/3MHz
  - Programmable SC-H phase
- HDTV Support
  - Progressive Output (525p/625p)
  - Component YPbPr
  - RGB
  - CGMS/WSS
- 4 10-bit Over-Sampling D/A Converters
- Optional 7.5% Pedestal
- 16-235/0-255 Input Amplitude Selectable
- Programmable Luma Delay
- Master/Slave Operation
- Internal Color Bar Generation (100%/75%)

The Digital LCD Controller (DLCD) of the VENC supports the following features.

- Programmable DCLK

- Various Output Formats
  - YCbCr 16bit
  - YCbCr 8bit
  - ITU-R BT. 656
  - Parallel RGB 24bit
- Low Pass Filter for Digital RGB Output
- Programmable Timing Generator
- Master/Slave Operation
- Internal Color Bar Generation (100%/75%)

The VENC register memory mapping including the Digital LCD and DACs is shown in Table 5-54.

Table 5-54. VENC (Including Digital LCD and DACs) Register Descriptions

Address	Register	Description
0x01C7 2400	VMOD	Video Mode
0x01C7 2404	VIDCTL	Video Interface I/O Control
0x01C7 2408	VDPRO	Video Data Processing
0x01C7 240C	SYNCCTL	Sync Control
0x01C7 2410	HSPLS	Horizontal Sync Pulse Width
0x01C7 2414	VSPLS	Vertical Sync Pulse Width
0x01C7 2418	HINT	Horizontal Interval
0x01C7 241C	HSTART	Horizontal Valid Data Start Position
0x01C7 2420	HVALID	Horizontal Data Valid Range
0x01C7 2424	VINT	Vertical Interval
0x01C7 2428	VSTART	Vertical Valid Data Start Position
0x01C7 242C	VVALID	Vertical Data Valid Range
0x01C7 2430	HSDLY	Horizontal Sync Delay
0x01C7 2434	VSDLY	Veritcal Sync Delay
0x01C7 2438	YCCTL	YCbCr Control
0x01C7 243C	RGBCTL	RGB Control
0x01C7 2440	RGBCLP	RGB Level Clipping
0x01C7 2444	LINECTL	Line Id Control
0x01C7 2448	CULLLINE	Culling line control
0x01C7 244C	LCDOUT	LCD Output Signal Control
0x01C7 2450	BRTS	Brightness Start Position Signal Control
0x01C7 2454	BRTW	Brightness Width Signal Control
0x01C7 2458	ACCTL	LCD_AC Signal Control
0x01C7 245C	PWMP	PWM Start Position Signal Control
0x01C7 2460	PWMW	PWM Width Signal Control
0x01C7 2464	DCLKCTL	DCLK Control
0x01C7 2468	DCLKPTN0	DCLK Pattern 0
0x01C7 246C	DCLKPTN1	DCLK Pattern 1
0x01C7 2470	DCLKPTN2	DCLK Pattern 2
0x01C7 2474	DCLKPTN3	DCLK Pattern 3
0x01C7 2478	DCLKPTN0A	DCLK Auxiliary Pattern 0
0x01C7 247C	DCLKPTN1A	DCLK Auxiliary Pattern 1
0x01C7 2480	DCLKPTN2A	DCLK Auxiliary Pattern 2
0x01C7 2484	DCLKPTN3A	DCLK Auxiliary Pattern 3
0x01C7 2488	DCLKHS	Horizontal DCLK Mask Atart

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Table 5-54. VENC (Including Digital LCD and DACs) Register Descriptions (continued)

0x01C7 248C	DCLKHSA	Horizontal Auxiliary DCLK Mask Atart
0x01C7 2490	DCLKHR	Horizontal DCLK Mask Range
0x01C7 2494	DCLKVS	Vertical DCLK Mask Start
0x01C7 2498	DCLKVR	Vertical DCLK Mask Range
0x01C7 249C	CAPCTL	Caption Control
0x01C7 24A0	CAPDO	Caption Data Odd Field
0x01C7 24A4	CAPDE	Caption Data Even Field
0x01C7 24A8	ATR0	Video Attribute Data # 0
0x01C7 24AC	ATR1	Video Attribute Data # 1
0x01C7 24B0	ATR2	Video Attribute Data # 2
0x01C7 24B4		Reserved
0x01C7 24B4		Reserved
0x01C7 24B4		Reserved
0x01C7 24B4		Reserved
0x01C7 24B8	VSTAT	Video Status
0x01C7 24BC	RAMADR	GCP/FRC Table RAM Address
0x01C7 24C0	RAMPORT	GCP/FRC Table RAM Data Port
0x01C7 24C4	DACTST	DAC Test
0x01C7 24C8	YCOLVL	YOUT and COUT Levels
0x01C7 24CC	SCPROG	Sub-Carrier Programming
0x01C7 24D0		Reserved
0x01C7 24D4		Reserved
0x01C7 24D8		Reserved
0x01C7 24DC	CVBS	Composite Mode
0x01C7 24E0	CMPNT	Component Mode
0x01C7 24E4	ETMG0	CVBS Timing Control 0
0x01C7 24E8	ETMG1	CVBS Timing Control 1
0x01C7 24EC	ETMG2	Component Timing Control 0
0x01C7 24F0	ETMG3	Component Timing Control 1
0x01C7 24F4	DACSEL	DAC Output Select
0x01C7 24F8		Reserved
0x01C7 24FC		Reserved
0x01C7 2500	ARGBX0	Analog RGB Matrix 0
0x01C7 2504	ARGBX1	Analog RGB Matrix 1
0x01C7 2508	ARGBX2	Analog RGB Matrix 2
0x01C7 250C	ARGBX3	Analog RGB Matrix 3
0x01C7 2510	ARGBX4	Analog RGB Matrix 4
0x01C7 2514	DRGBX0	Digital RGB Matrix 0
0x01C7 2518	DRGBX1	Digital RGB Matrix 1
0x01C7 251C	DRGBX2	Digital RGB Matrix 2
0x01C7 2520	DRGBX3	Digital RGB Matrix 3
0x01C7 2524	DRGBX4	Digital RGB Matrix 4
0x01C7 2528	VSTARTA	Vertical Data Valid Start Position for Even Field
0x01C7 252C	OSDCLK0	OSD Clock Control 0
0x01C7 2530	OSDCLK1	OSD Clock Control 1
0x01C7 2534	HVLDCL0	Horizontal Valid Culling Control 0
0x01C7 2538	HVLDCL1	Horizontal Valid Culling Control 1
0x01C7 253C	OSDHADV	OSD Horizontal Sync Advance

5.13.2.3 VPBE Electrical Data/Timing

Table 5-55. Timing Requirements for VPBE CLK Inputs (see Figure 5-45)

NO.			-594		UNIT
			MIN	MAX	
1	$t_{c(PCLK)}$	Cycle time, PCLK	13.33	160	ns
2	$t_{w(PCLKH)}$	Pulse duration, PCLK high	5.7		ns
3	$t_{w(PCLKL)}$	Pulse duration, PCLK low	5.7		ns
4	$t_{t(PCLK)}$	Transition time, PCLK		3	ns
5	$t_{c(VPBECLK)}$	Cycle time, VPBECLK	13.33	160	ns
6	$t_{w(VPBECLKH)}$	Pulse duration, VPBECLK high	5.7		ns
7	$t_{w(VPBECLKL)}$	Pulse duration, VPBECLK low	5.7		ns
8	$t_{t(VPBECLK)}$	Transition time, VPBECLK		3	ns

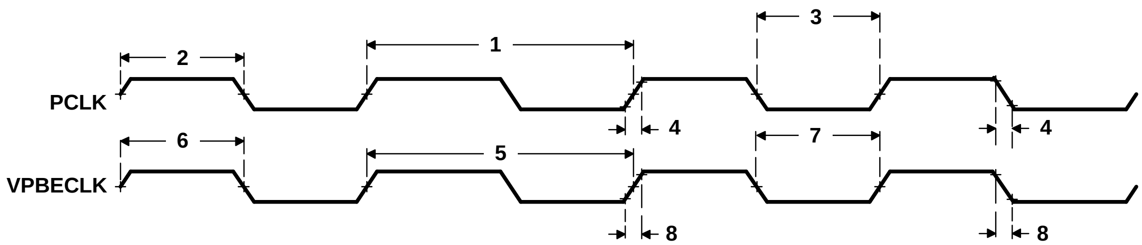
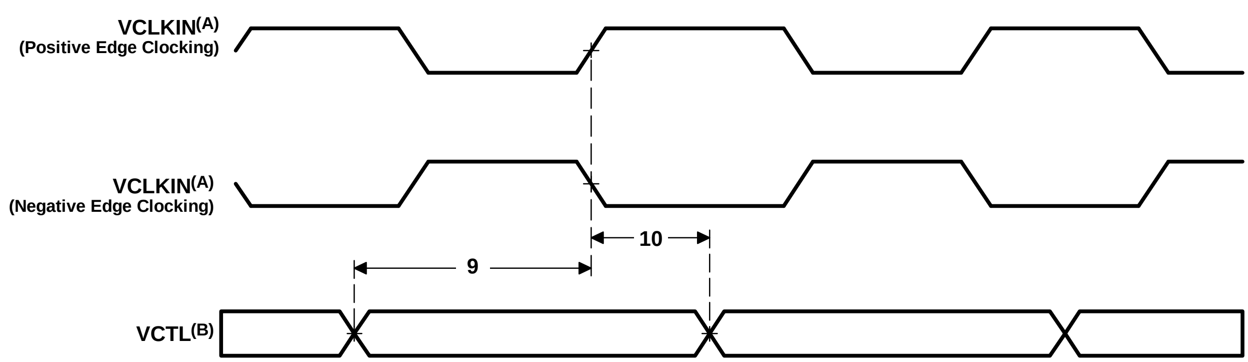


Figure 5-45. VPBE PCLK and VPBECLK Timing

Table 5-56. Timing Requirements for VPBE Control Input With Respect to PCLK and VPBECLK(1)(2) (see Figure 5-46)

NO.			-594		UNIT
			MIN	MAX	
9	$t_{su(VCTLV-VCLKIN)}$	Setup time, VCTL valid before VCLKIN edge	2		ns
10	$t_{h(VCLKIN-VCTLV)}$	Hold time, VCTL valid after VCLKIN edge	0.5		ns

(1) The VPBE may be configured to operate in either positive or negative edge clocking mode. When in positive edge clocking mode, the rising edge of VCLKIN is referenced. When in negative edge clocking mode, the falling edge of VCLKIN is referenced.
(2) VCLKIN = PCLK or VPBECLK



A. VCLKIN = PCLK or VPBECLK
B. VCTL = HSYNC, VSYNC, and VCLK

Figure 5-46. VPBE Input Timing With Respect to PCLK and VPBECLK

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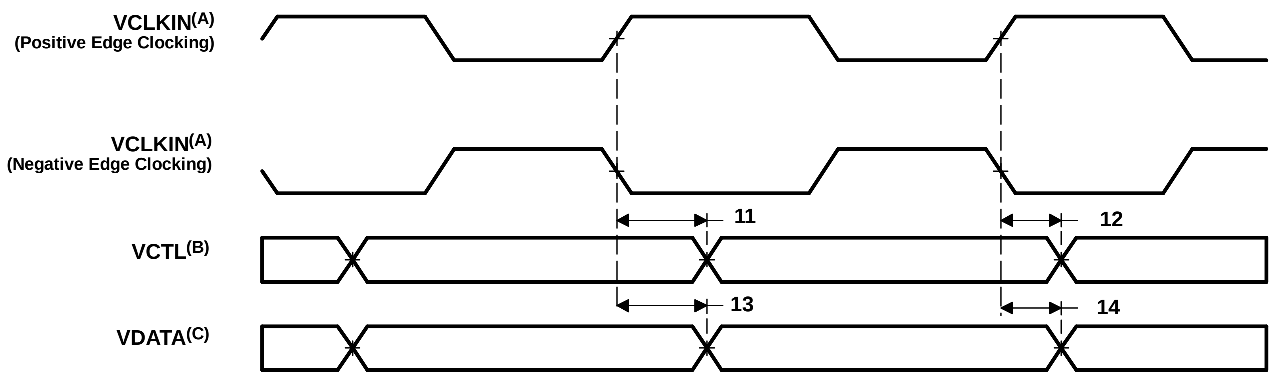
Table 5-57. Switching Characteristics Over Recommended Operating Conditions for VPBE Control and Data Output With Respect to PCLK and VPBECLK(1)(2) (see Figure 5-47)

NO.	PARAMETER		-594 MIN	-594 MAX	UNIT
11	$t_{d(VCLKIN-VCTLV)}$	Delay time, VCLKIN edge to VCTL valid		13.3	ns
12	$t_{d(VCLKIN-VCTLIV)}$	Delay time, VCLKIN edge to VCTL invalid	2		ns
13	$t_{d(VCLKIN-VDATAV)}$	Delay time, VCLKIN edge to VDATA valid		13.3	ns
14	$t_{d(VCLKIN-VDATAIV)}$	Delay time, VCLKIN edge to VDATA invalid	2		ns

(1) The VPBE may be configured to operate in either positive or negative edge clocking mode. When in positive edge clocking mode, the rising edge of VCLKIN is referenced. When in negative edge clocking mode, the falling edge of VCLKIN is referenced.
(2) VCLKIN = PCLK or VPBECLK



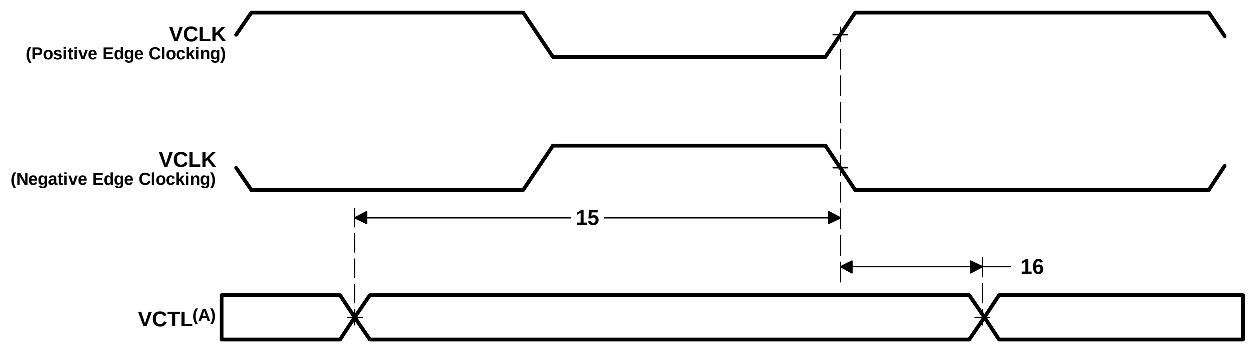
A. VCLKIN = PCLK or VPBECLK
B. VCTL = HSYNC, VSYNC, and VCLK
C. VDATA = COUT[7:0], YOUT[7:0], R[7:0], G[7:0], and B[7:0]

Figure 5-47. VPBE Output Timing With Respect to PCLK and VPBECLK

Table 5-58. Timing Requirements for VPBE Control Input With Respect to VCLK(1) (see Figure 5-48)

NO.			-594 MIN	-594 MAX	UNIT
15	$t_{su(VCTLV-VCLK)}$	Setup time, VCTL valid before VCLK edge	2		ns
16	$t_{h(VCLK-VCTLV)}$	Hold time, VCTL valid after VCLK edge	0.5		ns

(1) The VPBE may be configured to operate in either positive or negative edge clocking mode. When in positive edge clocking mode, the rising edge of VCLK is referenced. When in negative edge clocking mode, the falling edge of VCLK is referenced.



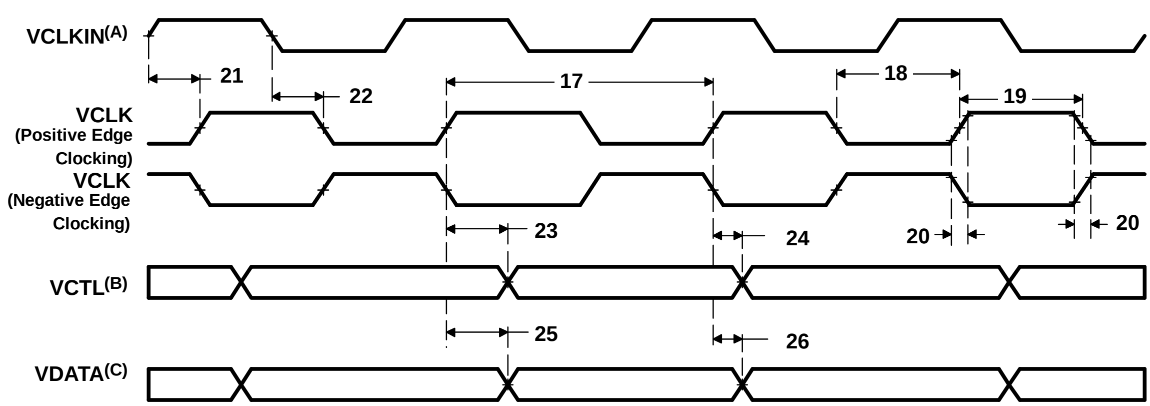
A. VCTL = HSYNC, VSYNC, and VCLK

Figure 5-48. VPBE Control Input Timing With Respect to VCLK

Table 5-59. Switching Characteristics Over Recommended Operating Conditions for VPBE Control and Data Output With Respect to VCLK(1)(2) (see Figure 5-49)

NO.	PARAMETER		-594 MIN	-594 MAX	UNIT
17	$t_{c(VCLK)}$	Cycle time, VCLK	13.33	160	ns
18	$t_{w(VCLKH)}$	Pulse duration, VCLK high	5.7		ns
19	$t_{w(VCLKL)}$	Pulse duration, VCLK low	5.7		ns
20	$t_{t(VCLK)}$	Transition time, VCLK		3	ns
21	$t_{d(VCLKINH-VCLKH)}$	Delay time, VCLKIN high to VCLK high	2	12	ns
22	$t_{d(VCLKINL-VCLKL)}$	Delay time, VCLKIN low to VCTL low	2	12	ns
23	$t_{d(VCLK-VCTLV)}$	Delay time, VCLK edge to VCTL valid		4	ns
24	$t_{d(VCLK-VCTLIV)}$	Delay time, VCLK edge to VCTL invalid	0		ns
25	$t_{d(VCLK-VDATAV)}$	Delay time, VCLK edge to VDATA valid		4	ns
26	$t_{d(VCLK-VDATAIV)}$	Delay time, VCLK edge to VDATA invalid	0		ns

(1) The VPBE may be configured to operate in either positive or negative edge clocking mode. When in positive edge clocking mode, the rising edge of VCLK is referenced. When in negative edge clocking mode, the falling edge of VCLK is referenced.
(2) VCLKIN = PCLK or VPBECLK



A. VCLKIN = PCLK or VPBECLK
B. VCTL = HSYNC, VSYNC, and VCLK
C. VDATA = COUT[7:0], YOUT[7:0], R[7:0], G[7:0], and B[7:0]

Figure 5-49. VPBE Control and Data Output Timing With Respect to VCLK

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5.14 USB 2.0

The DM6446 USB2.0 peripheral supports the following features:

- USB 2.0 peripheral at speeds high speed (HS: 480 Mb/s) and full speed (FS: 12 Mb/s)
- USB 2.0 host at speeds HS, FS, and low speed (LS: 1.5 Mb/s)
- All transfer modes (control, bulk, interrupt, and isochronous)
- 4 Transmit (TX) and 4 Receive (RX) endpoints in addition to endpoint 0
- FIFO RAM
  - 4K endpoint
  - Programmable size
- Connects to a standard UTMI+ PHY with a 60 MHz, 8-bit interface
- Connects to a standard Charge Pump for VBUS 5 V generation
- RNDIS mode for accelerating RNDIS type protocols using short packet termination over USB

The USB physical interface control register USBPHY_CTL is described in Figure 5-50 and Table 5-60.

Figure 5-50. USBPHY_CTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0000 0000 0000 0000															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							PHYC LKGD	SESN DEN	VBDT CTEN	RSV	PHYP LLON	CLKO 1SEL	OSCP DWN	RSV	PHYP DWN
R-0000 000							R-0	R/W-1	R/W-1	R-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1

LEGEND: R = Read, W = Write, n = value at reset

Table 5-60. USBPHY_CTL Register Descriptions

Name	Description
PHYCLKGD	USB PHY Power and Clock Good 0 = Phy power not ramped or PLL not locked 1 = Phy power is good and PLL is locked
SESNDEN	Session End Comparator enable 0 = comparator disabled 1 = comparator enabled
VBDTCTEN	vbus comparator enable 0 = comparators (except session end) disabled 1 = comparators (except session end) enabled
PHYPLLON	USB PHY PLL suspend override 0 = Normal PLL operation 1 = Override PLL suspend state
CLKO1SEL	CLK_OUT1 frequency select 0 = 24 MHz 1 = 12 MHz
OSCPDWN	USB PHY oscillator power down control 0 = PHY oscillator powered 1 = PHY oscillator power off
PHYPDWN	USB PHY power down control 0 = PHY powered 1 = PHY power off

5.14.1 USB2.0 Peripheral Register Description(s)

The USB register memory mapping is shown in Table 5-61.

Table 5-61. USB 2.0 Register Descriptions

Address	Acronym	Register Description
0x01C6 4000	REVR	Revision Register
0x01C6 4004	CTRLR	Control Register
0x01C6 4008	STATR	Status Register
0x01C6 400C	EMUR	Emulation Register
0x01C6 4010	RNDISR	RNDIS Register
0x01C6 4014	AUTOREQ	Auto Request Register
0x01C6 4018	Reserved	Reserved
0x01C6 401C	Reserved	Reserved
0x01C6 4020	INTSRCR	USB Interrupt Source Register
0x01C6 4024	INTSETR	USB Interrupt Source Set Register
0x01C6 4028	INTCLRR	USB Interrupt Source Clear Register
0x01C6 402C	INTMSKR	USB Interrupt Mask Register
0x01C6 4030	INTMSKSETR	USB Interrupt Mask Set Register
0x01C6 034	INTMSKCLRR	USB Interrupt Mask Clear Register
0x01C6 4038	INTMASKEDR	USB Interrupt Source Masked Register
0x01C6 403C	EOIR	USB End of Interrupt Register
0x01C6 4040	INTVECTR	USB Interrupt Vector Register
0x01C6 4044	Reserved	Reserved
0x01C6 407C	Reserved	Reserved
0x01C6 4080	TCPPICR	TX CPPI Control Register
0x01C6 4084	TCPPITDR	TX CPPI Teardown Register
0x01C6 4088	TCPPIEOIR	TX CPPI DMA Controller End of Interrupt Register
0x01C6 408C	TCPPIIVECTR	TX CPPI DMA Controller Interrupt Vector Register
0x01C6 4090	TCPPIMSKSR	TX CPPI Masked Status Register
0x01C6 4094	TCPPIRAWSR	TX CPPI Raw Status Register
0x01C6 4098	TCPPIIENSETR	TX CPPI Interrupt Enable Set Register
0x01C6 409C	TCPPIIENCLRR	TX CPPI Interrupt Enable Clear Register
0x01C6 40A0	Reserved	Reserved
0x01C6 40B0	Reserved	Reserved
0x01C6 40C0	RCPPICR	RX CPPI Control Register
0x01C6 40CA	Reserved	Reserved
0x01C6 40CC	Reserved	Reserved
0x01C6 40D0	RCPPIMSKSR	RX CPPI Masked Status Register
0x01C6 40D4	RCPPIRAWSR	RX CPPI Raw Status Register
0x01C6 40D8	RCPPIENSETR	RX CPPI Interrupt Enable Set Register
0x01C6 40DC	RCPPIIENCLRR	RX CPPI Interrupt Enable Clear Register
0x01C6 40E0	RBUFCNT0	RX Buffer Count 0 Register
0x01C6 40E4	RBUFCNT1	RX Buffer Count 1 Register
0x01C6 40E8	RBUFCNT2	RX Buffer Count 2 Register
0x01C6 40EC	RBUFCNT3	RX Buffer Count 3 Register
TX/RX CCPI Channel 0 State Block		
0x01C6 4100	TCPPIDMASTATEW0	TX CPPI DMA State Word 0

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Table 5-61. USB 2.0 Register Descriptions (continued)

Address	Acronym	Register Description
0x01C6 4104	TCPPIDMASTATEW1	TX CPPI DMA State Word 1
0x01C6 4108	TCPPIDMASTATEW2	TX CPPI DMA State Word 2
0x01C6 410C	TCPPIDMASTATEW3	TX CPPI DMA State Word 3
0x01C6 4110	TCPPIDMASTATEW4	TX CPPI DMA State Word 4
0x01C6 4114	TCPPIDMASTATEW5	TX CPPI DMA State Word 5
0x01C6 4118	TCPPIDMASTATEW6	TX CPPI DMA State Word 6
0x01C6 411C	TCPPICOMPPTR	TX CPPI Completion Pointer
0x01C6 4120	RCPPIDMASTATEW0	RX CPPI DMA State Word 0
0x01C6 4124	RCPPIDMASTATEW1	RX CPPI DMA State Word 1
0x01C6 4128	RCPPIDMASTATEW2	RX CPPI DMA State Word 2
0x01C6 412C	RCPPIDMASTATEW3	RX CPPI DMA State Word 3
0x01C6 4130	RCPPIDMASTATEW4	RX CPPI DMA State Word 4
0x01C6 4134	RCPPIDMASTATEW5	RX CPPI DMA State Word 5
0x01C6 4138	RCPPIDMASTATEW6	RX CPPI DMA State Word 6
0x01C6 413C	RCPPICOMPPTR	RX CPPI Completion Pointer
TX/RX CCPI Channel 1 State Block		
0x01C6 4140	TCPPIDMASTATEW0	TX CPPI DMA State Word 0
0x01C6 4144	TCPPIDMASTATEW1	TX CPPI DMA State Word 1
0x01C6 4148	TCPPIDMASTATEW2	TX CPPI DMA State Word 2
0x01C6 414C	TCPPIDMASTATEW3	TX CPPI DMA State Word 3
0x01C6 4150	TCPPIDMASTATEW4	TX CPPI DMA State Word 4
0x01C6 4154	TCPPIDMASTATEW5	TX CPPI DMA State Word 5
0x01C6 4158	TCPPIDMASTATEW6	TX CPPI DMA State Word 6
0x01C6 415C	TCPPICOMPPTR	TX CPPI Completion Pointer
0x01C6 4160	RCPPIDMASTATEW0	RX CPPI DMA State Word 0
0x01C6 4164	RCPPIDMASTATEW1	RX CPPI DMA State Word 1
0x01C6 4168	RCPPIDMASTATEW2	RX CPPI DMA State Word 2
0x01C6 416C	RCPPIDMASTATEW3	RX CPPI DMA State Word 3
0x01C6 4170	RCPPIDMASTATEW4	RX CPPI DMA State Word 4
0x01C6 4174	RCPPIDMASTATEW5	RX CPPI DMA State Word 5
0x01C6 4178	RCPPIDMASTATEW6	RX CPPI DMA State Word 6
0x01C6 417C	RCPPICOMPPTR	RX CPPI Completion Pointer
TX/RX CCPI Channel 2 State Block		
0x01C6 4180	TCPPIDMASTATEW0	TX CPPI DMA State Word 0
0x01C6 4184	TCPPIDMASTATEW1	TX CPPI DMA State Word 1
0x01C6 4188	TCPPIDMASTATEW2	TX CPPI DMA State Word 2
0x01C6 418C	TCPPIDMASTATEW3	TX CPPI DMA State Word 3
0x01C6 4190	TCPPIDMASTATEW4	TX CPPI DMA State Word 4
0x01C6 4194	TCPPIDMASTATEW5	TX CPPI DMA State Word 5
0x01C6 4198	TCPPIDMASTATEW6	TX CPPI DMA State Word 6
0x01C6 419C	TCPPICOMPPTR	TX CPPI Completion Pointer
0x01C6 41A0	RCPPIDMASTATEW0	RX CPPI DMA State Word 0
0x01C6 41A4	RCPPIDMASTATEW1	RX CPPI DMA State Word 1
0x01C6 41A8	RCPPIDMASTATEW2	RX CPPI DMA State Word 2
0x01C6 41AC	RCPPIDMASTATEW3	RX CPPI DMA State Word 3
0x01C6 41BA	RCPPIDMASTATEW4	RX CPPI DMA State Word 4
0x01C6 41B4	RCPPIDMASTATEW5	RX CPPI DMA State Word 5

Table 5-61. USB 2.0 Register Descriptions (continued)

Address	Acronym	Register Description
0x01C6 41B8	RCPPIDMASTATEW6	RX CPPI DMA State Word 6
0x01C6 41BC	RCPPICOMPPTR	RX CPPI Completion Pointer
TX/RX CCPI Channel 3 State Block		
0x01C6 41C0	TCPPIDMASTATEW0	TX CPPI DMA State Word 0
0x01C6 41C4	TCPPIDMASTATEW1	TX CPPI DMA State Word 1
0x01C6 41C8	TCPPIDMASTATEW2	TX CPPI DMA State Word 2
0x01C6 41CC	TCPPIDMASTATEW3	TX CPPI DMA State Word 3
0x01C6 41D0	TCPPIDMASTATEW4	TX CPPI DMA State Word 4
0x01C6 41D4	TCPPIDMASTATEW5	TX CPPI DMA State Word 5
0x01C6 41D8	TCPPIDMASTATEW6	TX CPPI DMA State Word 6
0x01C6 41DC	TCPPICOMPPTR	TX CPPI Completion Pointer
0x01C6 41E0	RCPPIDMASTATEW0	RX CPPI DMA State Word 0
0x01C6 41E4	RCPPIDMASTATEW1	RX CPPI DMA State Word 1
0x01C6 41E8	RCPPIDMASTATEW2	RX CPPI DMA State Word 2
0x01C6 41EC	RCPPIDMASTATEW3	RX CPPI DMA State Word 3
0x01C6 41F0	RCPPIDMASTATEW4	RX CPPI DMA State Word 4
0x01C6 41F4	RCPPIDMASTATEW5	RX CPPI DMA State Word 5
0x01C6 41F8	RCPPIDMASTATEW6	RX CPPI DMA State Word 6
0x01C6 41FC	RCPPICOMPPTR	RX CPPI Completion Pointer
0x01C6 4200	Reserved	Reserved
0x01C6 43FC	Reserved	Reserved
0x01C6 4400	FADDR	Function Address Register
0x01C6 4401	POWER	Power Management Register
0x01C6 4402	INTRTX	Interrupt Register for Endpoint 0 plus TX Endpoints 1 to 4
0x01C6 4404	INTRRX	Interrupt Register for RX Endpoints 1 to 4
0x01C6 4406	INTRTXE	Interrupt Enable Register for INTRTX
0x01C6 4408	INTRRXE	Interrupt Enable Register for INTRRX
0x01C6 440A	INTRUSB	Interrupt Register for Common USB Interrupts
0x01C6 440B	INTRUSBE	Interrupt Enable Register for INTRUSB
0x01C6 440C	FRAME	Frame Number Register
0x01C6 440E	INDEX	Index register for selecting the endpoint status and control registers
0x01C6 440F	TESTMODE	Register to enable the USB 2.0 test modes
0x01C6 4410	TXMAXP	Maximum packet size for peripheral/host TX endpoint (Index register set to select Endpoints 1 - 4 only)
0x01C6 4411	Reserved	Reserved
0x01C6 4412	PERI_CSR0	Control Status register for Endpoint 0 in Peripheral mode. (Index register set to select Endpoint 0)
0x01C6 4412	HOST_CSR0	Control Status register for Endpoint 0 in Host mode. (Index register set to select Endpoint 0)
0x01C6 4412	PERI_TXCSR	Control Status register for peripheral TX endpoint. (Index register set to select Endpoints 1 - 4)
0x01C6 4412	HOST_TXCSR	Control Status register for host TX endpoint. (Index register set to select Endpoints 1 - 4)
0x01C6 4413	Reserved	Reserved
0x01C6 4414	RXMAXP	Maximum packet size for peripheral/host RX endpoint (Index register set to select Endpoints 1 - 4 only)
0x01C6 4416	PERI_RXCSR	Control Status register for peripheral RX endpoint. (Index register set to select Endpoints 1 - 4)
0x01C6 4416	HOST_RXCSR	Control Status register for host RX endpoint. (Index register set to select Endpoints 1 - 4)

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Table 5-61. USB 2.0 Register Descriptions (continued)

Address	Acronym	Register Description
0x01C6 4418	COUNT0	Number of received bytes in Endpoint 0 FIFO. (Index register set to select Endpoint 0)
0x01C6 4418	RXCOUNT	Number of bytes in host RX endpoint FIFO. (Index register set to select Endpoints 1 - 4)
0x01C6 441A	HOST_TYPE0	Defines the speed of Endpoint 0
0x01C6 441A	HOST_TXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host TX endpoint. (Index register set to select Endpoints 1 - 4 only)
0x01C6 441B	HOST_NAKLIMIT0	Sets the NAK response timeout on Endpoint 0. (Index register set to select Endpoint 0)
0x01C6 441B	HOST_TXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host TX endpoint. (Index register set to select Endpoints 1 - 4 only)
0x01C6 441C	HOST_RXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host RX endpoint. (Index register set to select Endpoints 1 - 4 only)
0x01C6 441D	HOST_RXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host RX endpoint. (Index register set to select Endpoints 1 - 4 only)
0x01C6 441F	CONFIGDATA	Returns details of core configuration (Index register set to select Endpoint 0)
0x01C6 441F	FIFOSIZE	Returns the configured size of the selected RX FIFO and TX FIFOs (Endpoints 1 - 4 only)
0x01C6 4420	FIFO0	TX and RX FIFO Register for Endpoint 0
0x01C6 4424	FIFO1	TX and RX FIFO Register for Endpoint 1
0x01C6 4428	FIFO2	TX and RX FIFO Register for Endpoint 2
0x01C6 442C	FIFO3	TX and RX FIFO Register for Endpoint 3
0x01C6 4430	FIFO4	TX and RX FIFO Register for Endpoint 4
0x01C6 4434	Reserved	Reserved
0x01C6 445C	Reserved	Reserved
0x01C6 4462	TXFIFOSZ	TX Endpoint FIFO Size (Index register set to select Endpoints 0 - 4 only)
0x01C6 4463	RXFIFOSZ	RX Endpoint FIFO Size (Index register set to select Endpoints 0 - 4 only)
0x01C6 4464	TXFIFOADDR	TX Endpoint FIFO Address (Index register set to select Endpoints 0 - 4 only)
0x01C6 4466	RXFIFOADDR	RX Endpoint FIFO Address (Index register set to select Endpoints 0 - 4 only)
Target Endpoint Control Registers (Valid Only in Host Mode) - EPTRG0		
0x01C6 4480	TXFUNCADDR	Address of the target function that has to be accessed through the associated TX Endpoint
0x01C6 4482	TXHUBADDR	Address of the hub that has to be accessed through the associated TX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
0x01C6 4483	TXHUBPORT	Port of the hub that has to be accessed through the associated TX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
0x01C6 4484	RXFUNCADDR	Address of the target function that has to be accessed through the associated RX Endpoint
0x01C6 4486	RXHUBADDR	Address of the hub that has to be accessed through the associated RX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
0x01C6 4487	RXHUBPORT	Port of the hub that has to be accessed through the associated RX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
Target Endpoint Control Registers (Valid Only in Host Mode) - EPTRG1		
0x01C6 4488	TXFUNCADDR	Address of the target function that has to be accessed through the associated TX Endpoint
0x01C6 448A	TXHUBADDR	Address of the hub that has to be accessed through the associated TX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub

Table 5-61. USB 2.0 Register Descriptions (continued)

Address	Acronym	Register Description
0x01C6 448B	TXHUBPORT	Port of the hub that has to be accessed through the associated TX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
0x01C6 448C	RXFUNCADDR	Address of the target function that has to be accessed through the associated RX Endpoint
0x01C6 448E	RXHUBADDR	Address of the hub that has to be accessed through the associated RX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
0x01C6 448F	RXHUBPORT	Port of the hub that has to be accessed through the associated RX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
Target Endpoint Control Registers (Valid Only in Host Mode) - EPTRG2		
0x01C6 4490	TXFUNCADDR	Address of the target function that has to be accessed through the associated TX Endpoint
0x01C6 4492	TXHUBADDR	Address of the hub that has to be accessed through the associated TX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
0x01C6 4493	TXHUBPORT	Port of the hub that has to be accessed through the associated TX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
0x01C6 4494	RXFUNCADDR	Address of the target function that has to be accessed through the associated RX Endpoint
0x01C6 4496	RXHUBADDR	Address of the hub that has to be accessed through the associated RX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
0x01C6 4497	RXHUBPORT	Port of the hub that has to be accessed through the associated RX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
Target Endpoint Control Registers (Valid Only in Host Mode) - EPTRG3		
0x01C6 4498	TXFUNCADDR	Address of the target function that has to be accessed through the associated TX Endpoint
0x01C6 449A	TXHUBADDR	Address of the hub that has to be accessed through the associated TX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
0x01C6 449B	TXHUBPORT	Port of the hub that has to be accessed through the associated TX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
0x01C6 449C	RXFUNCADDR	Address of the target function that has to be accessed through the associated RX Endpoint
0x01C6 449E	RXHUBADDR	Address of the hub that has to be accessed through the associated RX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
0x01C6 449F	RXHUBPORT	Port of the hub that has to be accessed through the associated RX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
Target Endpoint Control Registers (Valid Only in Host Mode) - EPTRG4		
0x01C6 44A0	TXFUNCADDR	Address of the target function that has to be accessed through the associated TX Endpoint
0x01C6 44A2	TXHUBADDR	Address of the hub that has to be accessed through the associated TX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
0x01C6 44A3	TXHUBPORT	Port of the hub that has to be accessed through the associated TX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
0x01C6 44A4	RXFUNCADDR	Address of the target function that has to be accessed through the associated RX Endpoint

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Table 5-61. USB 2.0 Register Descriptions (continued)

Address	Acronym	Register Description
0x01C6 44A6	RXHUBADDR	Address of the hub that has to be accessed through the associated RX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
0x01C6 44A7	RXHUBPORT	Port of the hub that has to be accessed through the associated RX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub
0x01C6 44A8	Reserved	Reserved
0x01C6 44FC	Reserved	Reserved
Control and Status Register for Endpoints- EOCSR0		
0x01C6 4500	TXMAXP	Maximum packet size for peripheral/host TX endpoint
0x01C6 4502	PERI_CSR0	Control Status Register for Endpoint 0 in Peripheral mode
0x01C6 4502	HOST_CSR0	Control Status Register for Endpoint 0 in Host mode
0x01C6 4502	PERI_TXCSR	Control Status Register for Peripheral TX endpoint
0x01C6 4502	HOST_TXCSR	Control Status Register for Host TX endpoint
0x01C6 4504	RXMAXP	Maximum Packet Size for Peripheral/Host RX Endpoint
0x01C6 4506	PERI_RXCSR	Control Status Register for Peripheral RX Endpoint
0x01C6 4506	HOST_RXCSR	Control Status Register for Host RX Endpoint
0x01C6 4508	COUNT0	Number of Received Bytes in Endpoint 0 FIFO
0x01C6 4508	RXCOUNT	Number of Bytes in Host RX Endpoint FIFO
0x01C6 450A	HOST_TYPE0	Defines the Speed of Endpoint 0
0x01C6 450A	HOST_TXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host TX endpoint.
0x01C6 450B	HOST_NAKLIMIT0	Sets the NAK response timeout on Endpoint 0.
0x01C6 450B	HOST_TXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host TX endpoint.
0x01C6 450C	HOST_RXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host RX endpoint.
0x01C6 450D	HOST_RXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host RX endpoint.
0x01C6 450F	CONFIGDATA	Returns details of core configuration
0x01C6 450F	FIFOSIZE	Returns the configured size of the selected RX FIFO and TX FIFOs
Control and Status Register for Endpoints- EOCSR1		
0x01C6 4510	TXMAXP	Maximum Packet size for Peripheral/Host TX Endpoint
0x01C6 4512	PERI_CSR0	Control Status Register for Endpoint 0 in Peripheral Mode
0x01C6 4512	HOST_CSR0	Control Status Register for Endpoint 0 in Host Mode
0x01C6 4512	PERI_TXCSR	Control Status Register for Peripheral TX Endpoint
0x01C6 4512	HOST_TXCSR	Control Status Register for Host TX Endpoint
0x01C6 4514	RXMAXP	Maximum Packet Size for Peripheral/Host RX Endpoint
0x01C6 4516	PERI_RXCSR	Control Status Register for Peripheral RX Endpoint
0x01C6 4516	HOST_RXCSR	Control Status Register for Host RX Endpoint
0x01C6 4518	COUNT0	Number of Received Bytes in Endpoint 0 FIFO
0x01C6 4518	RXCOUNT	Number of Bytes in Host RX Endpoint FIFO
0x01C6 451A	HOST_TYPE0	Defines the Speed of Endpoint 0
0x01C6 451A	HOST_TXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host TX endpoint.
0x01C6 451B	HOST_NAKLIMIT0	Sets the NAK response timeout on Endpoint 0
0x01C6 451B	HOST_TXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host TX endpoint.
0x01C6 451C	HOST_RXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host RX endpoint.

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Table 5-61. USB 2.0 Register Descriptions (continued)

Address	Acronym	Register Description
0x01C6 451D	HOST_RXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host RX endpoint.
0x01C6 451F	CONFIGDATA	Returns details of core configuration
0x01C6 451F	FIFOSIZE	Returns the configured size of the selected RX FIFO and TX FIFOs
Control and Status Register for Endpoints- EOCSR2		
0x01C6 4520	TXMAXP	Maximum Packet Size for Peripheral/Host TX Endpoint
0x01C6 4522	PERI_CSR0	Control Status Register for Endpoint 0 in Peripheral Mode
0x01C6 4522	HOST_CSR0	Control Status Register for Endpoint 0 in Host Mode
0x01C6 4522	PERI_TXCSR	Control Status Register for Peripheral TX Endpoint
0x01C6 4522	HOST_TXCSR	Control Status Register for Host TX Endpoint
0x01C6 4524	RXMAXP	Maximum Packet Size for Peripheral/Host RX Endpoint
0x01C6 4526	PERI_RXCSR	Control Status Register for Peripheral RX Endpoint
0x01C6 4526	HOST_RXCSR	Control Status Register for Host RX Endpoint
0x01C6 4528	COUNT0	Number of Received Bytes in Endpoint 0 FIFO
0x01C6 4528	RXCOUNT	Number of Bytes in Host RX Endpoint FIFO
0x01C6 452A	HOST_TYPE0	Defines the Speed of Endpoint 0
0x01C6 452A	HOST_TXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host TX endpoint.
0x01C6 452B	HOST_NAKLIMIT0	Sets the NAK response timeout on Endpoint 0.
0x01C6 452B	HOST_TXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host TX endpoint.
0x01C6 452C	HOST_RXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host RX endpoint.
0x01C6 452D	HOST_RXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host RX endpoint.
0x01C6 452F	CONFIGDATA	Returns details of core configuration
0x01C6 452F	FIFOSIZE	Returns the configured size of the selected RX FIFO and TX FIFOs
Control and Status Register for Endpoints- EOCSR3		
0x01C6 4530	TXMAXP	Maximum Packet Size for Peripheral/Host TX Endpoint
0x01C6 4532	PERI_CSR0	Control Status Register for Endpoint 0 in Peripheral Mode
0x01C6 4532	HOST_CSR0	Control Status Register for Endpoint 0 in Host Mode
0x01C6 4532	PERI_TXCSR	Control Status Register for Peripheral TX Endpoint
0x01C6 4532	HOST_TXCSR	Control Status Register for Host TX Endpoint
0x01C6 4534	RXMAXP	Maximum Packet Size for Peripheral/Host RX Endpoint
0x01C6 4536	PERI_RXCSR	Control Status Register for Peripheral RX Endpoint
0x01C6 4536	HOST_RXCSR	Control Status Register for Host RX Endpoint
0x01C6 4538	COUNT0	Number of Received Bytes in Endpoint 0 FIFO
0x01C6 4538	RXCOUNT	Number of Bytes in Host RX Endpoint FIFO
0x01C6 453A	HOST_TYPE0	Defines the Speed of Endpoint 0
0x01C6 453A	HOST_TXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host TX endpoint.
0x01C6 453B	HOST_NAKLIMIT0	Sets the NAK response timeout on Endpoint 0.
0x01C6 453B	HOST_TXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host TX endpoint.
0x01C6 453C	HOST_RXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host RX endpoint.
0x01C6 453D	HOST_RXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host RX endpoint.
0x01C6 453F	CONFIGDATA	Returns details of core configuration
0x01C6 453F	FIFOSIZE	Returns the configured size of the selected RX FIFO and TX FIFOs

Table 5-61. USB 2.0 Register Descriptions (continued)

Address	Acronym	Register Description
Control and Status Register for Endpoints- EOCSR4		
0x01C6 4540	TXMAXP	Maximum Packet Size for Peripheral/Host TX Endpoint
0x01C6 4542	PERI_CSR0	Control Status Register for Endpoint 0 in Peripheral Mode
0x01C6 4542	HOST_CSR0	Control Status Register for Endpoint 0 in Host Mode
0x01C6 4542	PERI_TXCSR	Control Status Register for Peripheral TX Endpoint
0x01C6 4542	HOST_TXCSR	Control Status Register for Host TX Endpoint
0x01C6 4544	RXMAXP	Maximum Packet Size for Peripheral/Host RX Endpoint
0x01C6 4543	PERI_RXCSR	Control Status Register for Peripheral RX Endpoint
0x01C6 4543	HOST_RXCSR	Control Status Register for Host RX Endpoint
0x01C6 4548	COUNT0	Number of Received Bytes in Endpoint 0 FIFO
0x01C6 4548	RXCOUNT	Number of Bytes in Host RX Endpoint FIFO
0x01C6 454A	HOST_TYPE0	Defines the Speed of Endpoint 0
0x01C6 454A	HOST_TXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host TX endpoint.
0x01C6 454B	HOST_NAKLIMIT0	Sets the NAK response timeout on Endpoint 0.
0x01C6 454B	HOST_TXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host TX endpoint.
0x01C6 454C	HOST_RXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host RX endpoint.
0x01C6 454D	HOST_RXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host RX endpoint.
0x01C6 454F	CONFIGDATA	Returns details of core configuration
0x01C6 454F	FIFOSIZE	Returns the configured size of the selected RX FIFO and TX FIFOs
0x01C6 4560	Reserved	Reserved
0x01C6 5FFF	Reserved	Reserved

5.14.2 USB2.0 Electrical Data/Timing

Table 5-62. Switching Characteristics Over Recommended Operating Conditions for USB2.0 (see Figure 5-51)

NO.	PARAMETER		-594 LOW SPEED 1.5 Mbps MIN	LOW SPEED MAX	FULL SPEED 12 Mbps MIN	FULL SPEED MAX	HIGH SPEED 480 Mbps MIN	HIGH SPEED MAX	UNIT
1	$t_{r(D)}$	Rise time, USB_DP and USB_DM signals(1)	75	300	4	20	0.5		ns
2	$t_{f(D)}$	Fall time, USB_DP and USB_DM signals(1)	75	300	4	20	0.5		ns
3	t_{rfM}	Rise/Fall time, matching(2)	80	125	90	111.11	TBD	TBD	%
4	V_{CRS}	Output signal cross-over voltage(1)	1.3	2	1.3	2	–	–	V
5	$t_{jr(source)NT}$	Source (Host) Driver jitter, next transition		2		2		TBD(3)	ns
	$t_{jr(FUNC)NT}$	Function Driver jitter, next transition		25		2		TBD(3)	ns
6	$t_{jr(source)PT}$	Source (Host) Driver jitter, paired transition(4)		1		1		TBD(3)	ns
	$t_{jr(FUNC)PT}$	Function Driver jitter, paired transition		10		1		TBD(3)	ns
7	$t_{w(EOPT)}$	Pulse duration, EOP transmitter	1250	1500	160	175	–	–	ns
8	$t_{w(EOPR)}$	Pulse duration, EOP receiver	670		82		–		ns
9	$t_{(DRATE)}$	Data Rate		1.5		12		480	Mb/s

(1) Low Speed: C_L = 200 pF, Full Speed: C_L = 50 pF, High Speed: C_L = TBD pF
(2) $t_{RFM} = (t_r/t_f)$ x 100. [Excluding the first transaction from the Idle state.]
(3) For more detailed information, see the Universal Serial Bus Specification Revision 2.0, Chapter 7. Electrical.
(4) $t_{jr} = t_{px(1)} - t_{px(0)}$

Table 5-62. Switching Characteristics Over Recommended Operating Conditions for USB2.0 (see Figure 5-51) (continued)

NO.	PARAMETER		-594						UNIT
			LOW SPEED 1.5 Mbps		FULL SPEED 12 Mbps		HIGH SPEED 480 Mbps		
			MIN	MAX	MIN	MAX	MIN	MAX	
10	Z_{DRV}	Driver Output Resistance	–	–	28	44	40.5	49.5	Ω

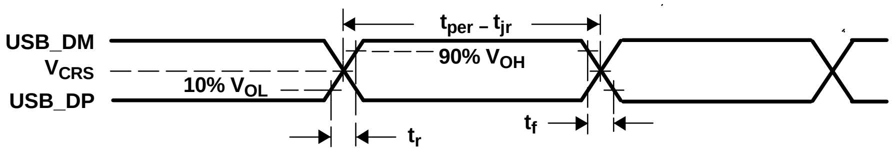

Figure 5-51. USB2.0 Integrated Transceiver Interface Timing

5.15 Universal Asynchronous Receiver/Transmitter (UART)

DM6446 has 3 UART peripherals. UART2 with the following features.

- 16-byte storage space for both the transmitter and receiver FIFOs
- 1, 4, 8, or 14 byte selectable receiver FIFO trigger level for autoflow control and DMA
- DMA signaling capability for both received and transmitted data
- Programmable auto-rts and auto-cts for autoflow control
- Frequency pre-scale values from 1 to 65,535 to generate appropriate baud rates
- Prioritized interrupts
- Programmable serial data formats
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no parity bit generation and detection
  - 1, 1.5, or 2 stop bit generation
- False start bit detection
- Line break generation and detection
- Internal diagnostic capabilities
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, and framing error simulation
- Modem control functions (CTS, RTS) on UART2.

The UART0/1/2 registers are listed in Table 5-63, Table 5-64, and Table 5-65.

5.15.1 UART Peripheral Register Description(s)

Table 5-63. UART0 Register Descriptions

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C2 0000	RBR	UART0 Receiver Buffer Register (Read Only)
0x01C2 0000	THR	UART0 Transmitter Holding Register (Write Only)
0x01C2 0004	IER	UART0 Interrupt Enable Register
0x01C2 0008	IIR	UART0 Interrupt Identification Register (Read Only)
0x01C2 0008	FCR	UART0 FIFO Control Register (Write Only)
0x01C2 000C	LCR	UART0 Line Control Register
0x01C2 0010	MCR	UART0 Modem Control Register
0x01C2 0014	LSR	UART0 Line Status Register

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Table 5-63. UART0 Register Descriptions (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C2 0018	-	Reserved
0x01C2 001C	-	Reserved
0x01C2 0020	DLL	UART0 Divisor Latch (LSB)
0x01C2 0024	DLH	UART0 Divisor Latch (MSB)
0x01C2 0028	PID1	Peripheral Identification Register 1
0x01C2 002C	PID2	Peripheral Identification Register 2
0x01C2 0030	PWREMU_MGMT	UART0 Power and Emulation Management Register
0x01C2 0034 - 0x01C2 03FF	-	Reserved

Table 5-64. UART1 Register Descriptions

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C2 0400	RBR	UART1 Receiver Buffer Register (Read Only)
0x01C2 0400	THR	UART1 Transmitter Holding Register (Write Only)
0x01C2 0404	IER	UART1 Interrupt Enable Register
0x01C2 0408	IIR	UART1 Interrupt Identification Register (Read Only)
0x01C2 0408	FCR	UART1 FIFO Control Register (Write Only)
0x01C2 040C	LCR	UART1 Line Control Register
0x01C2 0410	MCR	UART1 Modem Control Register
0x01C2 0414	LSR	UART1 Line Status Register
0x01C2 0418	-	Reserved
0x01C2 041C	-	Reserved
0x01C2 0420	DLL	UART1 Divisor Latch (LSB)
0x01C2 0424	DLH	UART1 Divisor Latch (MSB)
0x01C2 0428	PID1	Peripheral Identification Register 1
0x01C2 042C	PID2	Peripheral Identification Register 2
0x01C2 0430	PWREMU_MGMT	UART1 Power and Emulation Management Register
0x01C2 0434 - 0x01C2 07FF	-	Reserved

Table 5-65. UART2 Register Descriptions

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C2 0800	RBR	UART2 Receiver Buffer Register (Read Only)
0x01C2 0800	THR	UART2 Transmitter Holding Register (Write Only)
0x01C2 0804	IER	UART2 Interrupt Enable Register
0x01C2 0808	IIR	UART2 Interrupt Identification Register (Read Only)
0x01C2 0808	FCR	UART2 FIFO Control Register (Write Only)
0x01C2 080C	LCR	UART2 Line Control Register
0x01C2 0810	MCR	UART2 Modem Control Register
0x01C2 0814	LSR	UART2 Line Status Register
0x01C2 0818	-	Reserved
0x01C2 081C	-	Reserved
0x01C2 0820	DLL	UART2 Divisor Latch (LSB)
0x01C2 0824	DLH	UART2 Divisor Latch (MSB)
0x01C2 0828	PID1	Peripheral Identification Register 1
0x01C2 082C	PID2	Peripheral Identification Register 2
0x01C2 0830	PWREMU_MGMT	UART2 Power and Emulation Management Register
0x01C2 0834 - 0x01C2 0BFF	-	Reserved

5.15.2 UART Electrical Data/Timing

Table 5-66. Timing Requirements for UARTx Receive(1) (see Figure 5-52)

NO.			-594		UNIT
			MIN	MAX	
4	$t_{w(URXDB)}$	Pulse duration, receive data bit (RXDn) [15/30/100 pF]	0.99U	1.05U	ns
5	$t_{w(URXSB)}$	Pulse duration, receive start bit [15/30/100 pF]	0.99U	1.05U	ns

(1) U = UART baud time = 1/programmed baud rate.

Table 5-67. Switching Characteristics Over Recommended Operating Conditions for UARTx Transmit(1) (see Figure 5-52)

NO.	PARAMETER		-594		UNIT
			MIN	MAX	
1	$f_{(baud)}$	Maximum programmable baud rate		5	MHz
2	$t_{w(UTXDB)}$	Pulse duration, transmit data bit (TXDn) [15/30/100 pF]	U - 2	U + 2	ns
3	$t_{w(UTXSB)}$	Pulse duration, transmit start bit [15/30/100 pF]	U - 2	U + 2	ns

(1) U = UART baud time = 1/programmed baud rate.

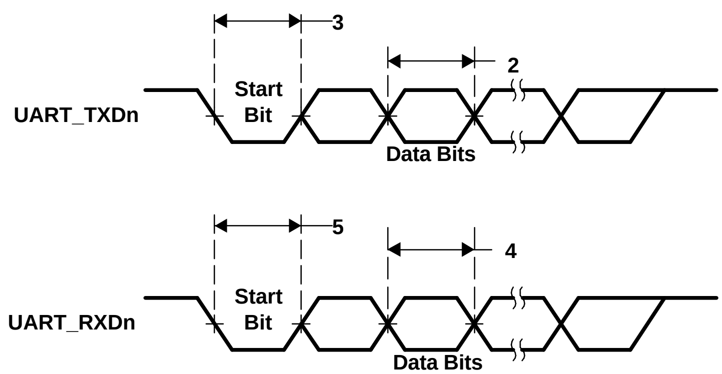

Figure 5-52. UART Transmit/Receive Timing

5.16 Serial Port Interface (SPI)

The DM6446 SPI peripheral provides a programmable length shift register which allows serial communication with other SPI devices through a 3 or 4 wire interface. The SPI supports the following features.

- Master mode operation
- 2 chip selects for interfacing to multiple slave SPI devices.
- 3 or 4 wire interface

The SPI registers are shown in Table 5-68.

5.16.1 SPI Peripheral Register Description(s)

Table 5-68. SPI Register Descriptions

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C6 6800	SPIGCR0	SPI Global Control Register 0
0x01C6 6804	SPIGCR1	SPI Global Control Register 1

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Table 5-68. SPI Register Descriptions (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C6 6808	SPIINT	SPI Interrupt Register
0x01C6 680C	SPILVL	SPI Interrupt Level Register
0x01C6 6810	SPIFLG	SPI Flag Status Register
0x01C6 6814	SPIPC0	SPI Pin Control Register 0
0x01C6 6818	–	Reserved
0x01C6 681C	SPIPC2	SPI Pin Control Register 2
0x01C6 6820 - 0x01C6 6838	–	Reserved
0x01C6 683C	SPIDAT1	SPI Shift Register 1
0x01C6 6840	SPIBUF	SPI Buffer Register
0x01C6 6844	SPIEMU	SPI Emulation Register
0x01C6 6848	SPIDELAY	SPI Delay Register
0x01C6 684C	SPIDEF	SPI Default Chip Select Register
0x01C6 6850	SPIFMT0	SPI Data Format Register 0
0x01C6 6854	SPIFMT1	SPI Data Format Register 1
0x01C6 6858	SPIFMT2	SPI Data Format Register 2
0x01C6 685C	SPIFMT3	SPI Data Format Register 3
0x01C6 6860	INTVEC0	SPI Interrupt Vector Register 0
0x01C6 6864	INTVEC1	SPI Interrupt Vector Register 1
0x01C6 6868 - 0x01C6 6FFF		Reserved

5.16.2 SPI Electrical Data/Timing

Table 5-69. Timing Requirements for SPI (All Modes)(1) (see Figure 5-53)

NO.			-594		UNIT
			MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, SPI_CLK	26.1	56888.89	ns
2	$t_{w(CLKH)}$	Pulse duration, SPI_CLK high (All Master Modes)	0.45*T	0.55*T	ns
3	$t_{w(CLKL)}$	Pulse duration, SPI_CLK low (All Master Modes	0.45*T	0.55*T	ns

(1) T = $t_{c(CLK)}$ [SPI_CLK period is equal to the SPI module clock divided by a configurable divider.]

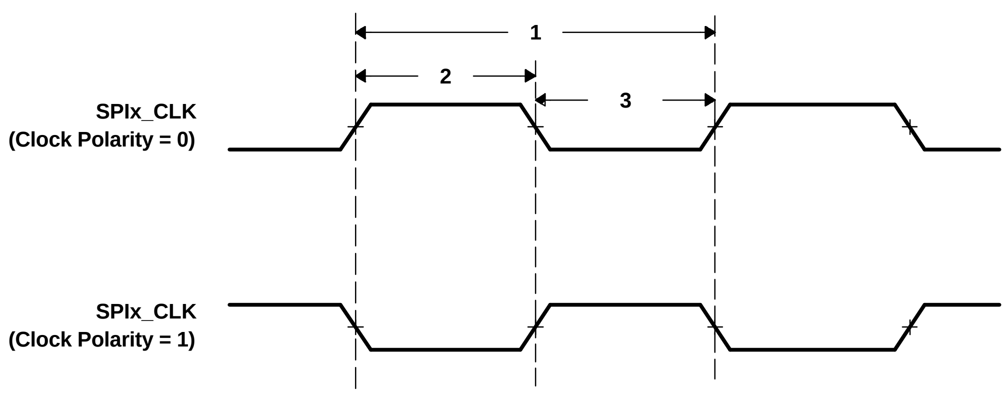

Figure 5-53. SPI_CLK Timing

SPI Master Mode Timings (Clock Phase = 0)

Table 5-70. Timing Requirements for SPI Master Mode [Clock Phase = 0] (1)(see Figure 5-54)

NO.				-594 MIN	-594 MAX	UNIT
4	$t_{su(DIV-CLKL)}$	Setup time, SPI_DI (input) valid before SPI_CLK (output) falling edge	Clock Polarity = 0	0.5P + TBD		ns
5	$t_{su(DIV-CLKH)}$	Setup time, SPI_DI (in put) valid before SPI_CLK (output) rising edge	Clock Polarity = 1	0.5P + TBD		ns
6	$t_{h(CLKL-DIV)}$	Hold time, SPI_DI (input) valid after SPI_CLK (output) falling edge	Clock Polarity = 0	0.5P + TBD		ns
7	$t_{h(CLKH-DIV)}$	Hold time, SPI_DI (input) valid after SPI_CLK (output) rising edge	Clock Polarity = 1	0.5P + TBD		ns

(1) P = Period of the SPI module clock in nanoseconds (P = PLL1/6).

Table 5-71. Switching Characteristics Over Recommended Operating Conditions for SPI Master Mode [Clock Phase = 0](1) (see Figure 5-54)

NO.	PARAMETER			-594 MIN	-594 MAX	UNIT
8	$t_{d(CLKH-DOV)}$	Delay time, SPI_CLK (output) rising edge to SPI_DO (output) transition	Clock Polarity = 0	-4	5	ns
9	$t_{d(CLKL-DOV)}$	Delay time, SPI_CLK (output) falling edge to SPI_DO (output) transition	Clock Polarity = 1	-4	5	ns
10	$t_{d(ENH-CLKH/L)}$	Delay time, SPI_EN[1:0] (output) rising edge to first SPI_CLK (output) rising or falling edge		2P + TBD		ns
11	$t_{d(CLKH/L-ENL)}$	Delay time, SPI_CLK (output) rising or falling edge to SPI_EN[1:0] (output) falling edge		2P + TBD		ns
12	$t_{d(DOHz-CLKL/H)}$	Delay time, SPI_DO (output) high impedance to SPI_CLK (output) falling or rising edge		TBD	TBD	ns

(1) P = Period of the SPI module clock in nanoseconds (P = PLL1/6).

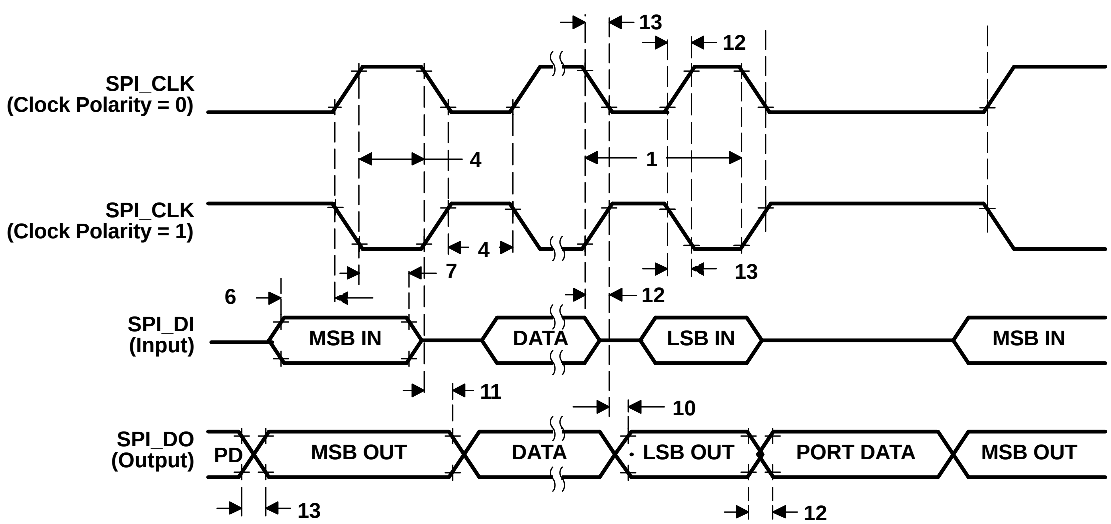

Figure 5-54. SPI Master Mode External Timing (Clock Phase = 0)

SPI Master Mode Timings (Clock Phase = 1)

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Table 5-72. Timing Requirements for SPI Master Mode [Clock Phase = 1] (see Figure 5-55)

NO.				-594 MIN	-594 MAX	UNIT
13	$t_{su(DIV-CLKL)}$	Setup time, SPI_DI (input) valid before SPI_CLK (output) rising edge	Clock Polarity = 0	0.5P + TBD		ns
14	$t_{su(DIV-CLKH)}$	Setup time, SPI_DI (in put) valid before SPI_CLK (output) falling edge	Clock Polarity = 1	0.5P + TBD		ns
15	$t_{h(CLKL-DIV)}$	Hold time, SPI_DI (input) valid after SPI_CLK (output) rising edge	Clock Polarity = 0	0.5P + TBD		ns
16	$t_{h(CLKH-DIV)}$	Hold time, SPI_DI (input) valid after SPI_CLK (output) falling edge	Clock Polarity = 1	0.5P + TBD		ns

Table 5-73. Switching Characteristics Over Recommended Operating Conditions for SPI Master Mode [Clock Phase = 1](1) (see Figure 5-55)

NO.	PARAMETER			-594 MIN	-594 MAX	UNIT
17	$t_{d(CLKL-DOV)}$	Delay time, SPI_CLK (output) falling edge to SPI_DO (output) transition	Clock Polarity = 1	-4	5	ns
18	$t_{d(CLKH-DOV)}$	Delay time, SPI_CLK (output) rising edge to SPI_DO (output) transition	Clock Polarity = 0	-4	5	ns
19	$t_{d(ENH-CLKH/L)}$	Delay time, SPI_EN[1:0] (output) rising edge to first SPI_CLK (output) rising or falling edge		2P + TBD		ns
20	$t_{d(DOHz-CLKL/H)}$	Delay time, SPI_DO (output) high impedance to SPI_CLK (output) falling or rising edge		TBD	TBD	ns

(1) P = Period of the SPI module clock in naoseconds (P = PLL1/6).

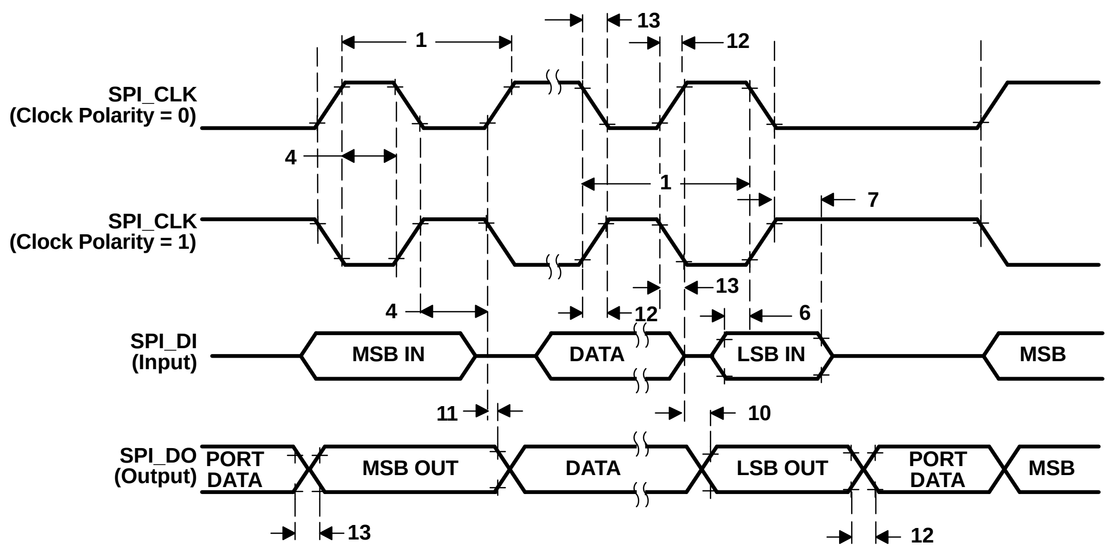

Figure 5-55. SPI Master Mode External Timing (Clock Phase = 1)

5.17 Inter-Integrated Circuit (I2C)

The inter-integrated circuit (I2C) module provides an interface between DM6446 and other devices compliant with Philips Semiconductors Inter-IC bus (I^2C-bus) specification version 2.1 and connected by way of an I^2C-bus. External components attached to this 2-wire serial bus can transmit/receive up to 8-bit data to/from the DSP through the I2C module.

The I2C port supports:

- Compatible with Philips I2C Specification Revision 2.1 (January 2000)
- Fast Mode up to 400 Kbps (no fail-safe I/O buffers)
- Noise Filter to Remove Noise 50 ns or less
- Seven- and Ten-Bit Device Addressing Modes
- Master (Transmit/Receive) and Slave (Transmit/Receive) Functionality
- Events: DMA, Interrupt, or Polling
- Slew-Rate Limited Open-Drain Output Buffers

Figure 5-56 is a block diagram of the I2C peripheral.

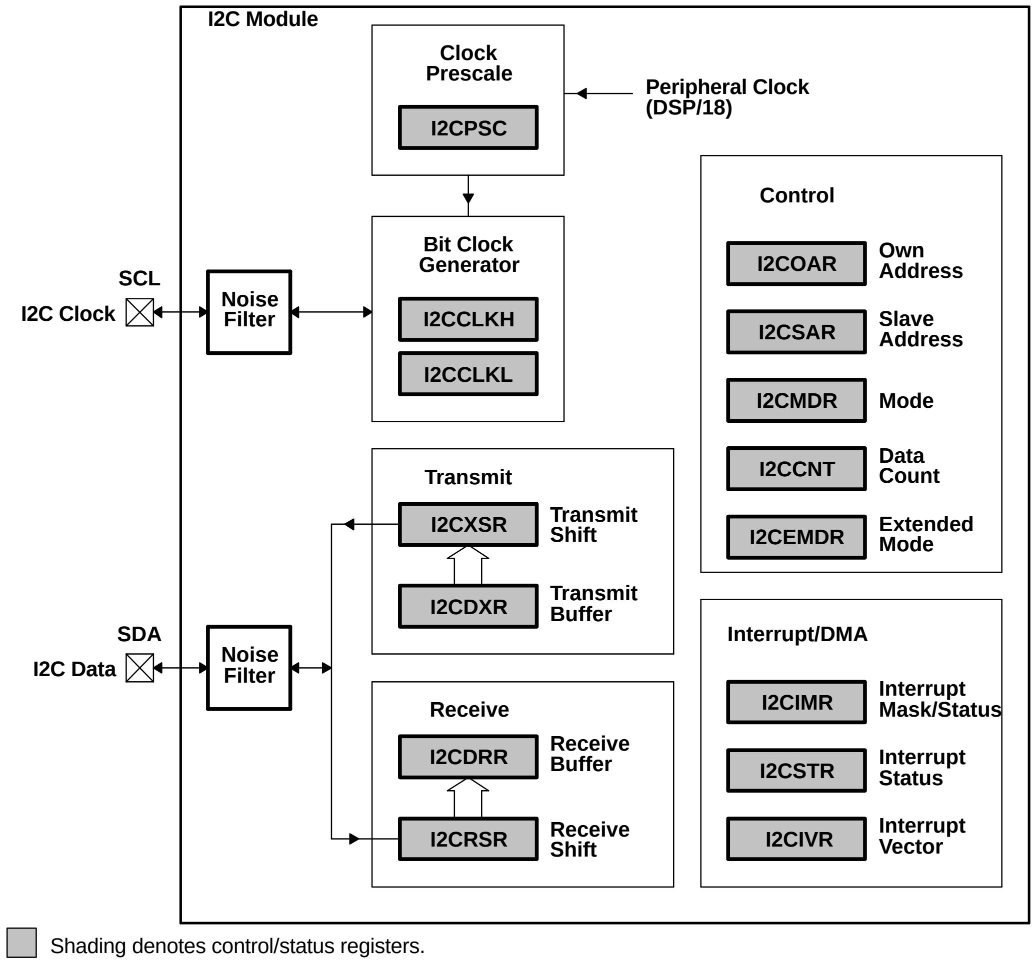

Figure 5-56. I2C Module Block Diagram

For more detailed information on the I2C peripheral, see the *Documentation Support* section for the DM6446 Inter-Integrated Circuit (I2C) Module Reference Guide.

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5.17.1 I2C Peripheral Register Description(s)

Table 5-74. I2C Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x1c2 1000	ICOAR	I2C Own Address Register
0x1c2 1004	ICIMR	I2C Interrupt Mask Register
0x1c2 1008	ICSTR	I2C Interrupt Status Register
0x1c2 100C	ICCLKL	I2C Clock Divider Low Register
0x1c2 1010	ICCLKH	I2C Clock Divider High Register
0x1c2 1014	ICCNT	I2C Data Count Register
0x1c2 1018	ICDRR	I2C Data Receive Register
0x1c2 101C	ICSAR	I2C Slave Address Register
0x1c2 1020	ICDXR	I2C Data Transmit Register
0x1c2 1024	ICMDR	I2C Mode Register
0x1c2 1028	ICIVR	I2C Interrupt Vector Register
0x1c2 102C	ICEMDR	I2C Extended Mode Register
0x1c2 1030	ICPSC	I2C Prescaler Register
0x1c2 1034	ICPID1	I2C Peripheral Identification Register 1
0x1c2 1038	ICPID2	I2C Peripheral Identification Register 2
0x1c2 103C - 0x1c2 105C	-	Reserved
0x1c2 1060 - 0x1c2 13FF	-	Reserved

5.17.2 I2C Electrical Data/Timing

5.17.2.1 Inter-Integrated Circuits (I2C) Timing

Table 5-75. Timing Requirements for I2C Timings[(1)] (see Figure 5-57)

NO.			-594 STANDARD MODE MIN	-594 STANDARD MODE MAX	-594 FAST MODE MIN	-594 FAST MODE MAX	UNIT
1	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
2	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
3	$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
4	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
5	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250		100[(2)]		ns
7	$t_{h(SDA-SCLL)}$	Hold time, SDA valid after SCL low (For I^2C bus™ devices)	0[(3)]		0[(3)]	0.9[(4)]	µs
8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
9	$t_{r(SDA)}$	Rise time, SDA		1000	$20 + 0.1C_b$[(5)]	300	ns
10	$t_{r(SCL)}$	Rise time, SCL		1000	$20 + 0.1C_b$[(5)]	300	ns
11	$t_{f(SDA)}$	Fall time, SDA		300	$20 + 0.1C_b$[(5)]	300	ns
12	$t_{f(SCL)}$	Fall time, SCL		300	$20 + 0.1C_b$[(5)]	300	ns
13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
15	C_b[(5)]	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) A Fast-mode I^2C-bus™ device can be used in a Standard-mode I^2C-bus™ system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA-SCLH)}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-Bus Specification) before the SCL line is released.
(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(4) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.
(5) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

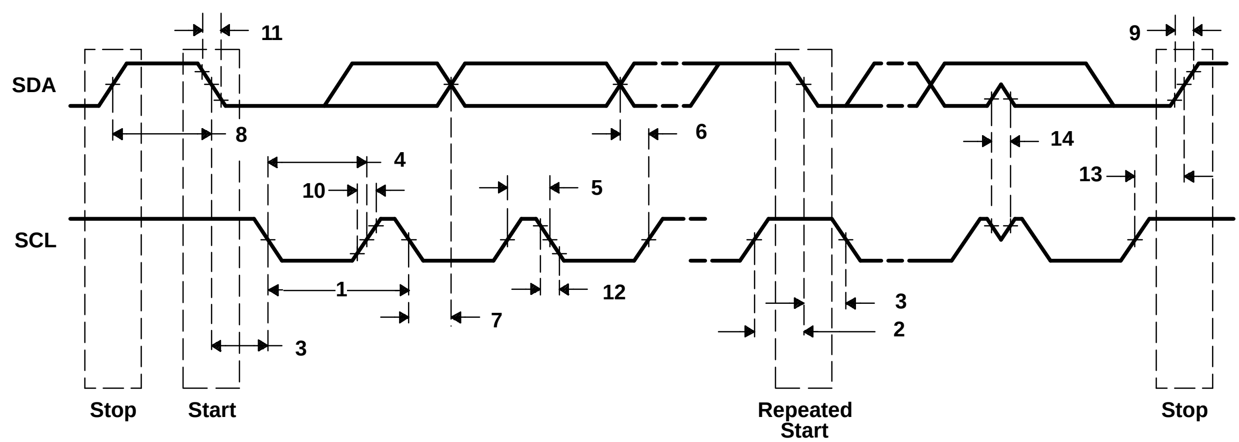

Figure 5-57. I2C Receive Timings

Table 5-76. Switching Characteristics for I2C Timings(1) (see Figure 5-58)

NO.	PARAMETER	-594 STANDARD MODE MIN	-594 STANDARD MODE MAX	-594 FAST MODE MIN	-594 FAST MODE MAX	UNIT
16	$t_{c(SCL)}$ Cycle time, SCL	10		2.5		µs
17	$t_{d(SCLH-SDAL)}$ Delay time, SCL high to SDA low (for a repeated START condition)	4.7		0.6		µs
18	$t_{d(SDAL-SCLL)}$ Delay time, SDA low to SCL low (for a START and a repeated START condition)	4		0.6		µs
19	$t_{w(SCLL)}$ Pulse duration, SCL low	4.7		1.3		µs
20	$t_{w(SCLH)}$ Pulse duration, SCL high	4		0.6		µs
21	$t_{d(SDAV-SCLH)}$ Delay time, SDA valid to SCL high	250		100		ns
22	$t_{v(SCLL-SDAV)}$ Valid time, SDA valid after SCL low (For I2C devices)	0		0	0.9	µs
23	$t_{w(SDAH)}$ Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
24	$t_{r(SDA)}$ Rise time, SDA		1000	$20 + 0.1C_b$(1)	300	ns
25	$t_{r(SCL)}$ Rise time, SCL		1000	$20 + 0.1C_b$(1)	300	ns
26	$t_{f(SDA)}$ Fall time, SDA		300	$20 + 0.1C_b$(1)	300	ns
27	$t_{f(SCL)}$ Fall time, SCL		300	$20 + 0.1C_b$(1)	300	ns
28	$t_{d(SCLH-SDAH)}$ Delay time, SCL high to SDA high (for STOP condition)	4		0.6		µs
29	C_p Capacitance for each I2C pin		10		10	pF

(1) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

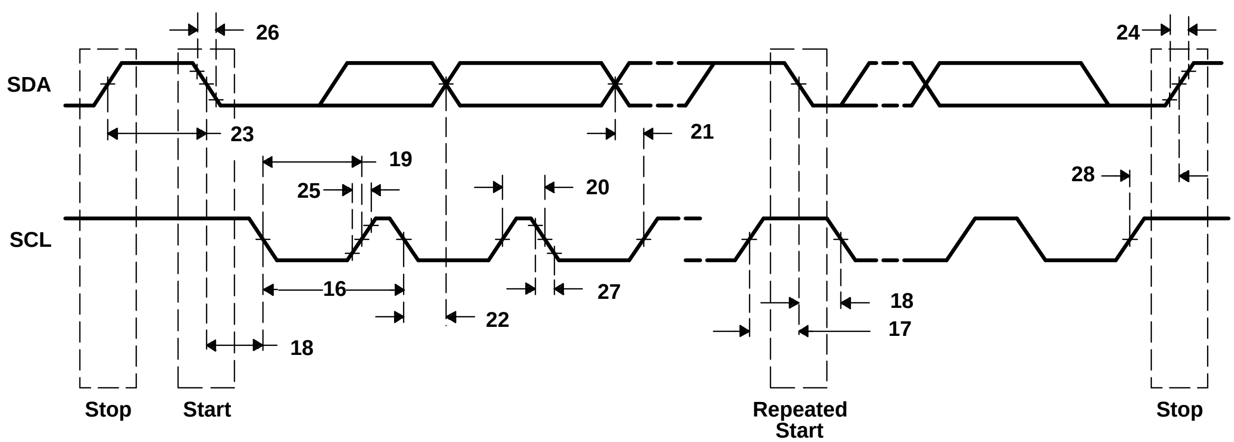

Figure 5-58. I2C Transmit Timings

5.18 Audio Serial Port (ASP)

The ASP provides these functions:

- Full-duplex communication
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected analog-to-digital (A/D) and digital-to-analog (D/A) devices
- External shift clock or an internal, programmable frequency shift clock for data transfer

For more detailed information on the ASP peripheral, see the *Documentation Support* section for the Audio Serial Port (ASP) Reference Guide.

5.18.1 ASP Peripheral Register Description(s)

Table 5-77. ASP Register Descriptions

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01E0 2000	DRR	ASP Data Receive Register
0x01E0 2004	DXR	ASP Data Transmit Register
0x01E0 2008	SPCR	ASP Serial Port Control Register
0x01E0 200C	RCR	ASP Receive Control Register
0x01E0 2010	XCR	ASP Transmit Control Register
0x01E0 2014	SRGR	ASP Sample Rate Generator Register
0x01E0 2018 - 0x01E0 2023	–	Reserved
0x01E0 2024	PCR	ASP Pin Control Register
0x01E0 2028 - 0x01E0 2047	–	Reserved
0x01E0 2048 - 0x01E0 3FFF	–	Reserved

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5.18.2 *ASP Electrical Data/Timing*

5.18.2.1 Audio Serial Port (ASP) Timing

Table 5-78. Timing Requirements for ASP(1) (see Figure 5-59)

NO.				-594		UNIT
				MIN	MAX	
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	38.5		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	$0.5t_{c(CKRX)}$ - 1(2)		ns
5	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	9		ns
			CLKR ext	1.3		
6	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	6		ns
			CLKR ext	3		
7	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	8		ns
			CLKR ext	0.9		
8	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	3		ns
			CLKR ext	3.1		
10	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	9		ns
			CLKX ext	1.3		
11	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	6		ns
			CLKX ext	3		

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) This parameter applies to the maximum ASP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

Table 5-79. Switching Characteristics Over Recommended Operating Conditions for ASP[(1)(2)] (see Figure 5-59)

NO.	PARAMETER			-594 MIN	-594 MAX	UNIT
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X int	38.5[(3)(4)]		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X int	C - 1[(5)]	C + 1[(5)]	ns
4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid	CLKR int	-2.1	3	ns
			CLKR ext	1.7	4	
9	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid	CLKX int	-1.7	3	ns
			CLKX ext	1.7	4	
12	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	CLKX int	-3.9	4	ns
			CLKX ext	2.1	4	
13	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	CLKX int	-3.9 + D1[(6)]	4 + D2[(6)]	ns
			CLKX ext	2.1 + D1[(6)]	4 + D2[(6)]	ns
14	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	FSX int	-2.3 + D1[(7)]	4 + D2[(7)]	ns
			FSX ext	1.9 + D1[(7)]	4 + D2[(7)]	

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) Minimum delay times also represent minimum output hold times.
(3) Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. Minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) P = 1/DSP CPU clock frequency in ns. For example, when running parts at 594 MHz, use P = 1.68 ns.
(5) C = H or L
S = sample rate generator input clock = 4P if CLKSM = 1 (P = 1/CPU clock frequency)
S = sample rate generator input clock = Not Supported if CLKSM = 0 (no CLKS pin on DM6446)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
H = (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
L = (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
CLKGDV should be set appropriately to ensure the ASP bit rate does not exceed the maximum limit (see footnote above).
(6) Extra delay from CLKX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 4P, D2 = 8P
(7) Extra delay from FSX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 4P, D2 = 8P

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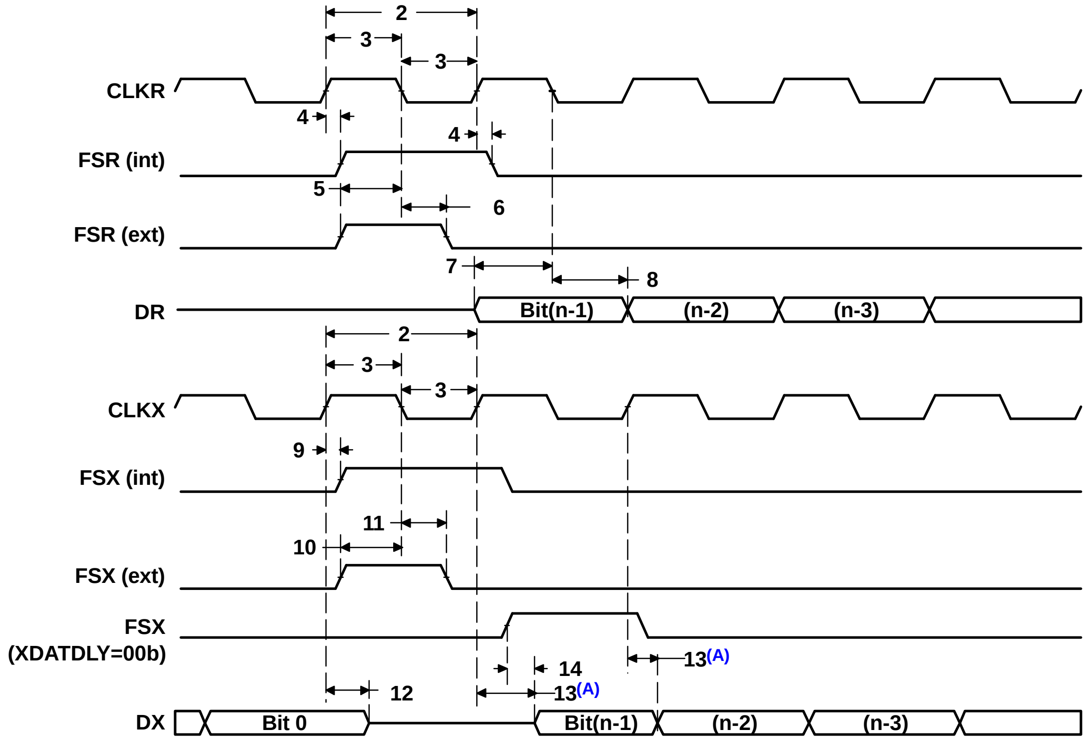

A. Parameter No. 13 applies to the first data bit *only* when XDATDLY ≠ 0.

A. Parameter No. 13 applies to the first data bit *only* when XDATDLY ≠ 0.

Figure 5-59. ASP Timing

5.19 Ethernet Media Access Controller (EMAC)

The Ethernet Media Access Controller (EMAC) provides an efficient interface between DM6446 and the network. The DM6446 EMAC support both 10Base-T and 100Base-TX, or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex mode, with hardware flow control and quality of service (QOS) support.

The EMAC controls the flow of packet data from the DM6446 device to the PHY. The MDIO module controls PHY configuration and status monitoring.

Both the EMAC and the MDIO modules interface to the DSP through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module, and is considered integral to the EMAC/MDIO peripheral. The control module is also used to multiplex and control interrupts.

For the DM6446 Ethernet Media Access Controller (EMAC) / Management Data Input/Output (MDIO) Module Reference Guide which describes the DM6446 EMAC peripheral in detail, see the *Documentation Support* section . For a list of supported registers and register fields, see Table 5-80 [Ethernet MAC (EMAC) Control Registers] and Table 5-81 [EMAC Statistics Registers] in this data manual.

5.19.1 EMAC Peripheral Register Description(s)

Table 5-80. Ethernet MAC (EMAC) Control Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01C8 0000	TXIDVER	Transmit Identification and Version Register
01C8 0004	TXCONTROL	Transmit Control Register
01C8 0008	TXTEARDOWN	Transmit Teardown Register
01C8 0010	–	Reserved
01C8 0014	RXCONTROL	Receive Control Register
01C8 0018	RXTEARDOWN	Receive Teardown Register
01C8 001C - 01C8 007C	–	Reserved
01C8 0180	TXINTSTATRAW	Transmit Interrupt Status (Unmasked) Register
01C8 0184	TXINTSTATMASKED	Transmit Interrupt Status (Masked) Register
01C8 0188	TXINTMASKSET	Transmit Interrupt Mask Set Register
01C8 018C	TXINTMASKCLEAR	Transmit Interrupt Mask Clear Register
01C8 0190	MACINVECTOR	MAC Input Vector Register
01C8 0194 - 01C8 019C	–	Reserved
01C8 01A0	RXINTSTATRAW	Receive Interrupt Status (Unmasked) Register
01C8 01A4	RXINTSTATMASKED	Receive Interrupt Status (Masked) Register
01C8 01A8	RXINTMASKSET	Receive Interrupt Mask Set Register
01C8 01AC	RXINTMASKCLEAR	Receive Interrupt Mask Clear Register
01C8 01B0	MACINTSTATRAW	MAC Interrupt Status (Unmasked) Register
01C8 01B4	MACINTSTATMASKED	MAC Interrupt Status (Masked) Register
01C8 01B8	MACINTMASKSET	MAC Interrupt Mask Set Register
01C8 01BC	MACINTMASKCLEAR	MAC Interrupt Mask Clear Register
01C8 00C0 - 01C8 00FC	–	Reserved
01C8 0100	RXMBPENABLE	Receive Multicast/Broadcast/Promiscuous Channel Enable Register
01C8 0104	RXUNICASTSET	Receive Unicast Enable Set Register
01C8 0108	RXUNICASTCLEAR	Receive Unicast Clear Register
01C8 010C	RXMAXLEN	Receive Maximum Length Register
01C8 0110	RXBUFFEROFFSET	Receive Buffer Offset Register
01C8 0114	RXFILTERLOWTHRESH	Receive Filter Low Priority Frame Threshold Register

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Table 5-80. Ethernet MAC (EMAC) Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01C8 0118 - 01C8 011C	–	Reserved
01C8 0120	RX0FLOWTHRESH	Receive Channel 0 Flow Control Threshold Register
01C8 0124	RX1FLOWTHRESH	Receive Channel 1 Flow Control Threshold Register
01C8 0128	RX2FLOWTHRESH	Receive Channel 2 Flow Control Threshold Register
01C8 012C	RX3FLOWTHRESH	Receive Channel 3 Flow Control Threshold Register
01C8 0130	RX4FLOWTHRESH	Receive Channel 4 Flow Control Threshold Register
01C8 0134	RX5FLOWTHRESH	Receive Channel 5 Flow Control Threshold Register
01C8 0138	RX6FLOWTHRESH	Receive Channel 6 Flow Control Threshold Register
01C8 013C	RX7FLOWTHRESH	Receive Channel 7 Flow Control Threshold Register
01C8 0140	RX0FREEBUFFER	Receive Channel 0 Free Buffer Count Register
01C8 0144	RX1FREEBUFFER	Receive Channel 1 Free Buffer Count Register
01C8 0148	RX2FREEBUFFER	Receive Channel 2 Free Buffer Count Register
01C8 014C	RX3FREEBUFFER	Receive Channel 3 Free Buffer Count Register
01C8 0150	RX4FREEBUFFER	Receive Channel 4 Free Buffer Count Register
01C8 0154	RX5FREEBUFFER	Receive Channel 5 Free Buffer Count Register
01C8 0158	RX6FREEBUFFER	Receive Channel 6 Free Buffer Count Register
01C8 015C	RX7FREEBUFFER	Receive Channel 7 Free Buffer Count Register
01C8 0160	MACCONTROL	MAC Control Register
01C8 0164	MACSTATUS	MAC Status Register
01C8 0168	EMCONTROL	Emulation Control Register
01C8 016C	FIFOCONTROL	FIFO Control Register (Transmit and Receive)
01C8 0170	MACCONFIG	MAC Configuration Register
01C8 0174	SOFTRESET	Soft Reset Register
01C8 0178 - 01C8 01CC	–	Reserved
01C8 01D0	MACSRCADDRLO	MAC Source Address Low Bytes Register (Lower 32-bits)
01C8 01D4	MACSRCADDRHI	MAC Source Address High Bytes Register (Upper 16-bits)
01C8 01D8	MACHASH1	MAC Hash Address Register 1
01C8 01DC	MACHASH2	MAC Hash Address Register 2
01C8 01E0	BOFFTEST	Back Off Test Register
01C8 01E4	TPACETEST	Transmit Pacing Algorithm Test Register
01C8 01E8	RXPAUSE	Receive Pause Timer Register
01C8 01EC	TXPAUSE	Transmit Pause Timer Register
01C8 01F0 - 01C8 01FC	–	Reserved
01C8 0200 - 01C8 02FC	(see Table 5-81)	EMAC Statistics Registers
01C8 0300 - 01C8 04FC	–	Reserved
01C8 0500	MACADDRLO	MAC Address Low Bytes Register
01C8 0504	MACADDRHI	MAC Address High Bytes Register
01C8 0508	MACINDEX	MAC Index Register
01C8 050C - 01C8 05FC	–	Reserved
01C8 0600	TX0HDP	Transmit Channel 0 DMA Head Descriptor Pointer Register
01C8 0604	TX1HDP	Transmit Channel 1 DMA Head Descriptor Pointer Register
01C8 0608	TX2HDP	Transmit Channel 2 DMA Head Descriptor Pointer Register
01C8 060C	TX3HDP	Transmit Channel 3 DMA Head Descriptor Pointer Register
01C8 0610	TX4HDP	Transmit Channel 4 DMA Head Descriptor Pointer Register
01C8 0614	TX5HDP	Transmit Channel 5 DMA Head Descriptor Pointer Register
01C8 0618	TX6HDP	Transmit Channel 6 DMA Head Descriptor Pointer Register
01C8 061C	TX7HDP	Transmit Channel 7 DMA Head Descriptor Pointer Register

Table 5-80. Ethernet MAC (EMAC) Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01C8 0620	RX0HDP	Receive Channel 0 DMA Head Descriptor Pointer Register
01C8 0624	RX1HDP	Receive Channel 1 DMA Head Descriptor Pointer Register
01C8 0628	RX2HDP	Receive Channel 2 DMA Head Descriptor Pointer Register
01C8 062C	RX3HDP	Receive Channel 3 DMA Head Descriptor Pointer Register
01C8 0630	RX4HDP	Receive Channel 4 DMA Head Descriptor Pointer Register
01C8 0634	RX5HDP	Receive Channel 5 DMA Head Descriptor Pointer Register
01C8 0638	RX6HDP	Receive Channel 6 DMA Head Descriptor Pointer Register
01C8 063C	RX7HDP	Receive Channel 7 DMA Head Descriptor Pointer Register
01C8 0640	TX0CP	Transmit Channel 0 Completion Pointer (Interrupt Acknowledge) Register
01C8 0644	TX1CP	Transmit Channel 1 Completion Pointer (Interrupt Acknowledge) Register
01C8 0648	TX2CP	Transmit Channel 2 Completion Pointer (Interrupt Acknowledge) Register
01C8 064C	TX3CP	Transmit Channel 3 Completion Pointer (Interrupt Acknowledge) Register
01C8 0650	TX4CP	Transmit Channel 4 Completion Pointer (Interrupt Acknowledge) Register
01C8 0654	TX5CP	Transmit Channel 5 Completion Pointer (Interrupt Acknowledge) Register
01C8 0658	TX6CP	Transmit Channel 6 Completion Pointer (Interrupt Acknowledge) Register
01C8 065C	TX7CP	Transmit Channel 7 Completion Pointer (Interrupt Acknowledge) Register
01C8 0660	RX0CP	Receive Channel 0 Completion Pointer (Interrupt Acknowledge) Register
01C8 0664	RX1CP	Receive Channel 1 Completion Pointer (Interrupt Acknowledge) Register
01C8 0668	RX2CP	Receive Channel 2 Completion Pointer (Interrupt Acknowledge) Register
01C8 066C	RX3CP	Receive Channel 3 Completion Pointer (Interrupt Acknowledge) Register
01C8 0670	RX4CP	Receive Channel 4 Completion Pointer (Interrupt Acknowledge) Register
01C8 0674	RX5CP	Receive Channel 5 Completion Pointer (Interrupt Acknowledge) Register
01C8 0678	RX6CP	Receive Channel 6 Completion Pointer (Interrupt Acknowledge) Register
01C8 067C	RX7CP	Receive Channel 7 Completion Pointer (Interrupt Acknowledge) Register
01C8 0680 - 02C8 0FFF	–	Reserved

Table 5-81. EMAC Statistics Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01C8 0200	RXGOODFRAMES	Good Receive Frames Register
01C8 0204	RXBCASTFRAMES	Broadcast Receive Frames Register (Total number of good broadcast frames received)
01C8 0208	RXMCASTFRAMES	Multicast Receive Frames Register (Total number of good multicast frames received)
01C8 020C	RXPAUSEFRAMES	Pause Receive Frames Register
01C8 0210	RXCRCERRORS	Receive CRC Errors Register (Total number of frames received with CRC errors)

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Table 5-81. EMAC Statistics Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01C8 0214	RXALIGNCODEERRORS	Receive Alignment/Code Errors Register (Total number of frames received with alignment/code errors)
01C8 0218	RXOVERSIZED	Receive Oversized Frames Register (Total number of oversized frames received)
01C8 021C	RXJABBER	Receive Jabber Frames Register (Total number of jabber frames received)
01C8 0220	RXUNDERSIZED	Receive Undersized Frames Register (Total number of undersized frames received)
01C8 0224	RXFRAGMENTS	Receive Frame Fragments Register
01C8 0228	RXFILTERED	Filtered Receive Frames Register
01C8 022C	RXQOSFILTERED	Received QOS Filtered Frames Register
01C8 0230	RXOCTETS	Receive Octet Frames Register (Total number of received bytes in good frames)
01C8 0234	TXGOODFRAMES	Good Transmit Frames Register (Total number of good frames transmitted)
01C8 0238	TXBCASTFRAMES	Broadcast Transmit Frames Register
01C8 023C	TXMCASTFRAMES	Multicast Transmit Frames Register
01C8 0240	TXPAUSEFRAMES	Pause Transmit Frames Register
01C8 0244	TXDEFERRED	Deferred Transmit Frames Register
01C8 0248	TXCOLLISION	Transmit Collision Frames Register
01C8 024C	TXSINGLECOLL	Transmit Single Collision Frames Register
01C8 0250	TXMULTICOLL	Transmit Multiple Collision Frames Register
01C8 0254	TXEXCESSIVECOLL	Transmit Excessive Collision Frames Register
01C8 0258	TXLATECOLL	Transmit Late Collision Frames Register
01C8 025C	TXUNDERRUN	Transmit Underrun Error Register
01C8 0260	TXCARRIERSENSE	Transmit Carrier Sense Errors Register
01C8 0264	TXOCTETS	Transmit Octet Frames Register
01C8 0268	FRAME64	Transmit and Receive 64 Octet Frames Register
01C8 026C	FRAME65T127	Transmit and Receive 65 to 127 Octet Frames Register
01C8 0270	FRAME128T255	Transmit and Receive 128 to 255 Octet Frames Register
01C8 0274	FRAME256T511	Transmit and Receive 256 to 511 Octet Frames Register
01C8 0278	FRAME512T1023	Transmit and Receive 512 to 1023 Octet Frames Register
01C8 027C	FRAME1024TUP	Transmit and Receive 1024 to 1518 Octet Frames Register
01C8 0280	NETOCTETS	Network Octet Frames Register
01C8 0284	RXSOFOVERRUNS	Receive FIFO or DMA Start of Frame Overruns Register
01C8 0288	RXMOFOVERRUNS	Receive FIFO or DMA Middle of Frame Overruns Register
01C8 028C	RXDMAOVERRUNS	Receive DMA Start of Frame and Middle of Frame Overruns Register
01C8 0290 - 01C8 02FC	–	Reserved

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Table 5-82. EMAC Control Module Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C8 1000	–	Reserved
0x01C8 1004	EWCTL	Interrupt control register
0x01C8 1008	EWINTTCNT	Interrupt timer count
0x01C8 100C - 0x01C8 17FF	–	Reserved

Table 5-83. EMAC Control Module RAM

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C8 2000 - 0x01C8 3FFF		EMAC Control Module Descriptor Memory

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5.19.2 EMAC Electrical Data/Timing

Table 5-84. Timing Requirements for MRCLK (see Figure 5-60)

NO.			-594		UNIT
			MIN	MAX	
1	$t_{c(MRCLK)}$	Cycle time, MRCLK	40		ns
2	$t_{w(MRCLKH)}$	Pulse duration, MRCLK high	14		ns
3	$t_{w(MRCLKL)}$	Pulse duration, MRCLK low	14		ns

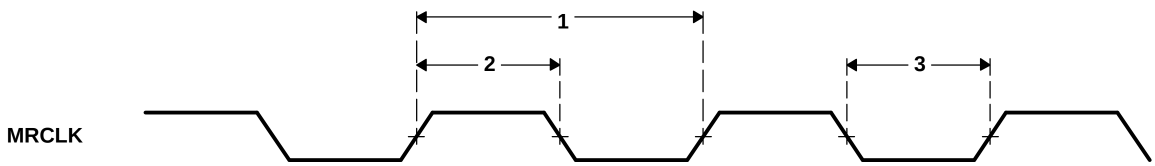

Figure 5-60. MRCLK Timing (EMAC - Receive)

Table 5-85. Timing Requirements for MTCLK (see Figure 5-60)

NO.			-594		UNIT
			MIN	MAX	
1	$t_{c(MTCLK)}$	Cycle time, MTCLK	40		ns
2	$t_{w(MTCLKH)}$	Pulse duration, MTCLK high	14		ns
3	$t_{w(MTCLKL)}$	Pulse duration, MTCLK low	14		ns

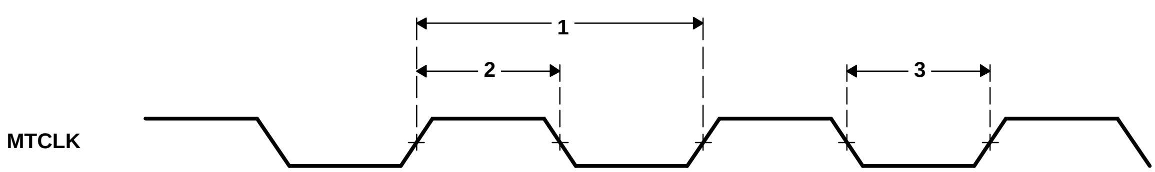

Figure 5-61. MTCLK Timing (EMAC - Transmit)

Table 5-86. Timing Requirements for EMAC MII Receive 10/100 Mbit/s(1) (see Figure 5-62)

NO.			-594		UNIT
			MIN	MAX	
1	$t_{su(MRXD-MRCLKH)}$	Setup time, receive selected signals valid before MRCLK high	8		ns
2	$t_{h(MRCLKH-MRXD)}$	Hold time, receive selected signals valid after MRCLK high	8		ns

(1) Receive selected signals include: MRXD3-MRXD0, MRXDV, and MRXER.

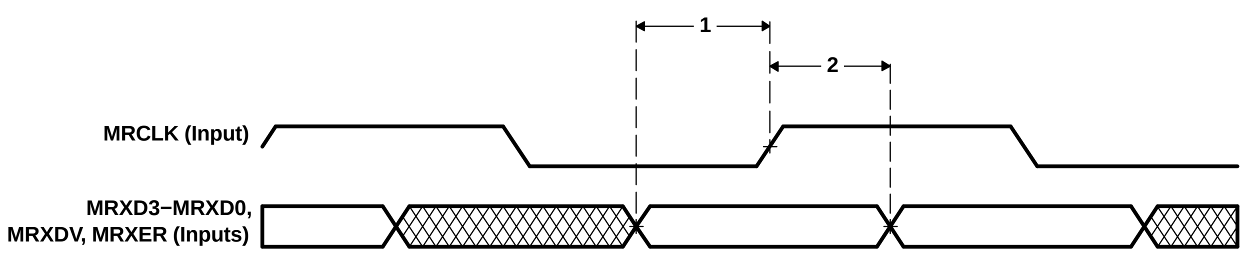

Figure 5-62. EMAC Receive Interface Timing

Table 5-87. Switching Characteristics Over Recommended Operating Conditions for EMAC MII Transmit 10/100 Mbit/s(1) (see Figure 5-63)

NO.			-594		UNIT
			MIN	MAX	
1	$t_{d(MTCLKH-MTXD)}$	Delay time, MTCLK high to transmit selected signals valid	5	25	ns

(1) Transmit selected signals include: MTXD3-MTXD0, and MTXEN.

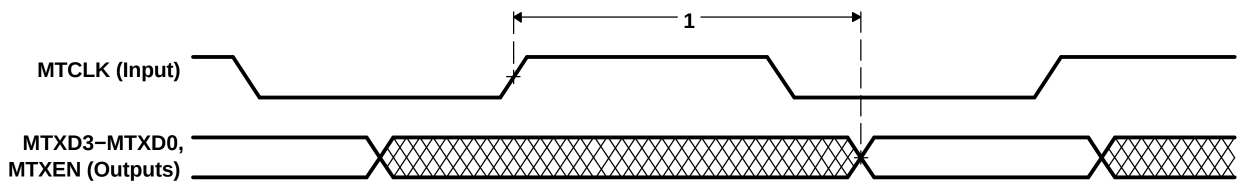

Figure 5-63. EMAC Transmit Interface Timing

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5.20 Management Data Input/Output (MDIO)

The Management Data Input/Output (MDIO) module continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system.

The Management Data Input/Output (MDIO) module implements the 802.3 serial management interface to interrogate and control Ethernet PHY(s) using a shared two-wire bus. Host software uses the MDIO module to configure the auto-negotiation parameters of each PHY attached to the EMAC, retrieve the negotiation results, and configure required parameters in the EMAC module for correct operation. The module is designed to allow almost transparent operation of the MDIO interface, with very little maintenance from the core processor. Only one PHY may be connected at any given time.

For more detailed information on the MDIO peripheral, see the *Documentation Support* section for the Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module Reference Guide. For a list of supported registers and register fields, see Table 5-88 [MDIO Registers] in this data manual.

5.20.1 Peripheral Register Description(s)

Table 5-88. MDIO Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C8 4000	–	Reserved
0x01C8 4004	CONTROL	MDIO Control Register
0x01C8 4008	ALIVE	MDIO PHY Alive Status Register
0x01C8 400C	LINK	MDIO PHY Link Status Register
0x01C8 4010	LINKINTRAW	MDIO Link Status Change Interrupt (Unmasked) Register
0x01C8 4014	LINKINTMASKED	MDIO Link Status Change Interrupt (Masked) Register
0x01C8 4018	–	Reserved
0x01C8 4020	USERINTRAW	MDIO User Command Complete Interrupt (Unmasked) Register
0x01C8 4024	USERINTMASKED	MDIO User Command Complete Interrupt (Masked) Register
0x01C8 4028	USERINTMASKSET	MDIO User Command Complete Interrupt Mask Set Register
0x01C8 402C	USERINTMASKCLEAR	MDIO User Command Complete Interrupt Mask Clear Register
0x01C8 4030 - 0x01C8 407C	–	Reserved
0x01C8 4080	USERACCESS0	MDIO User Access Register 0
0x01C8 4084	USERPHYSEL0	MDIO User PHY Select Register 0
0x01C8 4088	USERACCESS1	MDIO User Access Register 1
0x01C8 408C	USERPHYSEL1	MDIO User PHY Select Register 1
0x01C8 4090 - 0x01C8 47FF	–	Reserved

5.20.2 Management Data Input/Output (MDIO) Electrical Data/Timing

Table 5-89. Timing Requirements for MDIO Input (see Figure 5-64 and Figure 5-65)

NO.			-594		UNIT
			MIN	MAX	
1	$t_{c(MDCLK)}$	Cycle time, MDCLK	400		ns
2	$t_{w(MDCLK)}$	Pulse duration, MDCLK high/low	180		ns
3	$t_{t(MDCLK)}$	Transition time, MDCLK		5	ns
4	$t_{su(MDIO-MDCLKH)}$	Setup time, MDIO data input valid before MDCLK high	15		ns
5	$t_{h(MDCLKH-MDIO)}$	Hold time, MDIO data input valid after MDCLK high	0		ns

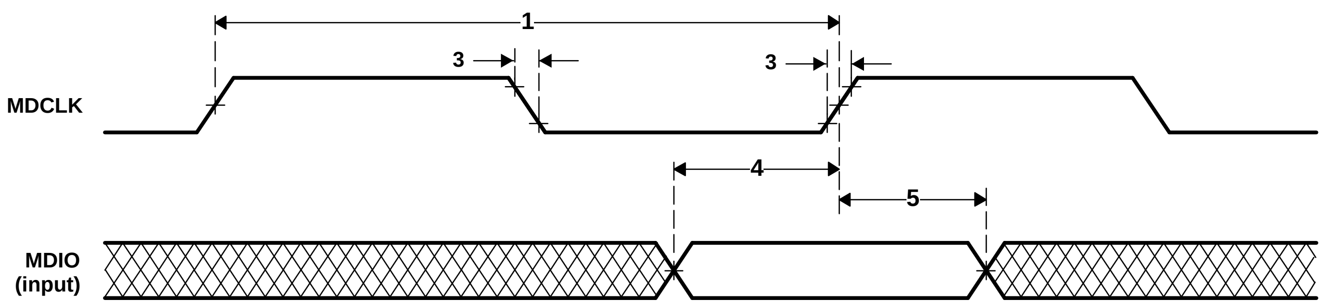

Figure 5-64. MDIO Input Timing

Table 5-90. Switching Characteristics Over Recommended Operating Conditions for MDIO Output (see Figure 5-65)

NO.			-594		UNIT
			MIN	MAX	
7	$t_{d(MDCLKL-MDIO)}$	Delay time, MDCLK low to MDIO data output valid	10	100	ns

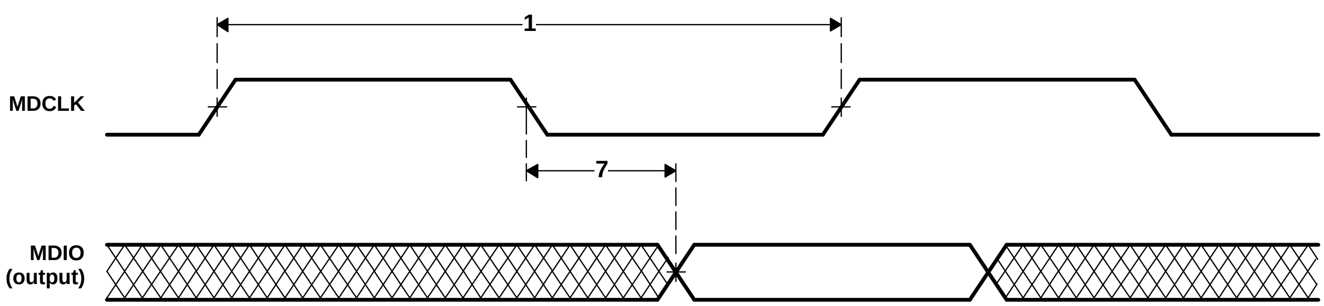

Figure 5-65. MDIO Output Timing

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5.21 Timer

The DM6446 device has 3 64-bit general-purpose timers which have the following features:

- 64-bit count-up counter
- Timer modes:
  – 64-bit general-purpose timer mode
  – Dual 32-bit general-purpose timer mode (Timer 0 and 1)
  – Watchdog timer mode (Timer 2)
- 2 possible clock sources:
  – Internal clock
  – External clock input via timer input pin TIM_IN (Timer 0 only)
- 2 operation modes:
  – One-time operation (timer runs for one period then stops)
  – Continuous operation (timer automatically resets after each period)
- Generates interrupts to both the DSP and the ARM CPUs
- Generates sync event to EDMA

For more detailed information, see the *Documentation Support* section for the Timer Reference Guide.

5.21.1 Timer Peripheral Register Description(s)

Table 5-91. Timer 0 Registers

HEX ADDRESS RANGE	ACRONYM	DESCRIPTION
0x01C2 1400	-	Reserved
0x01C2 1404	EMUMGT_CLKSPD	Timer 0 Emulation Management/Clock Speed Register
0x01C2 1410	TIM12	Timer 0 Counter Register 12
0x01C2 1414	TIM34	Timer 0 Counter Register 34
0x01C2 1418	PRD12	Timer 0 Period Register 12
0x01C2 141C	PRD34	Timer 0 Period Register 34
0x01C2 1420	TCR	Timer 0 Control Register
0x01C2 1424	TGCR	Timer 0 Global Control Register
0x01C2 1428 - 0x01C2 17FF	-	Reserved

Table 5-92. Timer 1 Registers

HEX ADDRESS RANGE	ACRONYM	DESCRIPTION
0x01C2 1800	-	Reserved
0x01C2 1804	EMUMGT_CLKSPD	Timer 1 Emulation Management/Clock Speed Register
0x01C2 1810	TIM12	Timer 1 Counter Register 12
0x01C2 1814	TIM34	Timer 1 Counter Register 34
0x01C2 1818	PRD12	Timer 1 Period Register 12
0x01C2 181C	PRD34	Timer 1 Period Register 34
0x01C2 1820	TCR	Timer 1 Control Register
0x01C2 1824	TGCR	Timer 1 Global Control Register
0x01C2 1828 - 0x01C2 1BFF	-	Reserved

Table 5-93. Timer 2 (Watchdog) Registers

HEX ADDRESS RANGE	ACRONYM	DESCRIPTION
0x01C2 1C00	-	Reserved

Table 5-93. Timer 2 (Watchdog) Registers (continued)

HEX ADDRESS RANGE	ACRONYM	DESCRIPTION
0x01C2 1C04	EMUMGT_CLKSPD	Timer 2 Emulation Management/Clock Speed Register
0x01C2 1C10	TIM12	Timer 2 Counter Register 12
0x01C2 1C14	TIM34	Timer 2 Counter Register 34
0x01C2 1C18	PRD12	Timer 2 Period Register 12
0x01C2 1C1C	PRD34	Timer 2 Period Register 34
0x01C2 1C20	TCR	Timer 2 Control Register
0x01C2 1C24	TGCR	Timer 2 Global Control Register
0x01C2 1C28	WDTCR	Timer 2 Watchdog Timer Control Register
0x01C2 1C2C - 0x01C2 1FFF	-	Reserved

5.21.2 Timer Electrical Data/Timing

Table 5-94. Timing Requirements for Timer Input(1)(2) (see Figure 5-66)

NO.			-594		UNIT
			MIN	MAX	
1	$t_{c(TIN)}$	Cycle time, TIM_IN	4P		ns
2	$t_{w(TINPH)}$	Pulse duration, TIM_IN high	0.45C	0.55C	ns
3	$t_{w(TINPL)}$	Pulse duration, TIM_IN low	0.45C	0.55C	ns
4	$t_{t(TIN)}$	Transition time, TIM_IN		0.05C	ns

(1) P = MXI/CLKIN cycle time in ns. For example, when MXI/CLKIN frequency is 27 MHz, use P = $37.0\overline{37}$ ns.
(2) C = TIM_IN cycle time in ns. For example, when TIM_IN frequency is 27 MHz, use C = $37.0\overline{37}$ ns

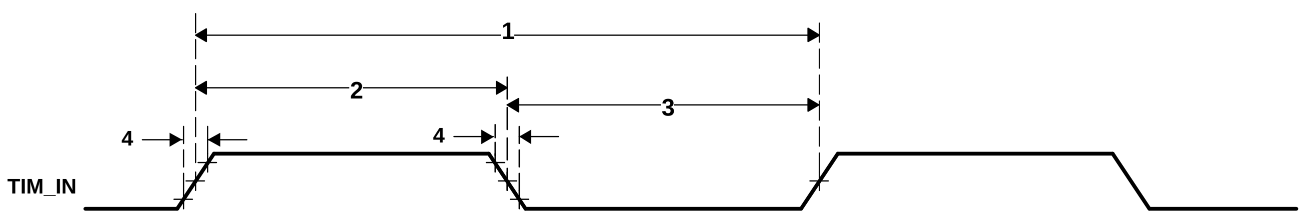

Figure 5-66. Timer Timing

5.22 Pulse Width Modulator (PWM)

The 3 DM6446 Pulse Width Modulator (PWM) peripherals support the following features:

- Period counter
- First-phase duration counter
- Repeat count for one-shot operation
- Configurable to operate in either one-shot or continuous mode
- Buffered period and first-phase duration registers
- One-shot operation triggerable by hardware events with programmable edge transitions. (low-to-high or high-to-low).
- One-shot operation generates N+1 periods of waveform, N being the repeat count register value
- Emulation support

The register memory maps for PWM0/1/2 are shown in Table 5-95, Table 5-96, and Table 5-97.

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Table 5-95. PWM0 Register Memory Map

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C2 2000		Reserved
0x01C2 2004	PCR	PWM0 Peripheral Control Register
0x01C2 2008	CFG	PWM0 Configuration Register
0x01C2 200C	START	PWM0 Start Register
0x01C2 2010	RPT	PWM0 Repeat Count Register
0x01C2 2014	PER	PWM0 Period Register
0x01C2 2018	PH1D	PWM0 First-Phase Duration Register
0x01C2 201C - 0x01C2 23FF	-	Reserved

Table 5-96. PWM1 Register Memory Map

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C2 2400		Reserved
0x01C2 2404	PCR	PWM1 Peripheral Control Register
0x01C2 2408	CFG	PWM1 Configuration Register
0x01C2 240C	START	PWM1 Start Register
0x01C2 2410	RPT	PWM1 Repeat Count Register
0x01C2 2414	PER	PWM1 Period Register
0x01C2 2418	PH1D	PWM1 First-Phase Duration Register
0x01C2 241C -0x01C2 27FF	-	Reserved

Table 5-97. PWM2 Register Memory Map

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01C2 2800		Reserved
0x01C2 2804	PCR	PWM2 Peripheral Control Register
0x01C2 2808	CFG	PWM2 Configuration Register
0x01C2 280C	START	PWM2 Start Register
0x01C2 2810	RPT	PWM2 Repeat Count Register
0x01C2 2814	PER	PWM2 Period Register
0x01C2 2818	PH1D	PWM2 First-Phase Duration Register
0x01C2 281C - 0x01C2 2BFF	-	Reserved

5.22.1 *PWM0/1/2 Electrical/Timing Data*

Table 5-98. Switching Characteristics Over Recommended Operating Conditions for PWM0/1/2 Outputs (see Figure 5-67 and Figure 5-68)

NO.	PARAMETER		-594		UNIT
			MIN	MAX	
1	$t_{w(PWMH)}$	Pulse duration, PWMx high	37		ns
2	$t_{w(PWML)}$	Pulse duration, PWMx low	37		ns
3	$t_{t(PWM)}$	Transition time, PWMx		5	ns
4	$t_{d(CCDC-PWMV)}$	Delay time, CCDC(VD) trigger event to PWMx valid	2	10	ns

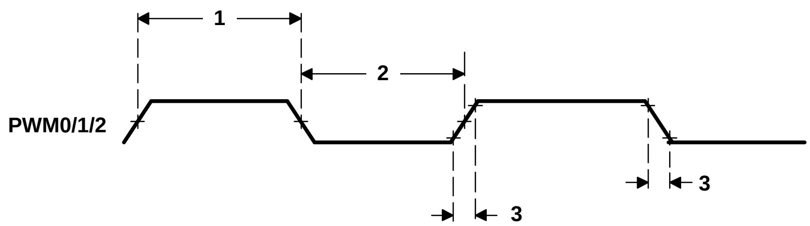

Figure 5-67. PWM Output Timing

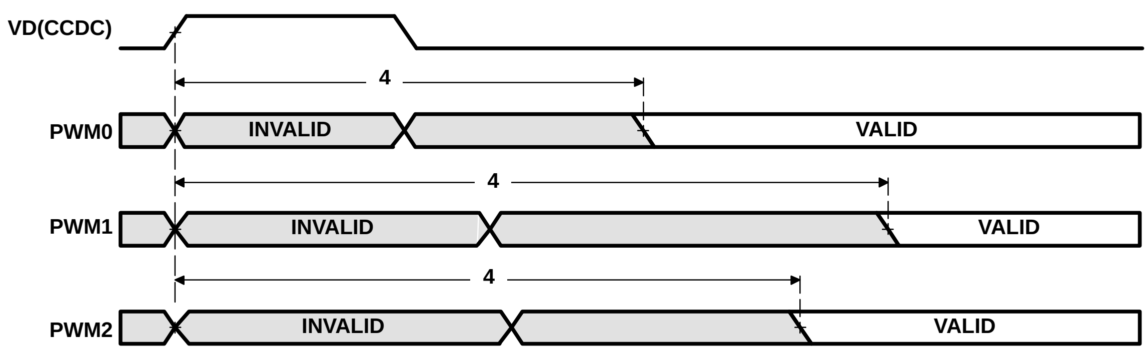

Figure 5-68. PWM Output Delay Timing

5.23 VLYNQ

The DM6446 VLYNQ peripheral provides a high speed serial communications interface with the following features.

- Low Pin Count
- Scalable Performance / Support
- Simple Packet Based Transfer Protocol for Memory Mapped Access
  - Write Request / Data Packet
  - Read Request Packet
  - Read Response Data Packet
  - Interrupt Request Packet
- Supports both Symmetric and Asymmetric Operation
  - Tx pins on first device connect to Rx pins on second device and vice versa
  - Data pin widths are automatically detected after reset
  - Request packets, response packets, and flow control information are all multiplexed and sent across the same physical pins
  - Supports both Host/Peripheral and Peer to Peer communication
- Simple Block Code Packet Formatting (8b/10b)
- In Band Flow Control
  - No extra pins needed
  - Allows receiver to momentarily throttle back transmitter when overflow is about to occur
  - Uses built in special code capability of block code to seamlessly interleave flow control information with user data
  - Allows system designer to balance cost of data buffering versus performance
- Multiple outstanding transactions
- Automatic packet formatting optimizations
- Internal loop-back mode

5.23.1 VLYNQ Peripheral Register Description(s)

Table 5-99. VLYNQ Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x0C00 0000	-	Reserved
0x0C00 0004	CTRL	VLYNQ Local Control Register
0x0C00 0008	STAT	VLYNQ Local Status Register
0x0C00 000C	INTPRI	VLYNQ Local Interrupt Priority Vector Status/Clear Register
0x0C00 0010	INTSTATCLR	VLYNQ Local Unmasked Interrupt Status/Clear Register
0x0C00 0014	INTPENDSET	VLYNQ Local Interrupt Pending/Set Register
0x0C00 0018	INTPTR	VLYNQ Local Interrupt Pointer Register
0x0C00 001C	XAM	VLYNQ Local Transmit Address Map Register
0x0C00 0020	RAMS1	VLYNQ Local Receive Address Map Size 1 Register
0x0C00 0024	RAMO1	VLYNQ Local Receive Address Map Offset 1 Register
0x0C00 0028	RAMS2	VLYNQ Local Receive Address Map Size 2 Register
0x0C00 002C	RAMO2	VLYNQ Local Receive Address Map Offset 2 Register
0x0C00 0030	RAMS3	VLYNQ Local Receive Address Map Size 3 Register
0x0C00 0034	RAMO3	VLYNQ Local Receive Address Map Offset 3 Register
0x0C00 0038	RAMS4	VLYNQ Local Receive Address Map Size 4 Register
0x0C00 003C	RAMO4	VLYNQ Local Receive Address Map Offset 4 Register
0x0C00 0040	CHIPVER	VLYNQ Local Chip Version Register
0x0C00 0044	AUTNGO	VLYNQ Local Auto Negotiation Register
0x0C00 0048	-	Reserved
0x0C00 004C	-	Reserved
0x0C00 0050 - 0x0C00 005C	-	Reserved
0x0C00 0060	-	Reserved
0x0C00 0064	-	Reserved
0x0C00 0068 - 0x0C00 007C	-	Reserved *for future use*
0x0C00 0080	RREVID	VLYNQ Remote Revision Register
0x0C00 0084	RCTRL	VLYNQ Remote Control Register
0x0C00 0088	RSTAT	VLYNQ Remote Status Register
0x0C00 008C	RINTPRI	VLYNQ Remote Interrupt Priority Vector Status/Clear Register
0x0C00 0090	RINTSTATCLR	VLYNQ Remote Unmasked Interrupt Status/Clear Register
0x0C00 0094	RINTPENDSET	VLYNQ Remote Interrupt Pending/Set Register
0x0C00 0098	RINTPTR	VLYNQ Remote Interrupt Pointer Register
0x0C00 009C	RXAM	VLYNQ Remote Transmit Address Map Register
0x0C00 00A0	RRAMS1	VLYNQ Remote Receive Address Map Size 1 Register
0x0C00 00A4	RRAMO1	VLYNQ Remote Receive Address Map Offset 1 Register
0x0C00 00A8	RRAMS2	VLYNQ Remote Receive Address Map Size 2 Register
0x0C00 00AC	RRAMO2	VLYNQ Remote Receive Address Map Offset 2 Register
0x0C00 00B0	RRAMS3	VLYNQ Remote Receive Address Map Size 3 Register
0x0C00 00B4	RRAMO3	VLYNQ Remote Receive Address Map Offset 3 Register
0x0C00 00B8	RRAMS4	VLYNQ Remote Receive Address Map Size 4 Register
0x0C00 00BC	RRAMO4	VLYNQ Remote Receive Address Map Offset 4 Register
0x0C00 00C0	RCHIPVER	VLYNQ Remote Chip Version Register (values on the device_id and device_rev pins of remote VLYNQ)
0x0C00 00C4	RAUTNGO	VLYNQ Remote Auto Negotiation Register
0x0C00 00C8	RMANNGO	VLYNQ Remote Manual Negotiation Register
0x0C00 00CC	RNGOSTAT	VLYNQ Remote Negotiation Status Register

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Table 5-99. VLYNQ Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x0C00 00D0 - 0x0C00 00DC	-	Reserved
0x0C00 00E0	RINTVEC0	VLYNQ Remote Interrupt Vectors 3 - 0 (sourced from vlynq_int_i[3:0] port of remote VLYNQ)
0x0C00 00E4	RINTVEC1	VLYNQ Remote Interrupt Vectors 7 - 4 (sourced from vlynq_int_i[7:4] port of remote VLYNQ)
0x0C00 00E8 - 0x0C00 00FC	-	Reserved *for future use*
0x0C00 0100 - 0x0FFF FFFF	-	Reserved

5.23.2 VLYNQ Electrical Data/Timing

Table 5-100. Timing Requirements for VLYNQ_CLK for VLYNQ (see Figure 5-69)

NO.			-594		UNIT
			MIN	MAX	
1	$t_{c(VCLK)}$	Cycle time, VLYNQ_CLK	10		ns
2	$t_{w(VCLKH)}$	Pulse duration, VLYNQ_CLK high **[CLK External]**	3		ns
		Pulse duration, VLYNQ_CLK high **[CLK Internal]**	4		ns
3	$t_{w(VCLKL)}$	Pulse duration, VLYNQ_CLK low **[CLK External]**	3		ns
		Pulse duration, VLYNQ_CLK low **[CLK Internal]**	4		ns
4	$t_{t(VCLK)}$	Transition time, VLYNQ_CLK		TBD	ns

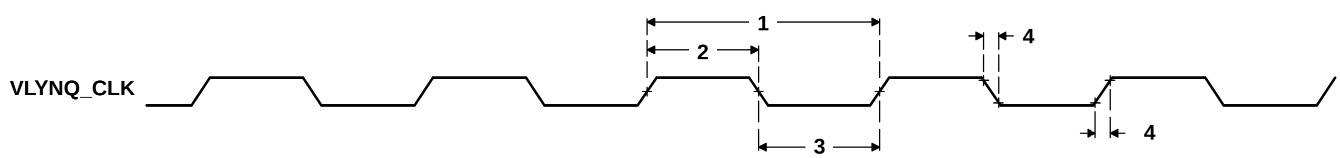

Figure 5-69. VLYNQ_CLK Timing for VLYNQ

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Table 5-101. Switching Characteristics Over Recommended Operating Conditions for Transmit Data for the VLYNQ Module (see Figure 5-70)

NO.	PARAMETER		-594 MIN	-594 MAX	UNIT
1	$t_{d(VCLKH-TXDI)}$	Delay time, VLYNQ_CLK high to VLYNQ_TXD[3:0] invalid [**SLOW** Mode]	1		ns
		Delay time, VLYNQ_CLK high to VLYNQ_ TXD[3:0] invalid [**FAST** Mode]	0.5		ns
2	$t_{d(VCLKH-TXDV)}$	Delay time, VLYNQ_CLK to VLYNQ_TXD[3:0] valid		9.75	ns

Table 5-102. Timing Requirements for Receive Data for the VLYNQ Module (see Figure 5-70)

NO.				-594 MIN	-594 MAX	UNIT
3	$t_{su(RXDV-VCLKH)}$	Setup time, VLYNQ_RXD[3:0] valid before VLYNQ_CLK high	RTM disabled, RTM sample = 3	0.2		ns
			RTM enabled, RXD Flop = 0	1.3		ns
			RTM enabled, RXD Flop = 1	0.8		ns
			RTM enabled, RXD Flop = 2	0.4		ns
			RTM enabled, RXD Flop = 3	0.2		ns
			RTM enabled, RXD Flop = 4	0		ns
			RTM enabled, RXD Flop = 5	-0.3		ns
			RTM enabled, RXD Flop = 6	-0.5		ns
			RTM enabled, RXD Flop = 7	-0.7		ns
4	$t_{h(VCLKH-RXDV)}$	Hold time, VLYNQ_RXD[3:0] valid after VLYNQ_CLK high	RTM disabled, RTM sample = 3	2		ns
			RTM enabled, RXD Flop = 0	0.5		ns
			RTM enabled, RXD Flop = 1	1.0		ns
			RTM enabled, RXD Flop = 2	1.5		ns
			RTM enabled, RXD Flop = 3	2.0		ns
			RTM enabled, RXD Flop = 4	2.5		ns
			RTM enabled, RXD Flop = 5	3.0		ns
			RTM enabled, RXD Flop = 6	3.5		ns
			RTM enabled, RXD Flop = 7	4.0		ns

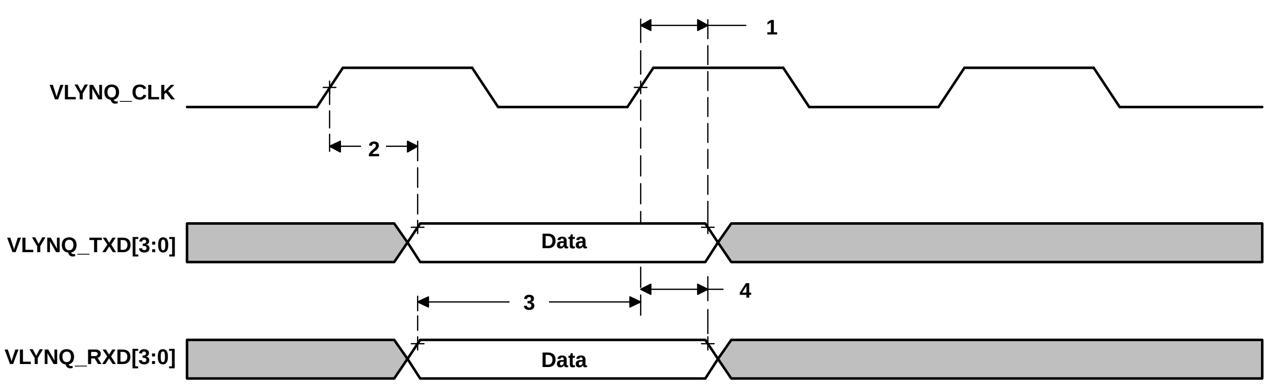

Figure 5-70. VLYNQ Transmit/Receive Timing

5.24 IEEE 1149.1 JTAG

The JTAG(1) interface is used for BSDL testing and emulation of the DM6446 device.

The DM6446 device requires that both TRST and RESET be asserted upon power up to be properly initialized. While RESET initializes the device, TRST initializes the device's emulation logic. Both resets are required for proper operation.

While both TRST and RESET need to be asserted upon power up, only RESET needs to be released for the device to boot properly. TRST may be asserted indefinitely for normal operation, keeping the JTAG port interface and device's emulation logic in the reset state.

TRST only needs to be released when it is necessary to use a JTAG controller to debug the device or exercise the device's boundary scan functionality. Note: TRST is synchronous and ***must*** be clocked by TCK; otherwise, the boundary scan logic may not respond as expected after TRST is asserted.

RESET must be released only in order for boundary-scan JTAG to read the variant field of IDCODE correctly. Other boundary-scan instructions work correctly independent of current state of RESET.

For maximum reliability, DM6446 includes an internal pulldown (IPD) on the TRST pin to ensure that TRST will always be asserted upon power up and the device's internal emulation logic will always be properly initialized.

JTAG controllers from Texas Instruments actively drive TRST high. However, some third-party JTAG controllers may not drive TRST high but expect the use of a pullup resistor on TRST.

When using this type of JTAG controller, assert TRST to intialize the device after powerup and externally drive TRST high before attempting any emulation or boundary scan operations. Following the release of RESET, the low-to-high transition of TRST must be "seen" to latch the state of EMU1 and EMU0. The EMU[1:0] pins configure the device for either Boundary Scan mode or Emulation mode. For more detailed information, see the terminal functions section of this data sheet.

(1) IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

5.24.1 JTAG ID Register Description

The JTAG ID register is a read-only register that identifies to the customer the JTAG/Device ID. For the DM6446 device, the JTAG ID register resides at address location 0x01C4 0028. The register hex value for DM6446 is: 0x0B70 002F. For the actual register bit names and their associated bit field descriptions, see Figure 5-71 and Table 5-103.

31-28	27-12	11-1	0
VARIANT (4-Bit)	PART NUMBER (16-Bit)	MANUFACTURER (11-Bit)	LSB
R-0000	R-1011 0111 0000 0000	R-0000 0010 111	R-1

LEGEND: R = Read, W = Write, n = value at reset

Figure 5-71. JTAG ID Register Description - DM6446 Register Value - 0xXB70 001F

Table 5-103. JTAG ID Register Selection Bit Descriptions

BIT	NAME	DESCRIPTION
31:28	VARIANT	Variant (4-Bit) value. DM6446 value: 0000.
27:12	PART NUMBER	Part Number (16-Bit) value. DM6446 value: 1011 0111 0000 0000.
11-1	MANUFACTURER	Manufacturer (11-Bit) value. DM6446 value: 0000 0010 111.
0	LSB	LSB. This bit is read as a "1" for DM6446.

5.24.2 JTAG Peripheral Register Description(s)

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Table 5-104. JTAG ID Register

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0x01C4 0028	JTAGID	JTAG Identification Register	Read-only. Provides 32-bit JTAG ID of the device.

5.24.3 JTAG Test-Port Electrical Data/Timing

Table 5-105. Timing Requirements for JTAG Test Port (see Figure 5-72)

NO.			-594		UNIT
			MIN	MAX	
1	$t_{c(TCK)}$	Cycle time, TCK	35		ns
3	$t_{su(TDIV-TCKH)}$	Setup time, TDI/TMS/$\overline{TRST}$ valid before TCK high	10		ns
4	$t_{h(TCKH-TDIV)}$	Hold time, TDI/TMS/$\overline{TRST}$ valid after TCK high	9		ns

Table 5-106. Switching Characteristics Over Recommended Operating Conditions for JTAG Test Port (see Figure 5-72)

NO.	PARAMETER		-594		UNIT
			MIN	MAX	
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0	18	ns

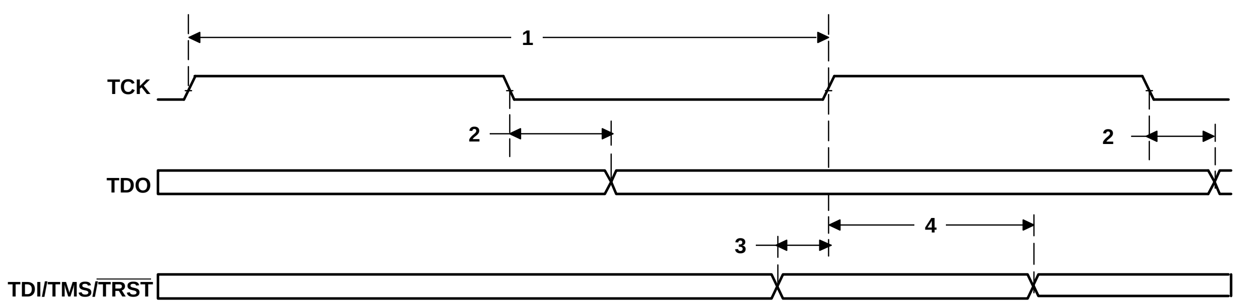

Figure 5-72. JTAG Test-Port Timing

6 Mechanical Packaging and Orderable Information

The following table(s) show the thermal resistance characteristics for the PBGA–ZWT mechanical package.

6.1 Thermal Data for ZWT

Table 6-1. Thermal Resistance Characteristics (PBGA Package) [ZWT]

NO.			°C/W	AIR FLOW (m/s)(1)
1	$R\Theta_{JC}$	Junction-to-case	6.54	N/A
2	$R\Theta_{JB}$	Junction-to-board	15.62	N/A
3	$R\Theta_{JA}$	Junction-to-free air	48.75	0.00
4			41.70	1.0
5			39.83	2.00
6			38.63	3.00
7	Psi_{JT}	Junction-to-package top	0.18	0.00
8			0.23	1.0
9			0.23	2.00
10			0.24	3.00
11	Psi_{JB}	Junction-to-board	15.06	0.00
12			15.06	1.0
13			15.05	2.00
14			15.04	3.00

(1) m/s = meters per second

6.1.1 Packaging Information

The following packaging information and addendum reflect the most current data available for the designated device(s). This data is subject to change without notice and without revision of this document.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TMX320DM6446ZWT	ACTIVE	BGA	ZWT	361	90	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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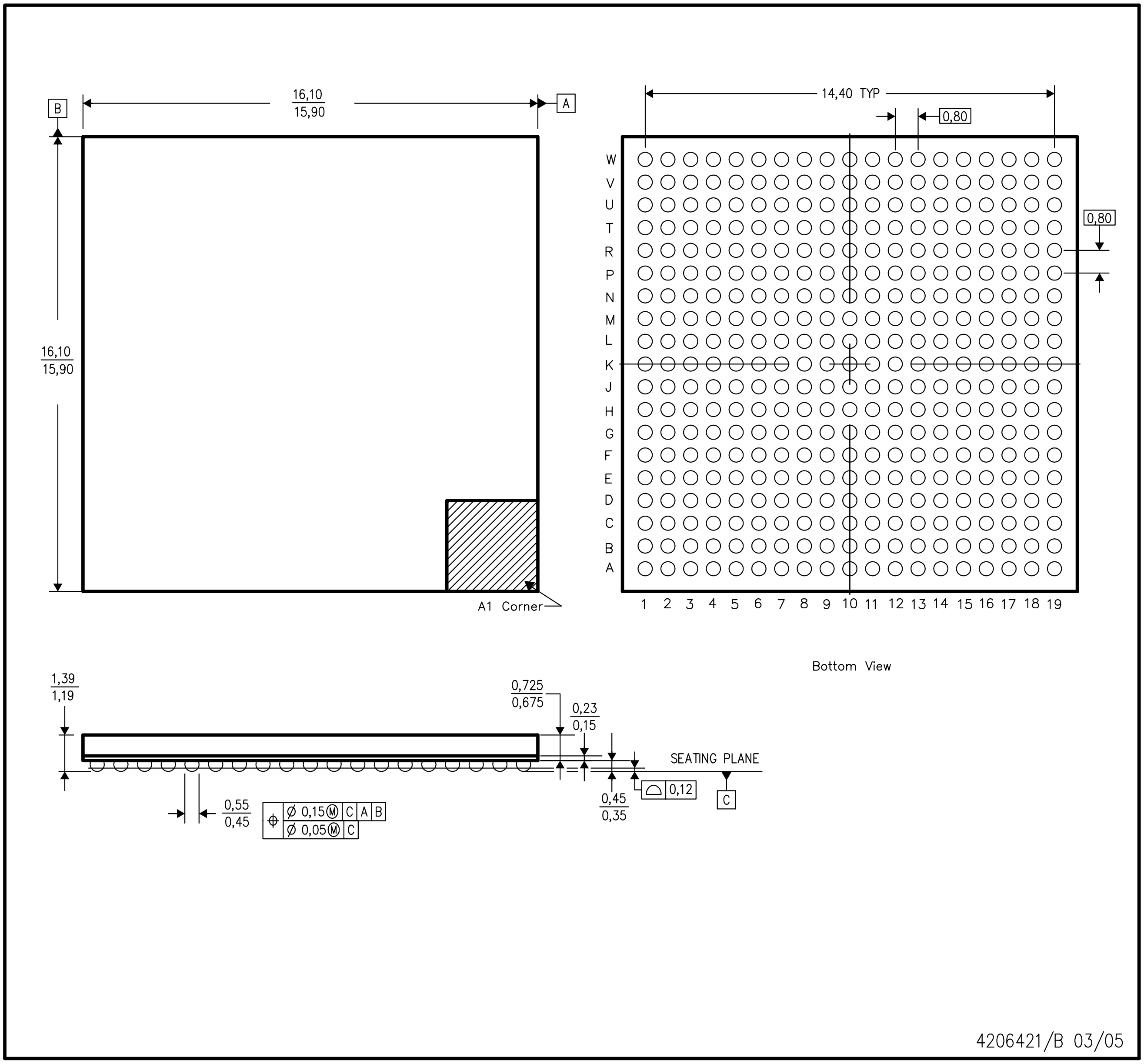
ZWT (S–PBGA–N361) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead–free.