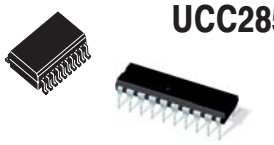


SLUS517B − DECEMBER 2002 − REVISED AUGUST 2004

ADVANCED PFC/PWM COMBINATION CONTROLLERS

FEATURES

- **Provides Control of PFC and PWM Power Stages In One Device**
- **Leading-Edge PFC, Trailing-Edge PWM Modulation for Reduced Ripple**
- **Built-In Sequencing of PFC and PWM Turn-On**
- **2-A Source and 3-A Sink Gate Drive for Both PFC and PWM Stages**
- **Typical 16-ns Rise Time and 7-ns Fall Time into 1-nF Loads**

PFC Features

- **Average-Current-Mode Control for Continuous Conduction Mode Operation**
- **Highly-Linear Multiplier for Near-Unity Power Factor**
- **Input Voltage Feedforward Implementation**
- **Improved Load Transient Response**
- **Accurate Power Limiting**
- **Zero Power Detect**

PWM Features

- **Peak-Current-Mode Control Operation**
- **1:1 or 1:2 PFC:PWM Frequency Options**
- **Programmable maximum duty cycle**
- **Programmable Soft-Start**
- **Two Hysteresis Options for Differing Hold-Up Time Requirements**

DESCRIPTION

The UCC28510 series of combination PFC/PWM controllers provide complete control functionality for any off-line power system requiring compliance with the IEC1000−3−2 harmonic reduction requirements. By combining the control and drive signals for the PFC and the PWM stages into a single device, significant performance and cost benefits are gained. By managing the modulation mechanisms of the two stages (leading-edge modulation for PFC and trailing-edge modulation for PWM), the ripple current in the boost capacitor is minimized.

Based on the average current mode control architecture with input voltage feedforward of prior PFC/PWM combination controllers, these devices offer performance advantages. Two new key PWM features are programmable maximum duty cycle and the 2x PWM frequency options to the base PFC frequency. For the PFC stage, the devices feature an improved multiplier and the use of a transconductance amplifier for enhanced transient response.

The core of the PFC section is in a three-input multiplier that generates the reference signal for the line current. The UCC28510 series features a highly linearized multiplier circuit capable of producing a low distortion reference for the line current over the full range of line and load conditions. A low-offset, high-bandwidth current error amplifier ensures that the actual inductor current (sensed through a resistor in the return path) follows the multiplier output command signal. The output voltage error is processed through a transconductance voltage amplifier.

DESCRIPTION (CONTINUED)

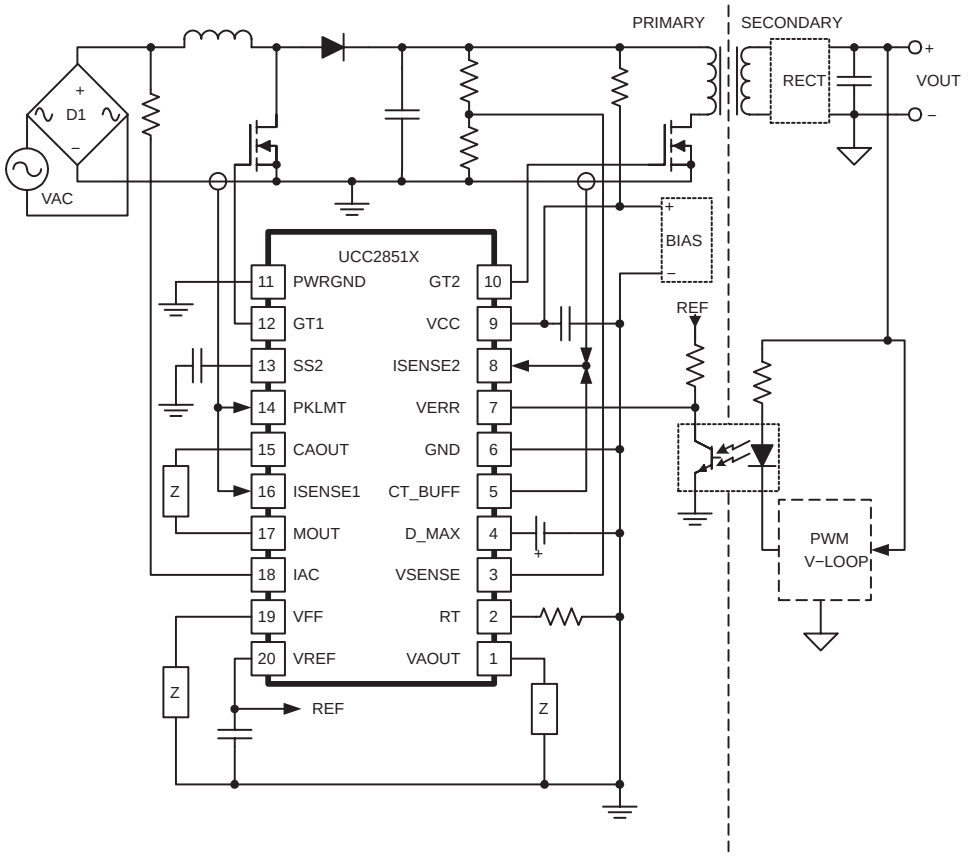
The transient response of the circuit is enhanced by allowing a much faster charge/discharge of the voltage amplifier output capacitance when the output voltage falls outside a certain regulation window. A number of additional features such as UVLO circuit with selectable hysteresis levels, an accurate reference voltage for the voltage amplifier, zero power detect, OVP/enable, peak current limit, power limiting, high-current output gate driver characterize the PFC section.

The PWM section features peak current mode control (with a ramp signal available to add slope compensation), programmable soft-start, accurate maximum duty cycle clamp, peak current limit and high-current output gate driver. The oscillator for the combination controller is available in two versions. In UCC28510, UCC28511, UCC28512, and UCC28513, the PWM and the PFC circuits are switched at the same frequency. In the UCC28514, UCC28515, UCC28516, and UCC28517, the PWM stage frequency is twice that of the PFC frequency. The PWM stage is suppressed until the PFC output has reached 90% of its programmed value during startup. During line dropout and turn off, the device allows the PWM stage to operate until the PFC output has dropped to 47% (UCC28512, UCC28513, UCC28516, and UCC28517) or 71% (UCC28510, UCC28511, UCC28514, and UCC28515) of its nominal value. See available options table on page 1 for a summary of options.

The UCC28510 family also features leading-edge modulation for the PFC stage and trailing-edge modulation for the PWM stage in order to reduce the ripple current in the boost output capacitor. The current amplifier implementation associated with this scheme also results in better noise immunity.

Available in 20-pin N and DW packages.

SIMPLIFIED APPLICATION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)†‡

- Supply voltage VCC
  - Idle . . . 20 V
  - Operating . . . 18 V
- Gate drive current (GT1, GT2)
  - Continuous . . . 0.4 A
  - Pulsed
    - Sourcing . . . −2.5 A
    - Sinking . . . 3.5 A
- Maximum GT1, GT2 voltage . . . −0.5 V to VCC+0.3 V
- Input voltage
  - VSENSE . . . 0 V to 11 V
  - D_MAX, SS2, CAOUT, ISENSE1, MOUT, VFF . . . −0.5 V to VREF+0.3 V
  - VAOUT, CT_BUFF, ISENSE2, PKLMT . . . −0.5 V to 6 V
- Pin Current
  - RT . . . −0.5 mA
  - VFF . . . −5 mA
  - CT_BUFF . . . 1 mA
  - VAOUT, VERR, ISENSE2, SS2, CAOUT, IAC . . . 10 mA
- Maximum pin capacitance
  - ISENSE2 . . . 220 pF
- Operating junction temperature range, T_J . . . −55 ^{0}C to 150 ^{0}C
- Storage Temperature range, T_{stg} . . . −65 ^{0}C to 150 ^{0}C
- Lead temperature 1.6mm (1/16 inch from case for 10 seconds) . . . 300 ^{0}C
- Power dissipation
  - PDIP (N) package . . . 1 W
  - SOIC (DW) package . . . 0.7 W

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute−maximum−rated conditions for extended periods may affect reliability.

‡ Currents are positive into, negative out of the specified terminal. All voltages are referenced to GND.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

PARAMETER	MAX	UNITS
Human body model	2.5	kV
CDM	0.5	

AVAILABLE OPTIONS†‡

OPTIONS					PACKAGED DEVICES	
PFC:PWM FREQUENCY RATIO	UVLO TURN-ON (V)	UVLO HYSTERESIS (V)	PWM UVLO2 TURN-OFF (V)	PWM UVLO2 HYSTERESIS (V)	PDIP−20 (N)	SOIC W−20 (DW)
1:1	16	6.3	5.30	1.45	UCC28510N	UCC28510DW
1:1	10.2	0.5	5.30	1.45	UCC28511N	UCC28511DW
1:1	16	6.3	3.55	3.2	UCC28512N	UCC28512DW
1:1	10.2	0.5	3.55	3.2	UCC28513N	UCC28513DW
1:2	16	6.3	5.30	1.45	UCC28514N	UCC28514DW
1:2	10.2	0.5	5.30	1.45	UCC28515N	UCC28515DW
1:2	16	6.3	3.55	3.2	UCC28516N	UCC28516DW
1:2	10.2	0.5	3.55	3.2	UCC28517N	UCC28517DW

† The DW package is available taped and reeled. Add R suffix to device type (e.g. UCC28510DWR) to order quantities of 2000 devices per reel.

‡ All devices are rated from −40°C to +105°C.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 105°C for the UCC2851x, $T_A = T_J$, VCC = 12 V, R_T = 156 kΩ, R_{CT_BUFF} = 10 kΩ (unless otherwise noted)

supply current

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply current, off	VCC turn-on threshold −300 mV		100	150	µA
Supply current, on	no load on GT1 or GT2		4	6	mA

undervoltage lockout (UVLO)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC turn-on threshold	UCC28510 UCC28512 UCC28514 UCC28516		15.4	16	16.6	V
	UCC28511 UCC28513 UCC28515 UCC28517		9.7	10.2	10.8	
VCC turn-off threshold	UCC2851X		9.1	9.7	10.6	
UVLO hysteresis	UCC28510 UCC28512 UCC28514 UCC28516		5.8	6.3	6.8	
	UCC28511 UCC28513 UCC28515 UCC28517		0.3	0.5	0.8	

voltage amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage	25°C	7.39	7.50	7.61	V
	Over temperature	7.35	7.50	7.65	
V_{SENSE} bias current	$V_{SENSE} = V_{REF}$		100	300	nA
Open loop gain	2 V ≤ VAOUT ≤ 4 V	50	60		dB
High-level output voltage	I_{LOAD} = –150 µA	5.3	5.5	5.6	V
Low-level output voltage	I_{LOAD} = 150 µA	0.00	0.05	0.15	
g_M conductance	I_{VAOUT} = −20 µA to 20 µA	70	100	130	µS
Maximum source current		−1	−3.5		mA
Maximum sink current		1	3.5		

PFC stage overvoltage protection and enable

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overvoltage reference window		VREF + 0.440	VREF + 0.490	VREF + 0.540	V
Hysteresis		300	500	600	mV
Enable threshold		1.7	1.9	2.1	V
Enable hysteresis		0.08	0.2	0.3	

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 105°C for the UCC2851x, $T_A = T_J$, VCC = 12 V, R_T = 156 kΩ, R_{CT_BUFF} = 10 kΩ (unless otherwise noted)

current amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input offset voltage	V_{CM} = 0 V, V_{CAOUT} = 3 V	–5	0	5	mV
Input bias current	V_{CM} = 0 V, V_{CAOUT} = 3 V		−50	−100	nA
Input offset current	V_{CM} = 0 V, V_{CAOUT} = 3 V		25	100	
Open loop gain	V_{CM} = 0 V, 2 V ≤ V_{CAOUT} ≤ 5 V	90			dB
Common−mode rejection ratio	0 V ≤ V_{CM} ≤ 1.5 V, V_{CAOUT} = 3 V	80			
High-level output voltage	I_{LOAD} = –500 µA	5.6	6.3	7.0	V
Low-level output voltage	I_{LOAD} = 500 µA	0	0.2	0.5	
Gain bandwidth product(1)	See Note 1		2.0		MHz

oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
f_{PWM}, PWM frequency, initial accuracy	T_A = 25°C	170	200	230	kHz
Frequency, voltage stability	10.8 V ≤ V_{CC} ≤ 15 V	−1%		1%	
Frequency, total variation	Line, Temp	160		240	kHz
dc-to-dc ramp peak voltage		4.5	5.0	5.5	V
dc-to-dc ramp amplitude voltage(1) (peak-to-peak)			4.0		
PFC ramp peak voltage		4.5	5.0	5.5	
PFC ramp amplitude voltage (peak-to-peak)		3.5	4.0	4.5	

voltage reference

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage	25°C	7.39	7.50	7.61	V
	Over temperature	7.35	7.50	7.65	V
Load regulation	I_{REF} = −1 mA to −6 mA		5	15	mV
Line regulation	10.8 V ≤ V_{CC} ≤ 15 V		1	10	
Short circuit current	VREF = 0V	−20	–25	−50	mA

peak current limit

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PKLMT reference voltage		–20	0	20	mV
PKLMT propagation delay	PKLMT to GT1	150	300	500	ns

multiplier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{MOUT}, high-line low-power output current	I_{AC} = 500 µA, VFF = 4.7 V, VAOUT = 1.25 V	−3	–6	−9	µA
I_{MOUT}, high-line high-power output current	I_{AC} = 500 µA, VFF = 4.7 V, VAOUT = 5 V	−75	–90	−110	
I_{MOUT}, low-line low-power output current	I_{AC} = 150 µA, VFF = 1.4 V, VAOUT = 1.25 V	−10	–15	−50	
I_{MOUT}, low-line high-power output current	I_{AC} = 150 µA, VFF = 1.4 V, VAOUT = 5 V	−245	–290	−330	
I_{MOUT}, IAC-limited output current	I_{AC} = 150 µA, VFF = 1.3 V, VAOUT = 5 V	−245	–290	−330	
Gain constant (k)	I_{AC} = 300 µA, VFF = 2.8 V, VAOUT = 2.5 V	0.8	1	1.2	1/V
I_{MOUT}, zero current	I_{AC} = 150 µA, VFF = 1.4 V, VAOUT = 0.25 V		0	–0.2	µA
	I_{AC} = 500 µA, VFF = 4.7 V, VAOUT = 0.25 V		0	–0.2	µA
	I_{AC} = 500 µA, VFF = 4.7 V, VAOUT = 0.5 V		0	–0.2	µA
Power limit ($I_{MOUT} \times V_{FF}$)	I_{AC} = 150 µA, VFF = 1.4 V, VAOUT = 5 V	−343	–406	−462	µW

1. Ensured by design. Not 100% tested in production.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 105°C for the UCC2851x, $T_A = T_J$, VCC = 12 V, R_T = 156 kΩ, R_{CT_BUFF} = 10 kΩ (unless otherwise noted)

zero power

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Zero power comparator threshold	Measured on VAOUT, falling edge	0.20	0.33	0.50	V
Zero power comparator hysteresis	Measured on VAOUT, rising edge	40	90	140	mV

PFC gate driver

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
GT1 pull-up resistance	−100 mA ≤ ΔI_{OUT} ≤ −200 mA		5	12	Ω
GT1 pull-down resistance	I_{OUT} = 100 mA		2	10	Ω
GT1 output rise time	C_{LOAD} = 1 nF, R_{LOAD} = 10 Ω		16	25	ns
GT1 output fall time	C_{LOAD} = 1 nF, R_{LOAD} = 10 Ω		7	15	ns
Maximum duty cycle		93%	95%	100%	
Minimum controllable pulse width		120	150	200	ns

PWM stage undervoltage lockout (UVLO2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM turn-on reference	UCC2851X		6.30	6.75	7.30	V
PWM turn-off threshold	UCC28510 UCC28511 UCC28514 UCC28515			5.3		V
	UCC28512 UCC28513 UCC28516 UCC28517			3.55		V
Hysteresis	UCC28510 UCC28511 UCC28514 UCC28515		1.16	1.45	1.74	V
	UCC28512 UCC28513 UCC28516 UCC28517		2.56	3.20	3.84	V

PWM stage soft-start

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SS2 charge current	V_{SENSE} = 7.5 V, SS2 = 0 V	–7.0	–10.5	–14.0	µA
SS2 discharge current	V_{SENSE} = 2.5 V, SS2 = 2.5 V, (UVLO2 = Low, ENABLE = High)	6	10	14	mA
Input voltage (VERR)	I_{VERR} = 2 mA,UVLO2 = Low			300	mV

PWM stage duty cycle clamp

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Maximum duty cycle	D_MAX = 4.15 V	70%	75%	80%	

PWM stage pulse-by-pulse current sense

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current sense comparator offset voltage	I_{SENSE2} = 0 V, measured on VERR	1.35	1.50	1.65	V

1. Ensured by design. Not 100% tested in production.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 105°C for the UCC2851x, $T_A = T_J$, VCC = 12 V, R_T = 156 kΩ, R_{CT_BUFF} = 10 kΩ (unless otherwise noted)

PWM stage overcurrent limit

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Peak current comparator threshold voltage		1.15	1.30	1.45	V
Input bias current(1)			50		nA

PWM stage gate driver

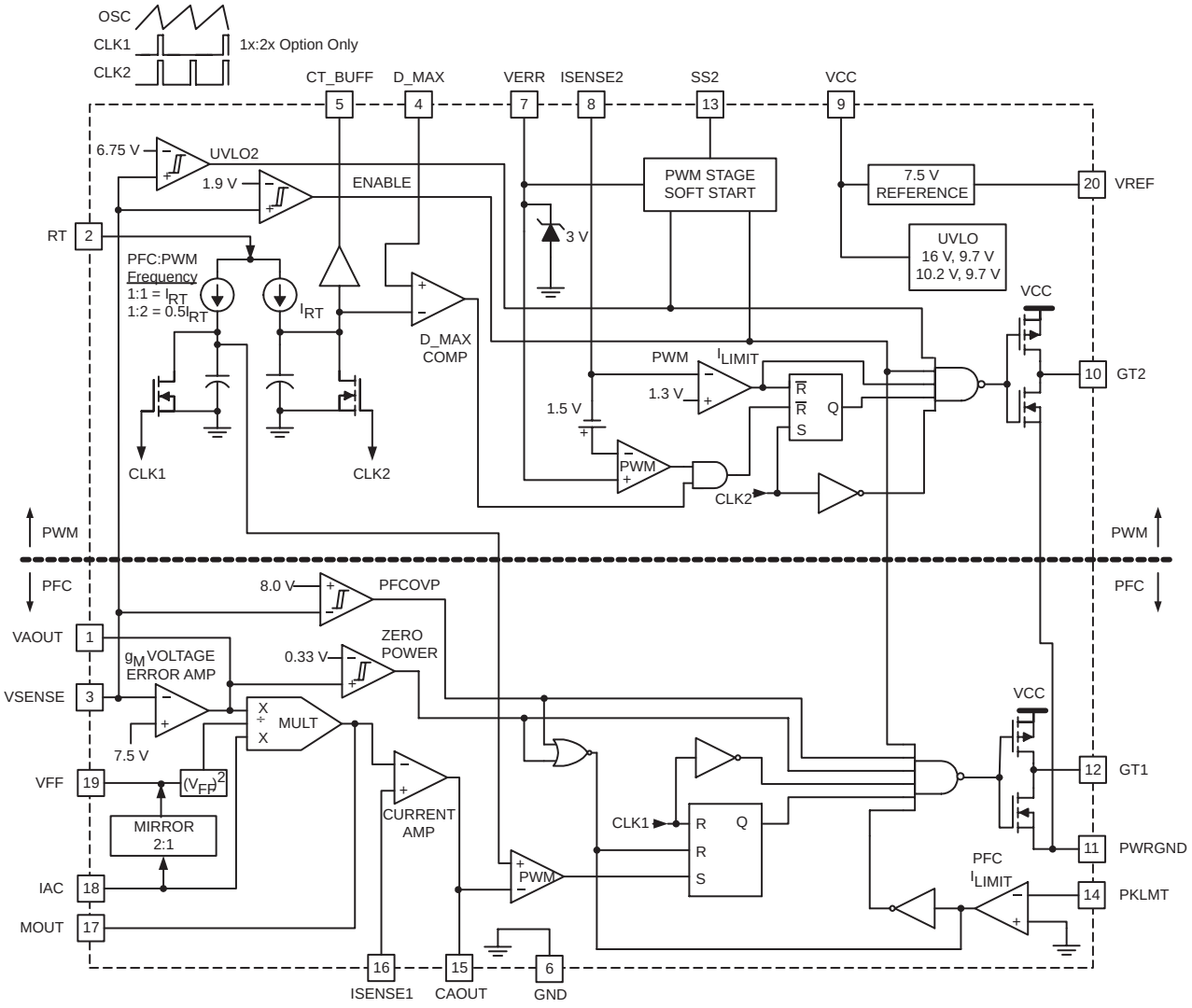
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
GT2 pull-up resistance	−100 mA ≤ ΔI_{OUT} ≤ −200 mA		5	12	Ω
GT2 pull-down resistance	I_{OUT} = 100 mA		2	10	Ω
GT2 output rise time	C_{LOAD} = 1 nF, R_{LOAD} = 10 Ω		16	25	ns
GT2 output fall time			7	15	ns

1. Ensured by design. Not 100% tested in production.

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	NO.	Stage		
CAOUT	15	PFC	O	Output of the current control amplifier of the PFC stage. CAOUT is internally connected to the PWM comparator input in the PFC stage
CT_BUFF	5	PWM	O	Internally buffered PWM stage oscillator ramp output, typically used to program slope compensation with a single resistor
D_MAX	4	PWM	I	Positive input to set the maximum duty cycle clamp level of the PWM stage
GND	6	–	–	Analog ground
GT1	12	PFC	O	PFC stage gate drive output
GT2	10	PWM	O	PWM stage gate drive output
IAC	18	PFC	I	Multiplier current input that is proportional to the instantaneous rectified line voltage
ISENSE1	16	PFC	I	Non-inverting input to the PFC stage current amplifier
ISENSE2	8	PWM	I	Input for PWM stage current sense and peak current limit
MOUT	17	PFC	I/O	PFC multiplier high−impedance current output, internally connected to the current amplifier inverting input
PKLMT	14	PFC	I	Voltage input to the PFC peak current limit comparator
PWRGND	11	–	–	Power ground for GT1, GT2 and high current return paths
RT	2	–	I	Oscillator programming pin that is set with a single resistor to GND
SS2	13	PWM	I	Soft start for the PWM stage
VAOUT	1	PFC	I/O	Output of the PFC transconductance voltage amplifier and it is internally connected to the Zero Power Detect comparator input and the multiplier input
VCC	9	–	I	Positive supply voltage pin
VERR	7	PWM	I	Feedback error voltage input for the PWM stage, typically connected to an optocoupler output
VFF	19	PFC	I	Voltage feedforward pin for the PFC stage, sources an IAC/2 current that should be externally filtered
VREF	20	–	O	Precision 7.5-V reference output
VSENSE	3	PFC	I	Inverting input to the PFC transconductance voltage amplifier, and input to the OVP, ENABLE and UVLO2 comparators

BLOCK DIAGRAM



DETAILED PIN DESCRIPTIONS

CAOUT (Pin 15): This is the output of a wide-bandwidth operational amplifier that senses line current and commands the PFC stage PWM comparator to force the correct duty cycle. This output can swing close to GND to command maximum duty cycle, and above the PFC ramp peak voltage to force zero duty cycle when necessary. Connect current loop compensation components between CAOUT and MOUT.

CT_BUFF (Pin 5): The 4-V amplitude oscillator ramp is internally buffered at this pin to allow a resistor to be connected directly from this pin to ISENSE2 for slope compensation. The internal buffer can drive a typical 500-µA resistive load at this pin.

D_MAX (Pin 4): Program the maximum duty cycle at GT2 by applying a dc voltage to this pin. Between 0.09 and 0.90, the maximum duty ratio is linearly related to D_MAX. Usually, this voltage is set with a precision resistor divider powered by VREF. A first order approximation, with the CT_BUFF frequency near 200 kHz, is estimated by:

$$D_{MAX} \cong \frac{V_{DX} - 1\ V}{4\ V}$$

where, D_{MAX} is a dimensionless ratio
V_{DX} is the voltage at D_MAX in volts

DETAILED PIN DESCRIPTIONS (CONTINUED)

The maximum duty ratio is modestly dependent on the switching frequency. A more accurate estimate of the maximum duty cycle that is valid over the full range of switching frequencies (65 kHz to 600 kHz) is given by:

$$D_{MAX} = \left(0.26 - \left(\frac{4.4 \times 10^{-8}}{Hz} \times f_S\right)\right)\frac{V_{DX}}{V} + \left(\frac{6.9 \times 10^{-8}}{Hz} \times f_S\right) - 0.31$$

where, f_S is the oscillator frequency measured at CT_BUFF in Hz

This pin can also be used to set D_{MAX} to 0 by setting V_{DX} less than 0.7 V.

GND (Pin 6): Signal ground for the integrated circuit. All voltages measured with respect to ground are referenced to this pin. The bypass capacitors for VCC and VREF should connect to this pin with as little lead length as possible. PWRGND must be externally connected to this pin. For best results, use a single small circuit trace to electrically connect between the circuits that use the GND return path and the circuits that use the PWRGND return path.

GT1 (Pin 12): A 2-A peak source and 3-A peak sink current totem pole MOSFET gate driver for the PFC stage. Some overshoot at GT1 can be expected when driving a capacitive load, but adding a minimal series resistor of about 2 Ω between GT1 and the external MOSFET gate can reduce this overshoot. GT1 is disabled unless VCC is outside the UVLO region and VREF is on.

GT2 (Pin 10): A 2-A peak source and 3-A peak sink current totem pole MOSFET gate driver for the PWM stage, identical to the driver at GT1.

IAC (Pin 18): This multiplier input senses the rectified ac line voltage. A resistor between IAC and the line voltage converts the instantaneous line voltage waveform into a current input for the analog multiplier. The recommended maximum IAC current is 500 μA.

ISENSE1 (Pin 16): This pin is the non-inverting input terminal of the current amplifier. Connect a resistor between this pin and the grounded side of the PFC stage current sensing resistor. The resistor connected to this pin should have a value that equals the value of the resistor that is connected between the MOUT pin and the ungrounded side of the PFC current sense resistor.

ISENSE2 (Pin 8): A voltage across the PWM stage external current sense resistor generates the input signal to this pin, with the peak limit threshold set to 1.3 V for peak current mode control. An internal 1.5-V level shift between ISENSE2 and the input to the PWM comparator provides greater noise immunity. The oscillator ramp can also be summed into this pin for slope compensation. Figure 36 shows the typical relationship of the capacitance on the ISENSE2 pin and the minimum controllable limit of the pulse width on the gate2 output. If the V_{ERR} is at the voltage that corresponds to a minimum controllable duty cycle and then is reduced further the pulse width collapses to near zero.

MOUT (Pin 17): The output of the multiplier and the input to the current amplifier in the PFC stage are internally connected at this pin. Set the power range of the PFC stage with a resistor tied between the MOUT pin and the non-grounded end of the PFC current sense resistor. Connect impedance between the MOUT pin and the CAOUT pin to compensate the PFC current control loop. The multiplier output is a current and the current amplifier input is high impedance. The multiplier output current is given by:

$$I_{MOUT} = \frac{\left(V_{VAOUT} - 1.0\right) \times I_{IAC}}{K \times \left(V_{VFF}\right)^2}$$

where, K is the multiplier gain constant, in $volts^{-1}$.

PKLMT (Pin 14): Program the peak current limit of the PFC stage using this pin. The threshold for peak limit is 0 V. Use a resistor divider between VREF and the non-grounded side of the PFC current sense resistor in order to shift the level of this signal to a voltage that corresponds to the desired overcurrent threshold voltage, measured across the PFC current sense resistor.

PWRGND (Pin 11): Ground for the output drivers at GT1 and GT2. This ground should be tied to GND externally via a single Kelvin connection.

DETAILED PIN DESCRIPTIONS (CONTINUED)

RT (Pin 2): A resistor between RT and GND programs the oscillator frequency, measured at CT_BUFF. In all options, the PWM stage operates at the frequency that is measured at CT_BUFF. In the UCC28510, UCC28511, UCC28512 and UCC28513, the PFC stage operates at the same frequency as the PWM stage. In the UCC28514, UCC28515, UCC28516 and UCC28517, the PFC stage operates at half the frequency of the PWM stage. The voltage is dc (nominally 3 V); do not connect a capacitor to this pin in an attempt to stabilize the voltage. Instead, connect the GND side of the oscillator-programming resistor closer to the GND pin. The recommended range of resistors is 45 kΩ to 500 kΩ for a frequency range of 600 kHz to 65 kHz, respectively. Resistor R_T programs the oscillator frequency f_S, as measured at CT_BUFF, according to the following equation:

$$R_T = \frac{1}{31 \times 10^{-12}} \left(\frac{1\ \text{Hz}}{f_S} - 2.0 \times 10^{-7} \right) \Omega$$

where, R_T is in Ω
f_S is in Hz

SS2 (pin 13): A capacitor between SS2 and GND programs the softstart duration of the PWM stage gate drive. When the UVLO2 comparator enables the PWM stage, an internal 10.5-μA current source charges the external capacitor at SS2 to 3 V to ramp the voltage at VERR during startup. This allows the GT2 duty cycle to increase from 0% to the maximum clamped by the duty cycle comparator over a controlled time delay t_{SS} given by:

$$C_{SS2} = \frac{t_{SS} \times 10.5 \times 10^{-6} \times \text{Amp}}{3\ \text{V}}$$

C_{SS2} is in Farads

In the event of a disable command or a UVLO2 dropout, SS2 quickly discharges to ground to disable the PWM stage gate drive.

VAOUT (Pin 1): This transconductance voltage amplifier output regulates the PFC stage output voltage and operates between GND and 5.5 V maximum to prevent overshoot. Connect the voltage compensation components between VAOUT and GND. When this output goes below 1 V, the multiplier output current goes to zero. When this output falls below 0.33 V, the zero power detect comparator ensures the PFC stage gate drive is turned off. In the linear range, this pin sources or sinks up to 30 μA. A slew rate enhancement feature enables VAOUT to sink or source up to 3.3 mA, when operating outside the linear range.

VCC (Pin 9): Chip positive supply voltage that should be connected to a stable source of at least 20 mA between 12 V and 17 V for normal operation. Bypass VCC directly to GND with a 0.1 μF or larger ceramic capacitor to absorb supply current spikes caused by the fast charging of the external MOSFET gate capacitances.

VERR (Pin 7): The voltage at this pin controls the GT2 duty cycle and is connected to the feedback error signal from an external amplifier in the PWM stage. This pin is clamped to a maximum of 3 V and can demand 100% duty cycle at GT2. The typical pull-up current flowing out of this pin is 10 μA.

VFF (Pin 19): The output current from this pin comes from an internal current mirror that divides the IAC input current by 2. The input voltage feedforward signal for the multiplier is then generated across an external single-pole R/C filter connected between VFF and GND. At low line, the VFF voltage should be set to 1.4 V.

VREF (Pin 20): This is the output of an accurate 7.5-V reference that powers most of the internal circuitry and can deliver over 10 mA, with a typical load regulation of 5 mV ensured for an external load of up to 6 mA. The internal reference is current limited to 25 mA, which protects the part if VREF is short-circuited to ground. VREF should be bypassed directly to GND with a ceramic capacitor between 0.1 μF and 10 μF for stability. VREF is disabled and remains at 0 V when VCC is below the 9.7-V UVLO threshold.

VSENSE (Pin 3): Inverting input to the PFC transconductance voltage amplifier, which serves as the PFC feedback connection point. When VSENSE operates within +/− 0.35 V of its steady-state value, the current at VAOUT is proportional to the difference between the VREF and VSENSE voltages by a factor of g_M. Outside this range, the magnitude of the current of VAOUT is increased in order to enhance the slew rate for rapid voltage control recovery in the PFC stage. Decisive activation and deactivation of the voltage control recovery is internally implemented with about 120 mV of hysteresis at VSENSE. VSENSE is internally connected to the PFC OVP, Enable and UVLO2 comparators as well.

APPLICATION INFORMATION

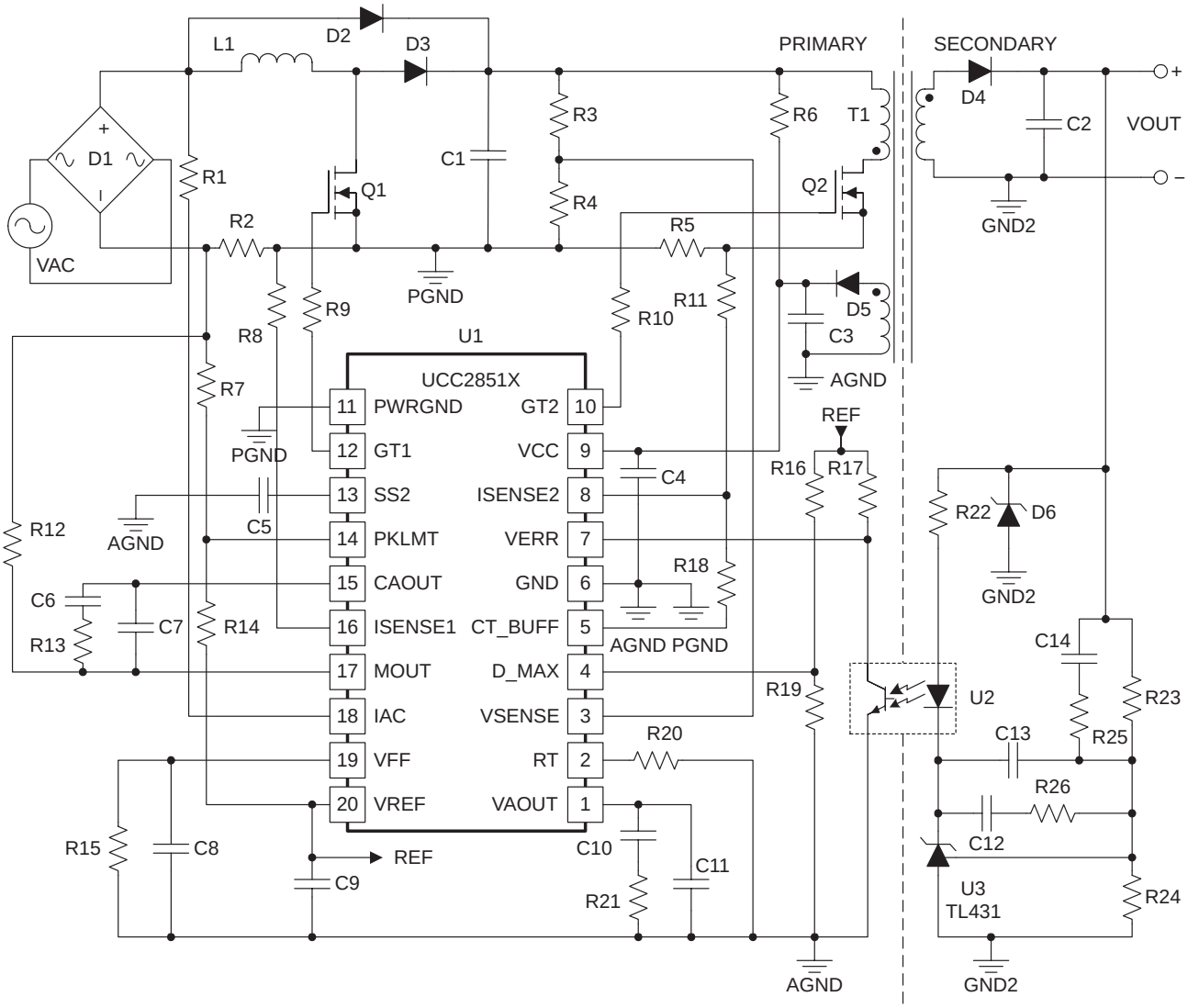


Figure 1. Typical Application Circuit: Boost PFC and Flyback PWM Power System

APPLICATION INFORMATION

The UCC28510 series of combination controllers include a power factor correction (PFC) controller that is synchronized with a pulse width modulator (PWM) controller integrated into one chip. The PFC controller has all of the features for an average current mode controlled PFC. The PWM controller has all of the features for an isolated peak current program mode controlled converter. The two controllers are synchronized at a fixed frequency so that the PFC controller is leading edge modulated (LEM) and the PWM controller is trailing edge modulated (TEM). The LEM/TEM combination reduces the ripple current in the energy storage capacitor of the PFC stage. A comparison between the ripple current in the energy storage capacitor with traditional TEM/TEM modulation versus LEM/TEM modulation is shown in Figure 2.

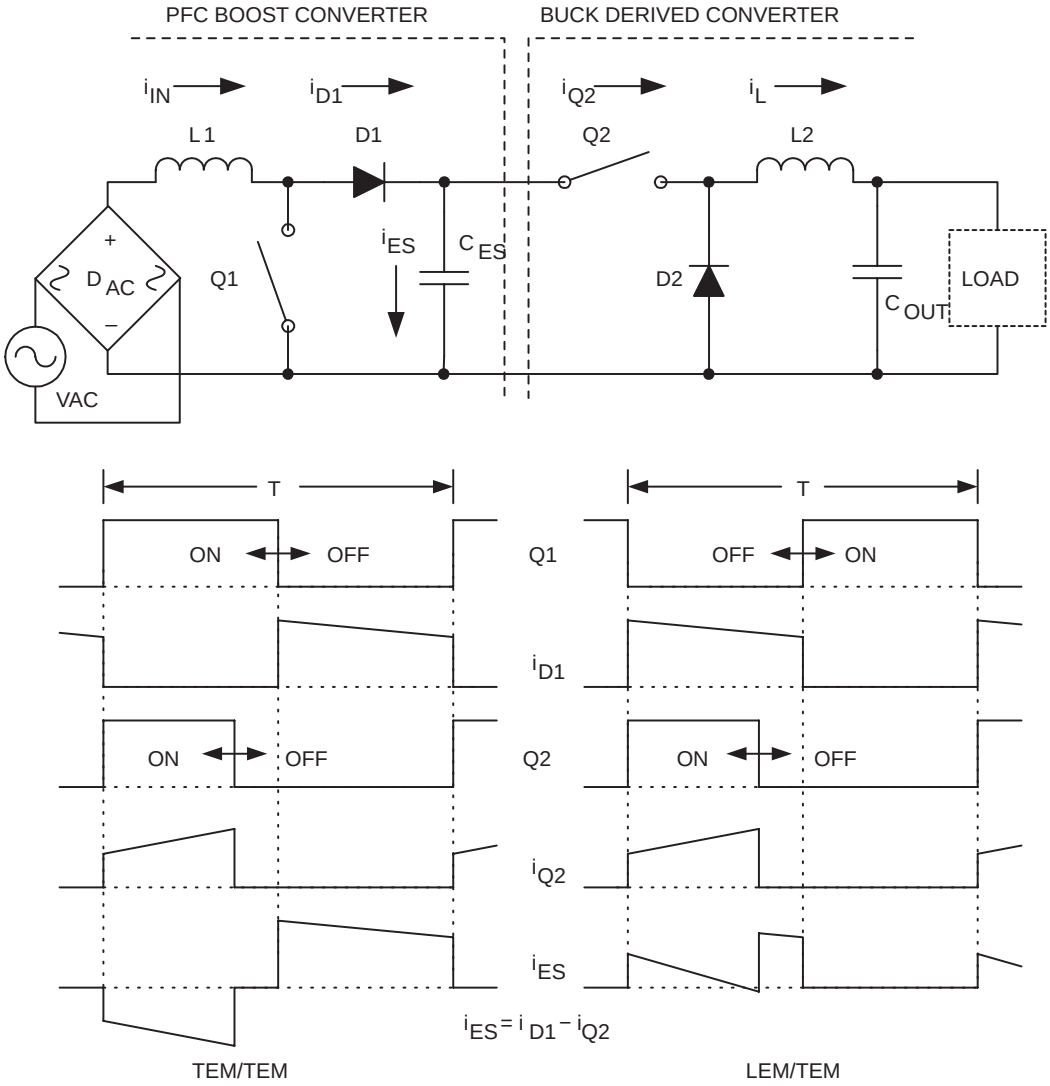


Figure 2. Equivalent PFC+PWM Power Supply System and the Comparison of the Energy Storage Capacitor Current for Traditional TEM/TEM with LEM/TEM Controllers.

APPLICATION INFORMATION

selection of controller options

The UCC2851x is optimized for the most common combination of PFC/PWM stages, which is a boost PFC stage cascaded by a buck-derived PWM stage. Other topology combinations can be used with this controller, as well. The programmable PWM duty ratio limit feature is especially useful when using two-transistor forward and flyback topologies for the PWM stage. The PFC boost stage is typically designed for continuous conduction mode (CCM) of operation at full rated load in order to minimize line filter requirements. The PWM stage can be designed for either continuous or discontinuous mode operation, as necessary.

Eight different options are available for the UCC2851x. This device is available in two under voltage lock out (UVLO) turn-on thresholds, two PWM UVLO hysteresis levels and, two combinations of PFC/PWM switching frequencies as shown in Table 1.

Table 1. Available Options

UVLO TURN-ON THRESHOLD (V)	PWM HYSTERESIS (V)	PFC:PWM FREQUENCY RATIO	
		1:1	1:2
16	1.45	UCC28510	UCC28514
10.2		UCC28511	UCC28515
16	3.20	UCC28512	UCC28516
10.2		UCC28513	UCC28517

Select the UVLO option first, based on biasing topology. Then, select the PFC versus PWM switching frequency based on the allowable switching loss of the intended PWM stage. Last, select the PWM UVLO option based on bulk ripple voltage and load transients.

The UVLO turn-on threshold is selected based on line range, bias supply topology and gate drive voltage requirements. The 16-V turn-on options are intended for applications where the bias voltage is self-generated from an auxiliary winding, with little or no regulation. The 10.2-V turn-on / 0.5-V hysteresis options are intended for applications where the bias voltage is derived from an auxiliary supply source and is regulated.

The PWM UVLO hysteresis level option is selected based on the desired operational range of the energy storage capacitor voltage. A narrow range permits a highly optimized PWM stage. However, the wider range permits larger energy storage capacitor voltage ripple and load transients.

Two options are available for the PFC:PWM switching frequency, 1:1 and 1:2. Both versions are synchronized as LEM/TEM oscillators. The best minimization of the energy storage capacitor ripple current occurs with the 1:1 option. However, the diode in the PFC stage often has high reverse recovery currents that restrict the switching frequency of the PFC stage. Situations where the switching losses of the PWM stage permit higher switching frequencies can benefit from the 1:2 option. For example, the 1:2 option would be a good choice for PWM stages that have Schottky diode output rectifiers. The energy storage capacitor ripple current for a system that is controlled by the 1:2 option will be larger than if it were controlled by a 1:1 option. However the capacitor current of the 1:2 option is less than a system that is TEM/TEM modulated.

APPLICATION INFORMATION

design procedure

The following discussion steps through the typical design process of a PFC/PWM converter system that is controlled by one of the UCC28510 options. The design process begins with the power stage elements, then the control elements for the PFC stage, then the control elements for the PWM stage. Keep in mind that a general design process is often iterative. Iteration typically begins after either simulating and/or testing the completed PFC/PWM system. This design procedure refers to the typical application in Figure 1.

A design begins with a list of requirements for output voltage, output power and ac line voltage range. Other details, such as efficiency and permissible current harmonics could be given at the onset, or developed throughout the product design cycle. The need for power factor correction arises from either an agency requirement, such as IEC−61000, or if the available line power is nearly equal to the output power of the power system. Hold-up time requirements are also necessary at the early stages of design. Typically, the hold-up time, t_{HU}, is at least the period of 1.5 line cycles.

The general structure of the PFC/PWM stage power system is two switched-mode converters connected in cascade. Each stage has an associated efficiency and each stage has its own set of fault limiting controls that must be properly set in order to achieve the desired line harmonic and load regulation performance, simultaneously. The PFC stage must always be designed to supply sufficient average power to the PWM stage. The cycle-by-cycle current limit of the PFC stage should be programmed to activate at a slightly larger power level at low ac line voltage than the average power clamp in order to allow for PFC current sense tolerances. This will allow power factor correction for the full range of maximum rated load. If the instantaneous load nearly equals the average load, then the fault clamps for the PWM stage can be programmed to limit power at a level that is slightly less than or equal to the average power clamp of the PFC stage. The margin for the clamping action should allow for measurement tolerances and efficiency. Conversely, if the instantaneous load has high peaks that are much shorter than the hold-up time, the current limit and duty ratio limits of the PWM stage can clamp at a higher level than the average power clamp in the PFC stage. In order to simplify the design procedure, the average and the peak loads of the PWM stage are assumed to be equal. Thus, all of the current limits and duty cycle limits are programmed to clamp power at a slightly lower level (10%) than the average power clamp on the PFC stage.

developing the internal parameters

Select the energy storage voltage V_{C1} (the voltage on the PFC output capacitor). Since the PFC stage is a boost converter, the voltage across C1 must be larger than the peak ac line voltage by enough to permit controllability in the event of load transients. Typically, this will be around 5% which is about 400 V for a universal ac line application of 85 V_{AC} to 265 V_{AC}.

Once the energy storage voltage, V_{C1}, is determined, the range of the PFC stage duty ratio, D_1, is set. For CCM operation of the PFC stage, the minimum PFC duty ratio is given by:

$$D_{1(min)} = 1 - \frac{\sqrt{2} \times VAC_{MIN}}{V_{C1}} \quad (1)$$

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Select the regulation constant, k_{1R}, of the energy storage voltage, as described by equation 2.

$$k_{1R} \cong \left[\begin{array}{l} 0.29 \text{ for UCC28510, UCC28511, UCC28514, UCC28515} \\ 0.53 \text{ for UCC28512, UCC28513, UCC28516, UCC28517} \end{array}\right] \quad (2)$$

There are effectively two options for k_{1R} that directly relate to the two PWM hysteresis options, $k_{1R} = 0.29$ and $k_{1R} = 0.53$. Select the large PWM hysteresis option if the system load has large, sudden step changes during steady state operation. Select the small PWM hysteresis option if the system load has moderate step changes or slow load changes during steady state operation. The PWM stage can be optimized best with the small PWM hysteresis range because the maximum primary current of transformer T1 (which occurs at minimum V_{C1}) is smallest with the small PWM hysteresis range.

Select an approximate switching frequency for the PFC stage. A good starting frequency for a MOSFET based PFC stage is in the range of 100 kHz to 200 kHz, depending on maximum line voltage and maximum line current. Adjustments in switching frequency may result from meeting switching loss requirements in Q1 and D3, or in order to optimize the design of L1.

Select an appropriate topology for the PWM stage using the information about the power requirements and the magnitude of V_{C1}. For simplicity, the typical application in Figure 1 shows a flyback converter in the PWM stage. In most cases, the PWM stage topology must have transformer isolation and the topology must require only one pulse-width signal. Topologies that have these features include:

- single-transistor forward converter
- single-transistor flyback converter
- two-transistor forward converter
- two-transistor flyback converter

Estimate the nominal and the maximum duty ratios of the PWM stage ($D_{2(nom)}$, $D_{2(max)}$ and the associated peak Q2 drain current, $i_{Q2(peak)}$), based on the topology, PWM hysteresis option and output voltage requirements of the PWM stage. Also estimate whether or not it is appropriate to operate the PWM stage at the same switching frequency as the PFC stage or if the PWM stage can operate at twice the switching frequency of the PFC stage. Base the estimation for the switching frequency of the PWM stage on the maximum voltages and currents of the power MOSFETs and power diodes. Program the oscillator frequency of the PWM stage with the value of R20.

$$R20 = \frac{1\ \Omega}{31 \times 10^{-12}} \left(\frac{1\ \text{Hz}}{f_{S(pwm)}} - 2.0 \times 10^{-7} \right) \quad (3)$$

Most applications require that the PWM stage regulates at the minimum energy storage capacitance voltage. Maximum duty ratio $D_{2(max)}$ and $i_{Q2(peak)}$ should be calculated for the minimum energy storage voltage in order to estimate the peak current stresses for transformer T1 and any other inductive element in the PWM stage.

$$V_{C1(min)} = \left(1 - k_{1R}\right) \times V_{C1(nom)} \quad (4)$$

At this point, enough information is available to estimate which member of the UCC28510 family should be selected.

APPLICATION INFORMATION

power stage elements

The power stage elements include the following elements: C1−3, D1−5, L1, R2, R5, Q1, Q2, T1. Details concerning the PWM stage elements C2, D4, D5, Q2 and T1 will not be discussed in detail here, due to their dependence on the choice PWM stage topology. The PWM stage is an isolated dc-to-dc topology with the same stresses and loss mechanisms that are typical for the selected topology. An estimation of the average steady state duty ratio of the PWM stage and the Q2 switch current will be needed for stress estimations in the PFC stage. Also, the natural step response of the PWM stage is required to estimate the soft start capacitor, C5, and the bias supply capacitor, C3.

The selection process of the PFC stage elements C1, C3, D1−3 and Q1 are discussed in detail here. In general, the selection process for the PFC stage elements is the same as for a typical fixed switching frequency PFC design, except for capacitor C1 due to PFC/PWM stage synchronization.

Diode bridge D1 is selected to withstand the rms line current and the peak ac line voltage. Diode D2 allows capacitor C1 to charge during initial power up without saturating L1 and it is selected to withstand the peak inrush current and peak of the maximum ac line voltage. Additional inrush current limiting circuitry in series with the ac line could be required, depending on agencies or situations.

The PFC stage inductor, L1, is selected to have a maximum current ripple at the minimum ac line voltage. Typically a ripple factor, k_{RF}, is chosen to be about 0.2. If the line current has excessive crossover distortion, a larger ripple factor (perhaps 0.3) will reduce the distortion but the line current will have more switching ripple. Initially, the inductance can be estimated by approximating the input power equal to the output power.

$$L1 = \frac{V_{AC(min)}^{2} \times D_{1(min)} \times T_{S(pfc)}}{k_{RF} \times P_{IN}} \quad (5)$$

where, $k_{RF} = \frac{\Delta i_{L1(p-p)}}{i_{L1(max)}}$

and $T_{s(pfc)}$ is $\frac{1}{\text{switching frequency of the PFC}}$

Inductor L1 must be designed to withstand the maximum ac rms line current without saturation at the peak ac line current.

Select power MOSFET Q1 and diode D3 with the same criteria that is normally used for fixed switching frequency PFC design. They must have sufficient voltage rating to withstand the energy storage voltage, V_{C1} and they must have sufficient current ratings. Gate drive resistor R9 is necessary to limit the source and sink current from the GT1 pin. Some circumstances require additional gate drive components for improved protection and performance.[10] A similar gate drive resistor, R10, is required between the GT2 pin and the gate of Q2 for the same reason.

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The current sense resistor for the PFC stage, R2, is selected to operate over a 1-V dynamic range ($V_{DYNAMIC}$). The sense resistor must also have a large enough power rating to permit safe operation with the maximum RMS line current.

$$R2 = \frac{V_{DYNAMIC}}{i_{L1(max)} + 0.5 \times \Delta i_{L1(p-p)}} \tag{6}$$

$$\text{where, } i_{L1(max)} = \frac{\sqrt{2} \times P_{IN}}{V_{AC(min)}}$$

The PFC I_{LIMIT} comparator threshold is at the ground reference for the controller device. So, the PFC current sense voltage, measured at PKLMT must be biased with a positive voltage to cross 0.0 V when the instantaneous PFC current is at its maximum. The bias voltage is established with R14 and R7, as shown in equation 7, and resistor R14 is arbitrarily chosen around 10 kΩ.

$$\frac{R7}{R14} = \frac{1}{\frac{V_{REF}}{i_{L1(max)} \times R2} - 1} \tag{7}$$

The capacitance value of the energy storage capacitor, C1 is selected to meet hold-up time requirements (t_{HU}) by the equation:

$$C1 = \frac{2 \times P_{OUT} \times t_{HU}}{V_{C1}^{\,2} \times k_{R1}\left(2 - k_{R1}\right)} \tag{8}$$

Capacitor C1 must be rated for the selected energy storage voltage and it must be able to withstand the rms ripple current, $I_{C1(rms)}$, that is produced by the combined action of the PFC stage and the PWM stage. The average Q2 drain current during the interval that GT2 activates MOSFET Q2 is used to find $I_{C1(rms)}$. An initial estimate can be made using the inequality in equation 9, then consult Figure 3 or Figure 4 for better accuracy.

$$\frac{I_{C1(rms)}}{I_{Q2}} < \sqrt{\frac{8 \times \sqrt{2} \times D_{2(nom)}^{\,2} \times V_{C1(nom)}}{3 \times \pi \times V_{AC(min)}} + D_{2(nom)}} \tag{9}$$

The ratio of $I_{C1(rms)}$ to I_{Q2} can be found by using the appropriate graph, Figure 3 for the 1X:1X oscillator option or Figure 4 for the 1X:2X oscillator option. To use the graphs, locate the ratio of VAC to V_{C1} along the horizontal axis then, draw a vertical line to the intersection of the curve for the duty ratio of the PWM stage. Draw a horizontal line from the intersection to the vertical axis and read the ratio of $I_{C1(rms)}$ to I_{Q2}.

APPLICATION INFORMATION

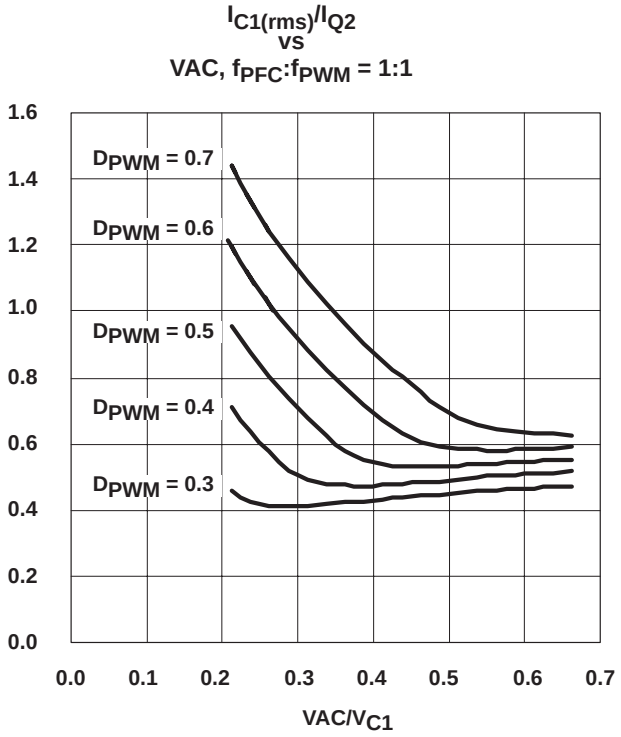

Figure 3. Graph for Finding $I_{C1(rms)}$ for the 1X:1X Oscillator Option

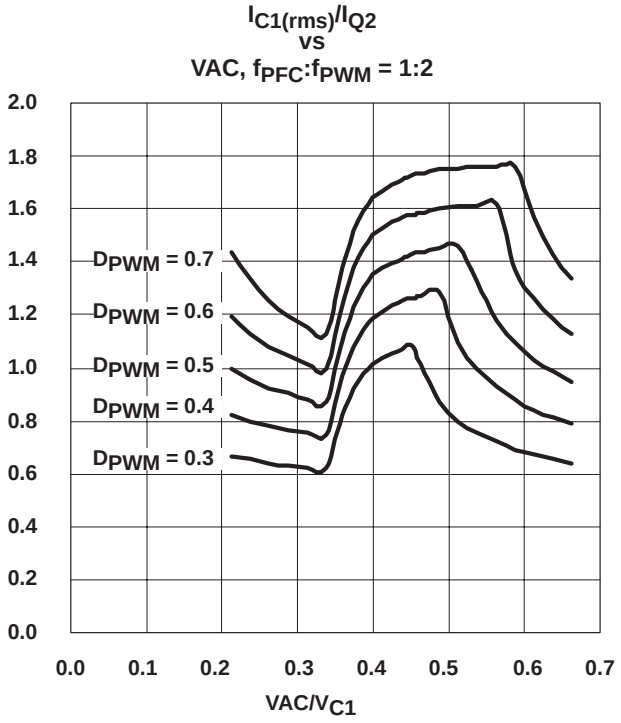

Figure 4. Graph for Finding $I_{C1(rms)}$ for the 1X:2X Oscillator Option

APPLICATION INFORMATION

The current sense resistor for the PWM stage, R5, is selected so that at maximum current, its voltage is the threshold voltage of the peak current comparator (nominally 1.3 V).

$$R5 = \frac{V_{TH}\left(\text{PWM stage} \times I_{LIMIT}\right)}{i_{Q2(peak)}} \quad (10)$$

In many cases, an input line filter will be necessary in order to meet the requirements of an agency or application. The input line filter design has been omitted from this procedure due to the vast array of requirements and circumstances. We urge you to refer to Reference [11] for details.

PFC stage control

The PFC stage is designed in a three-step process. First, set the dynamic range of the multiplier, second, stabilize the average current control loop and third, stabilize the voltage loop that controls the energy storage capacitor voltage. Use as much of the dynamic range of the multiplier as possible. The current control loop must have wide bandwidth in order to follow the instantaneous rectified line voltage. The voltage loop must be slower than twice the ac line frequency so that it will not compromise the power factor.

multiplier

The dynamic range of the multiplier is a function of the currents and/or voltages of the IAC, VAOUT and VFF pins. Coordinate the selection process to use the full range of the multiplier and obtain the desired power limiting features. Select the components R1 and R15 to use the $i_{IAC}(t)$ range and the V_{VFF} range under the condition that the maximum of the V_{VAOUT} range, described in equation 11. The selection process is similar to the selection process for UC3854, except for the VFF voltage and MOUT current limitations.[12] In this product series, the divide-by-square function is internally implemented so that it divides by the greater of 1.4 V or V_{VFF}. If the 1.4-V level controls the divider, power factor correction may still occur if the VAOUT level is within the functioning range of the multiplier. Power factor correction occurs during that condition because the multiplier section functions as a two-input multiplier, rather than a three-input multiplier. Notice that the voltage at the VFF pin will be proportional to the average of the IAC current. Typically, V_{VFF}=1.4 V at low ac line voltage is set as the design boundary; the upper boundary of V_{VFF} will remain within the range if the functional ac line voltage range varies by less than 4.3:1.

$$0 \le i_{IAC}(t) \le 500\ \mu A, \quad (11)$$

$$0 \le V_{VAOUT}(t) \le 5\ V,$$

$$1.4\ V \le V_{VFF} \le V_{VREF} - 1.4\ V$$

APPLICATION INFORMATION

The selection process begins with the selection of R1 so that the peak I_{AC} current at high ac line is about 500 μA, see Table 2. Second, select R15 for the minimum VFF voltage, also shown in Table 2. Third, select C8, in Table 2, to average the VFF voltage with sufficiently low ripple to meet a third harmonic distortion budget. For a system with a 3% THD target, it is typical to allow the feedforward circuit to contribute 1.5% third harmonic distortion to the input waveform [4]. An attenuation factor of 0.022 will meet the criteria. Finally, select the MOUT resistor in Table 2, R12, so that the voltage across R12 equals the voltage across sense resistor R2 under the condition of maximum power, minimum ac line voltage ($V_{VFF, MIN}$), and VAOUT at its maximum level of 5 V. Experimentally, the multiplier output resistor, R12, may need to be increased slightly if the energy storage capacitor voltage sags under maximum load. This would be due to tolerances in the components and the multiplier. In order to minimize current amplifier offsets, set the value of the resistor on the ISENSE1 pin, R8, equal to the value of R12 as shown in in Table 2.

Table 2.

REFERENCE DESIGNATOR	EQUATION	NOTES
R1	$\frac{\sqrt{2}V_{AC(max)}}{I_{IAC(peak)}}$	set $i_{IAC(peak)} = 500\ \mu A$
R15	$2 \times R1 \times \frac{V_{VFF(avgmin)}}{V_{AC(min)} \times 0.9}$	set $V_{VFF(avgmin)} = 1.4\ V$
C8	$\frac{1}{2 \times \pi \times f_{AC} \times A_{FF(2)} \times R15}$	$A_{FF(2)} = 0.022$ for 3% THD
R12	$\frac{I_{pk} \times R1 \times R2 \times k \times \left(V_{FF(min)}\right)^2}{\sqrt{2} \times V_{AC(min)} \times \left(V_{VAOUT(max)} - 1\ V\right)}$	k = 1/V $V_{AC(min)}$ = minimum RMS input voltage $V_{VFF(min)}$ = 1.4V $V_{VAOUT(max)}$ = 5.0V
R8	R12	Always change R8 if R12 is changed

PFC current loop control

This controller uses average current loop control for the PFC stage. The current control loop must typically be fast enough to track the rectified sinusoidal ac line voltage. There are many ways to design a controller that will stabilize the PFC current loop. The method that is described here achieves good results for most applications.[5] This method assumes that both the natural frequency of the system and the zero of the linearized boost PFC are much lower than both the switching frequency and the desired crossover frequency, $f_{CO(pfc)}$, as described in equation 12. The left side of the inequality in equation 12 will usually be true since the capacitance of C1 is quite large.

$$\frac{1 - D_{PWM(min)}}{\sqrt{L1 \times C1}} \text{ and } \frac{2P_{IN}}{C1 \times V_{C1}^{\ 2}} << 2 \times \pi \times f_{CO(pfc)} << 2 \times \pi \times f_{S(pfc)} \quad (12)$$

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The left side of the inequality should be at least a factor of 10 lower than the middle term; the right side of the inequality should be at least five times larger than the middle term. For the purposes of 50 Hz to 60 Hz power factor correction, good results can be achieved with the crossover frequency set to about 10 kHz. A lower crossover might be necessary if the switching frequency of the PWM stage is below 100 kHz, or if the compensator gain at the crossover frequency is large (over ~40 dB).

Upon selecting the crossover frequency, select R13 to set the gain at the crossover frequency, then select C6 to place a zero at the crossover frequency and select C7 to provide a pole at half of the switching frequency. The equations are in Table 3.

Table 3.

REFERENCE DESIGNATOR	EQUATION	NOTES
R13	$R12 \times \frac{2 \times \pi \times f_{CO(pfc)} \times L1 \times V_{CT\_BUFF(p-p)}}{V_{C1} \times R2}$	$V_{CT\_BUFF(p-p)} = 4\ V$ V_{C1} is the output voltage of the PFC
C6	$\frac{1}{R13 \times 2 \times \pi \times f_{CO(pfc)}}$	
C7	$\frac{1}{\pi \times f_{S(pfc)} \times R13}$	

PFC voltage loop

The voltage loop must crossover at a lower frequency than twice the ac line frequency so that voltage corrections will not interfere with power factor correction. Second harmonic ripple from the sensed V_{C1} voltage directly results in third harmonic distortion on the ac line, similar to ripple on the VFF voltage.

PWM stage control

The control elements of the PWM stage are the same as a typical isolated current program mode converter. The secondary elements include C12 to C14, D6, R22 to R25, U2 and U3, which perform the error amplifier, compensation and isolation functions. On the primary side, VERR is connected to the node between the opto-isolator output, U2, and a pull-up resistor, R17. Resistor R17 represents the gain in the conversion from the output current of opto-isolator U2 and the VERR input.

Slope compensation is programmed using resistors R18 and R11, which form a summing node at ISENSE2. The voltage at CT_BUFF is a saw-tooth waveform that swings between 1 V and 5 V.

Many applications require a duty ratio limit for the PWM stage in order to prevent transformer saturation. Program the maximum duty ratio using the following ratio of resistors R16 to R19.

$$\frac{R16}{R19} = \frac{V_{VREF}}{1\ V + 4\ V \times D_{PWM(max)}} - 1 \quad (13)$$

Soft-start

The soft-start capacitor, C5, which is connected to SS2, controls the soft-start ramp of the PWM stage. The soft-start ramp begins when the VSENSE voltage exceeds 6.75 V. In order to avoid loop saturation, the soft-start ramp rate must be less than or equal to the open loop response of the PWM stage converter.

REFERENCE DESIGN

Universal line input 100-W PFC output with 12 V, 8-W bias rail supply design is discussed in UCC28517EVM, TI literature number SLUU117. The schematic is shown in Figures 5, 6, 7. Please refer to the SLUU117 document on http://www.ti.com for further details.

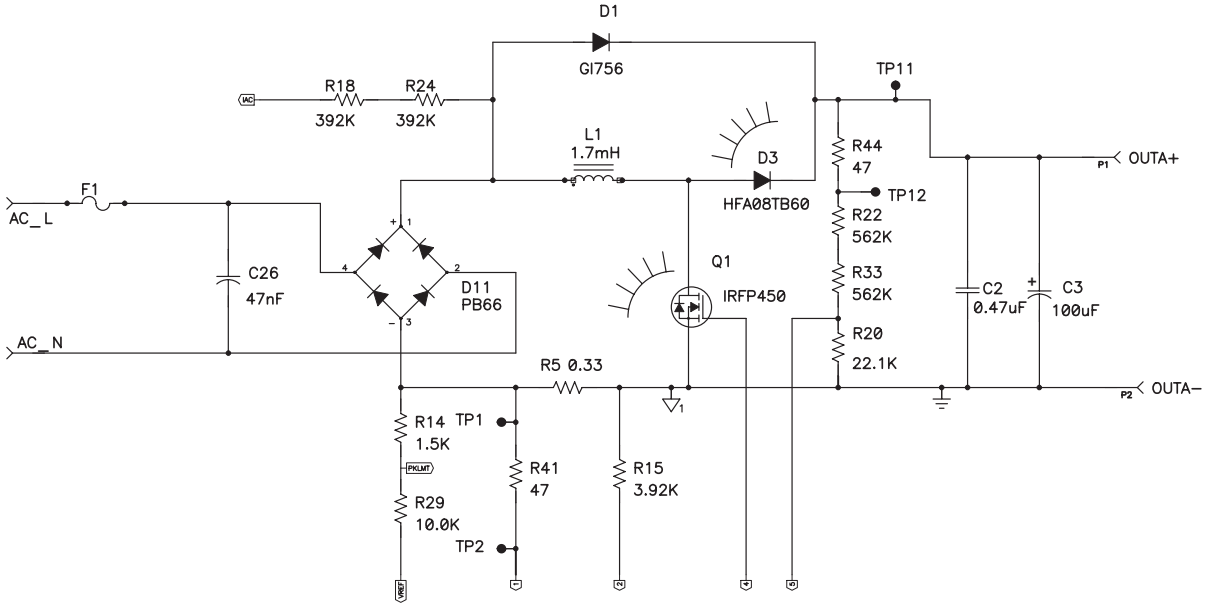


Figure 5. Section A

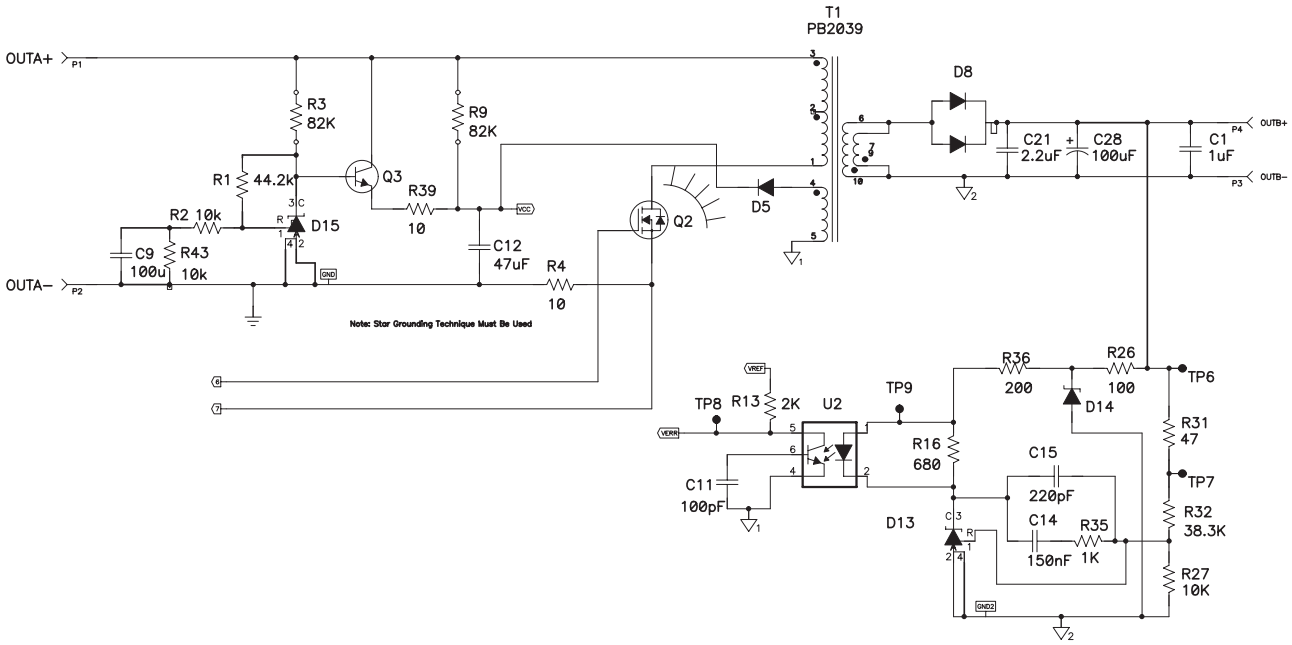
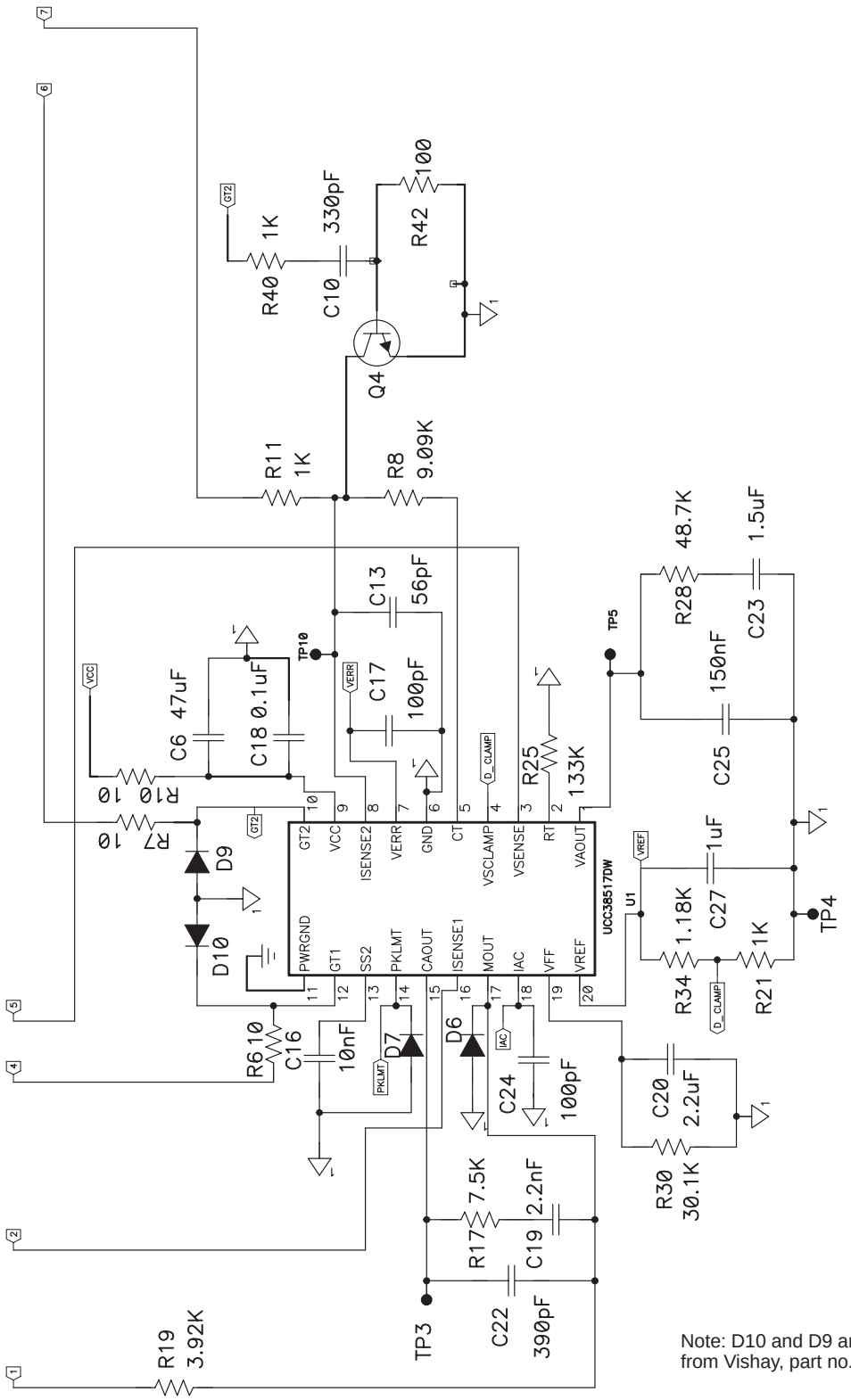


Figure 6. Section B

REFERENCE DESIGN



Note: D10 and D9 are Schottky diodes from Vishay, part no. BYS10−25

Figure 7. Section C

TYPICAL CHARACTERISTICS

STARTUP CURRENT vs TEMPERATURE

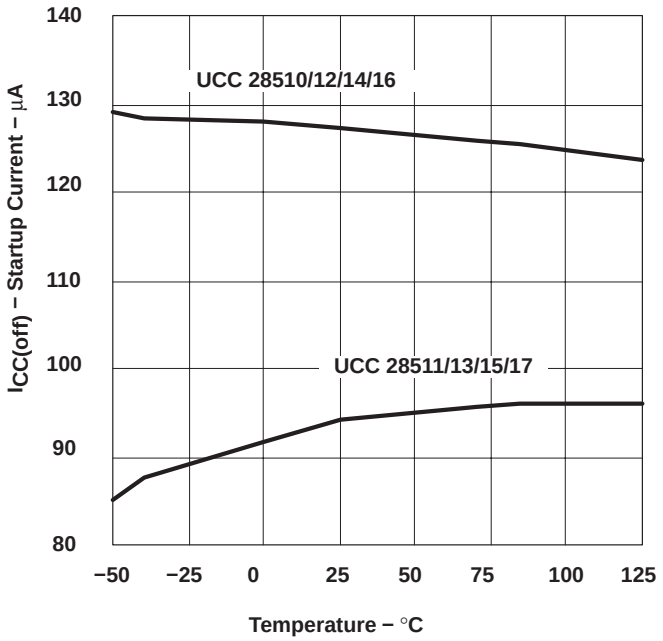


Figure 8

SUPPLY CURRENT vs TEMPERATURE

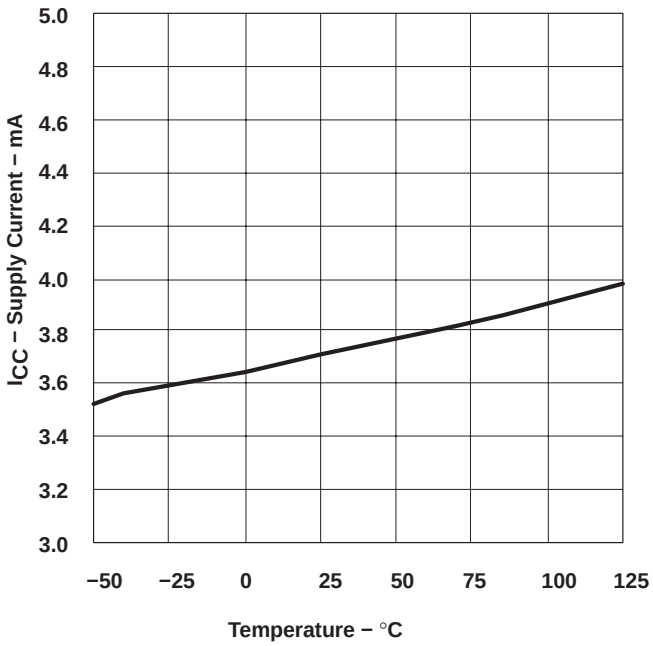


Figure 9

SUPPLY CURRENT vs SUPPLY VOLTAGE

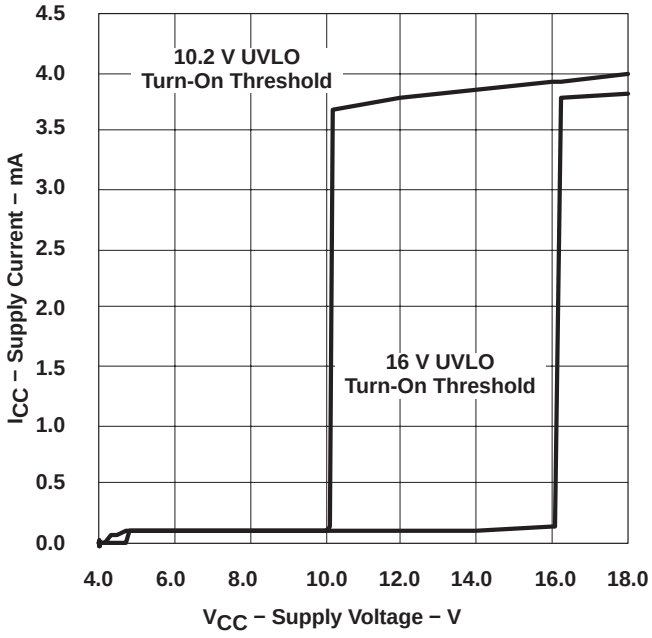


Figure 10

REFERENCE VOLTAGE vs TEMPERATURE

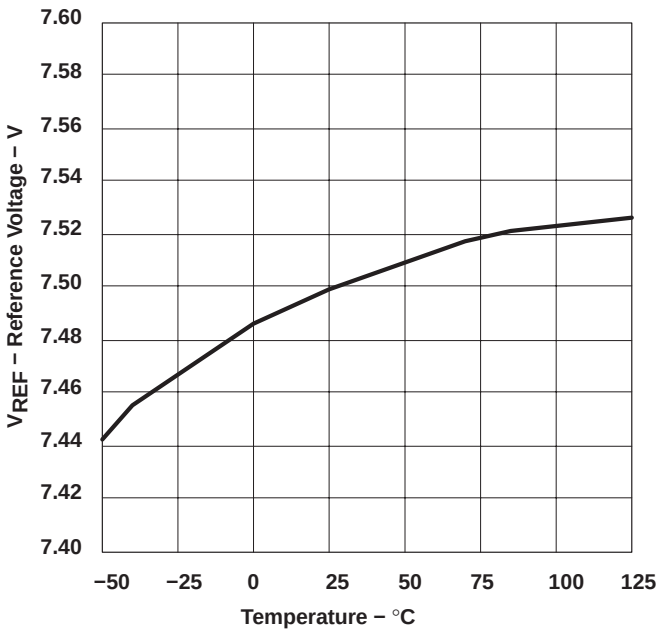


Figure 11

TYPICAL CHARACTERISTICS

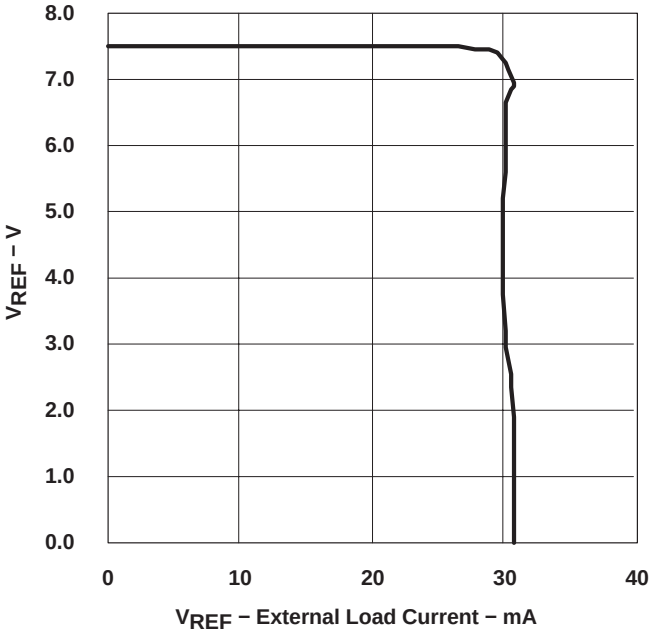


Figure 12

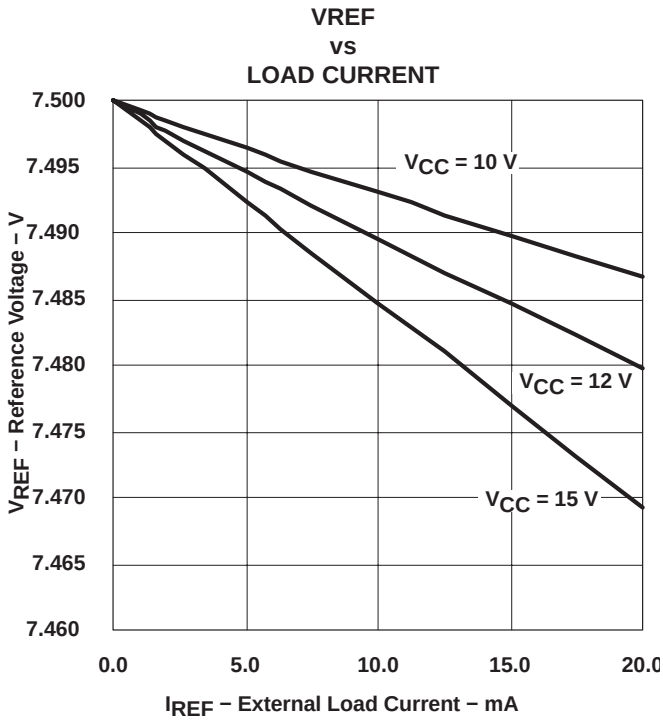


Figure 13

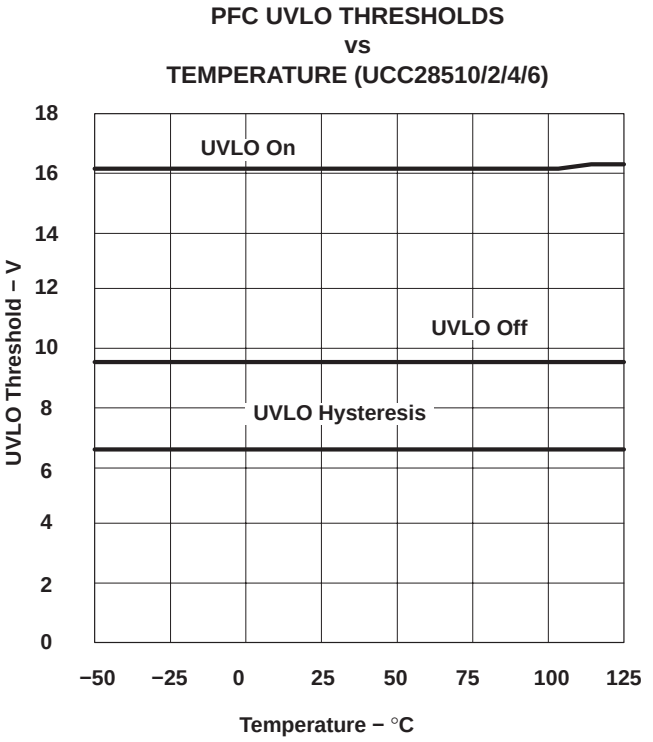


Figure 14

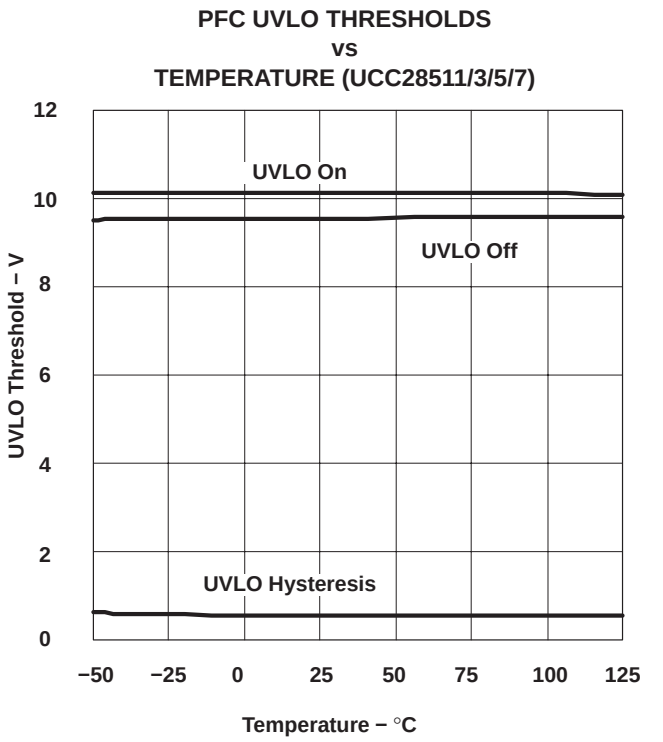


Figure 15

TYPICAL CHARACTERISTICS

PWM UVLO2 THRESHOLDS
vs
TEMPERATURE (UCC28510/1/4/5)

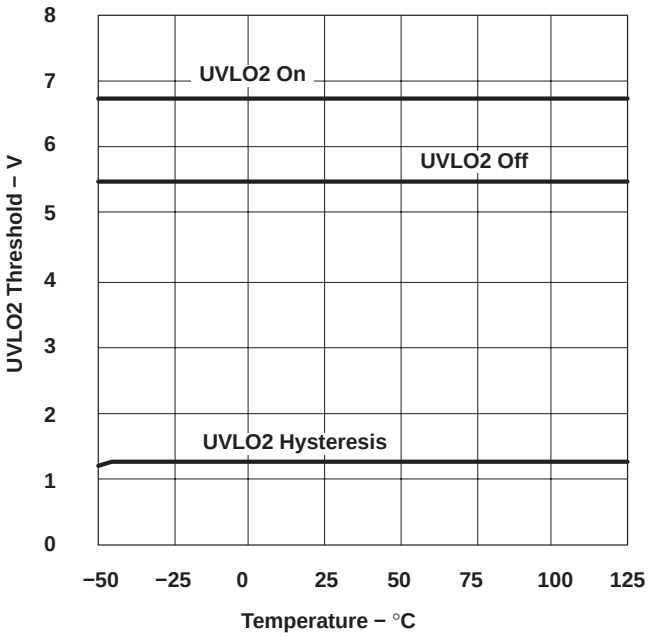


Figure 16

PWM UVLO2 THRESHOLDS
vs
TEMPERATURE (UCC28512/3/6/7)

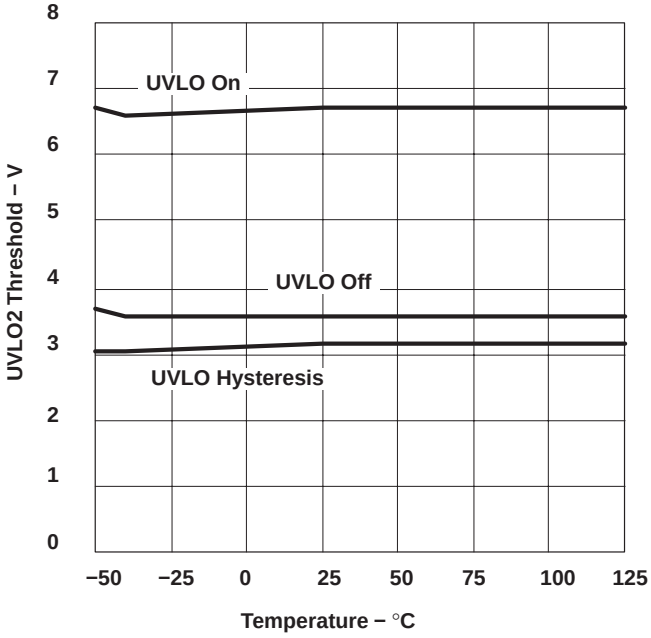


Figure 17

OSCILLATOR FREQUENCY
vs
RT

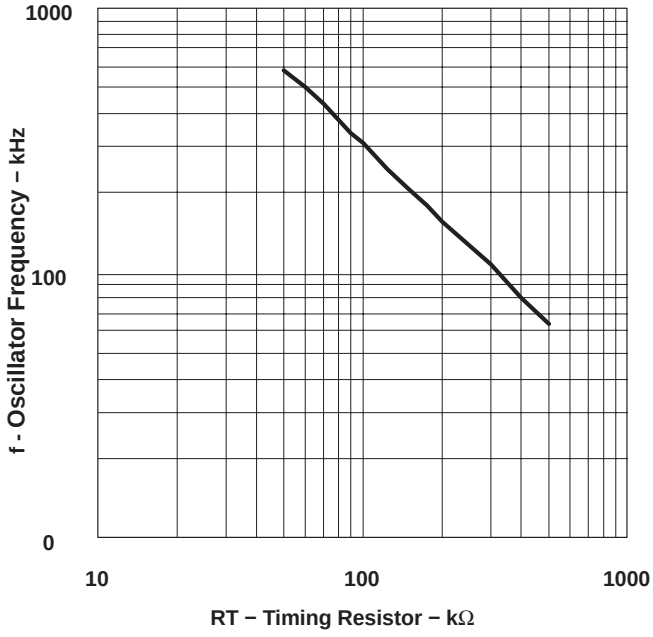


Figure 18

OSCILLATOR FREQUENCY
vs
RT OVER VCC (11 V TO 15 V) (−40°C TO 105°C)

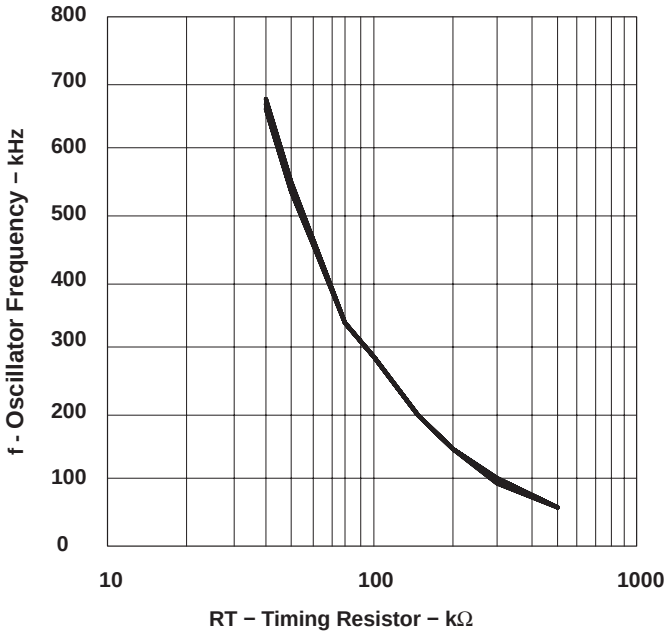


Figure 19

TYPICAL CHARACTERISTICS

GT1 MAXIMUM DUTY CYCLE vs PFC SWITCHING FREQUENCY (C_{AOUT} = 0.85 V)

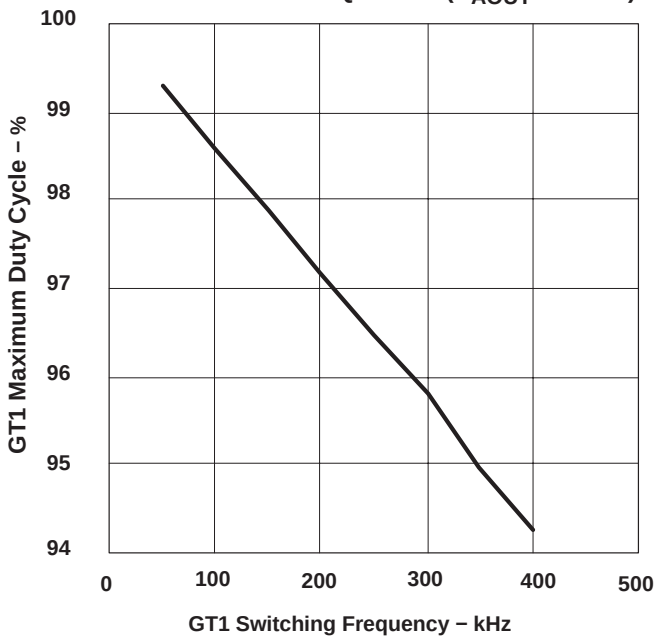


Figure 20

GT1, GT2 PULL-UP, PULL-DOWN RESISTANCE vs TEMPERATURE

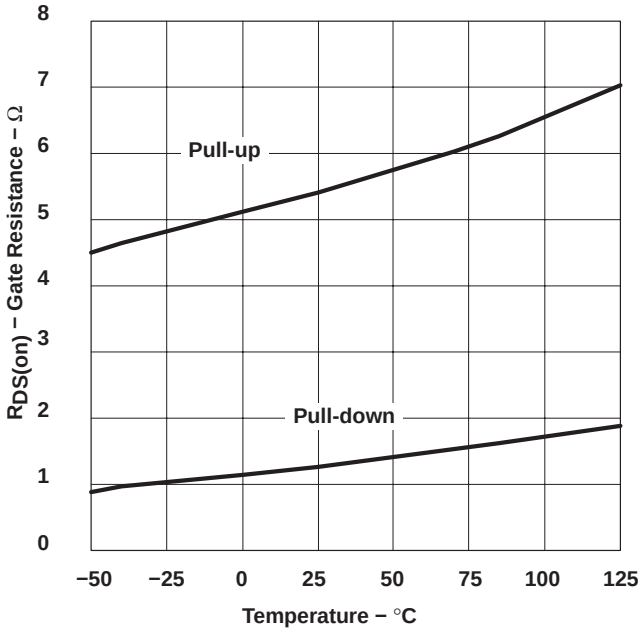


Figure 21

GT1 RISE/FALL TIME vs C_{LOAD} AND R_{SERIES} (V_{CC} = 12 V)

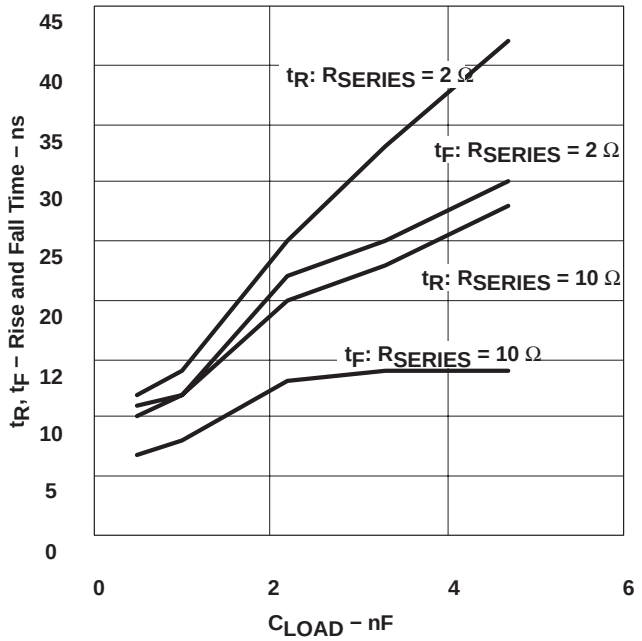


Figure 22

GT1, GT2 RISE AND FALL TIMES vs TEMPERATURE

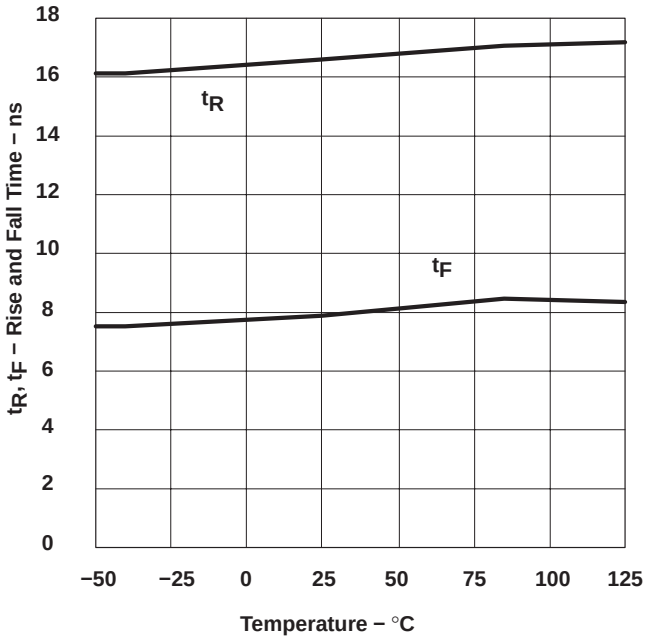


Figure 23

TYPICAL CHARACTERISTICS

GT2 MAXIMUM DUTY CYCLE vs D_MAX VOLTAGE

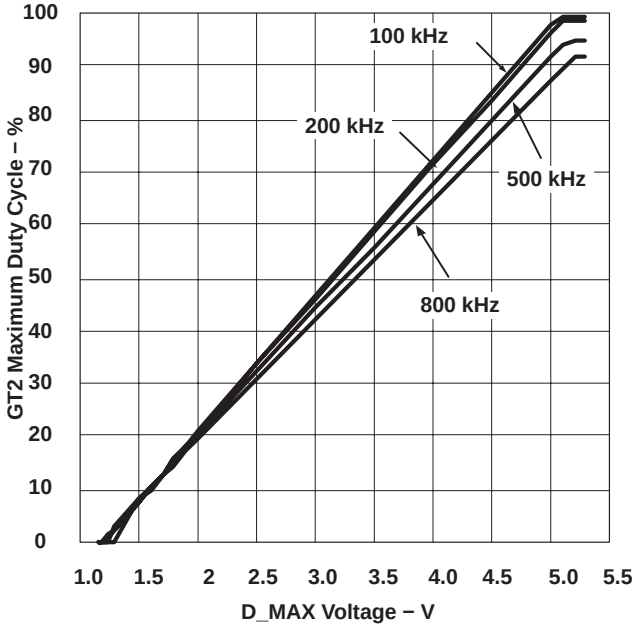


Figure 24

MULTIPLIER OUTPUT CURRENT vs VOLTAGE ERROR AMPLIFIER OUTPUT

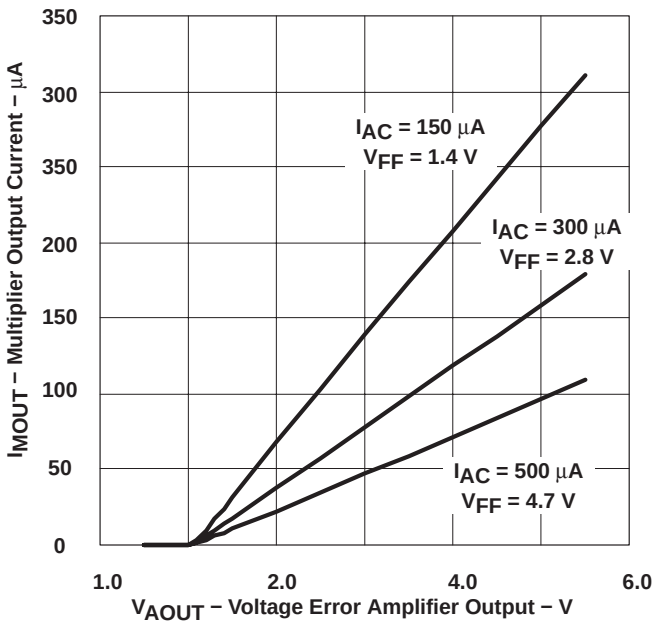


Figure 25

MULTIPLIER GAIN vs VOLTAGE ERROR AMPLIFIER OUTPUT

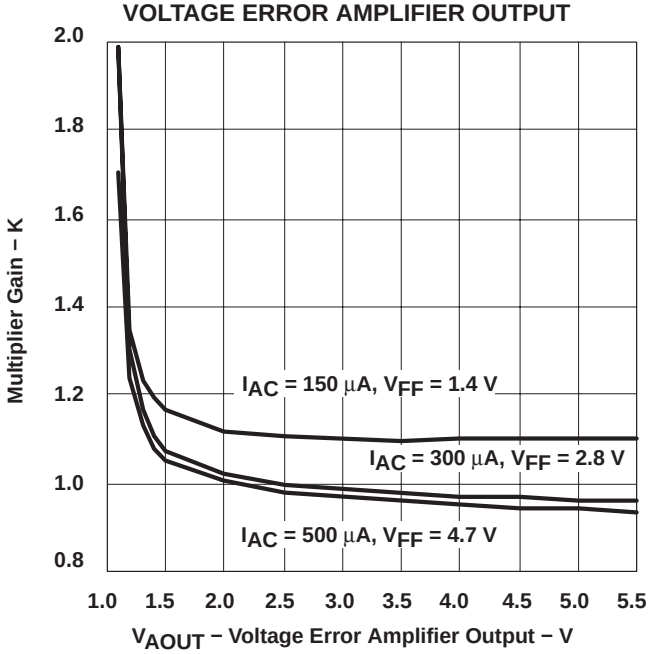


Figure 26

MULTIPLIER CONSTANT POWER PERFORMANCE

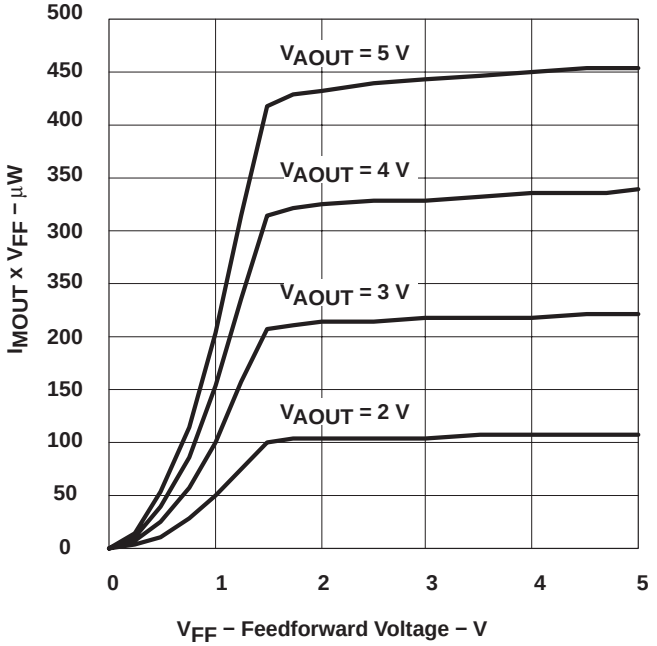


Figure 27

TYPICAL CHARACTERISTICS

CURRENT AMPLIFIER OPEN LOOP GAIN AND PHASE

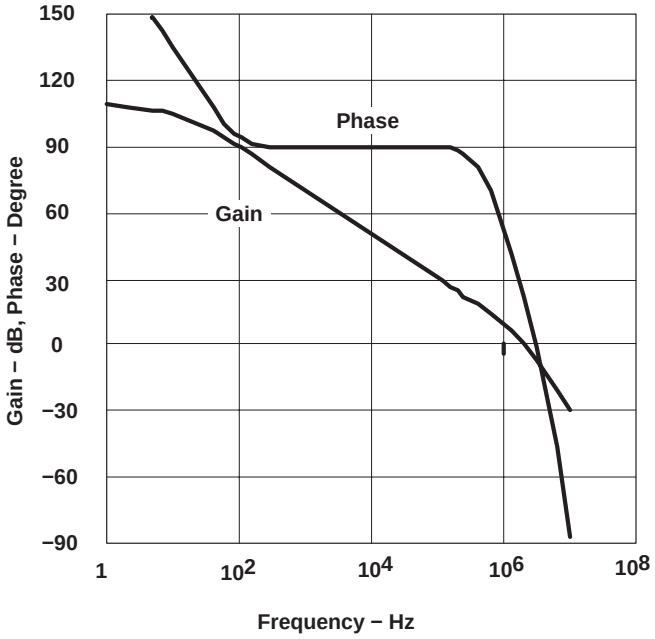


Figure 28

VOLTAGE AMPLIFIER TRANSCONDUCTANCE vs TEMPERATURE

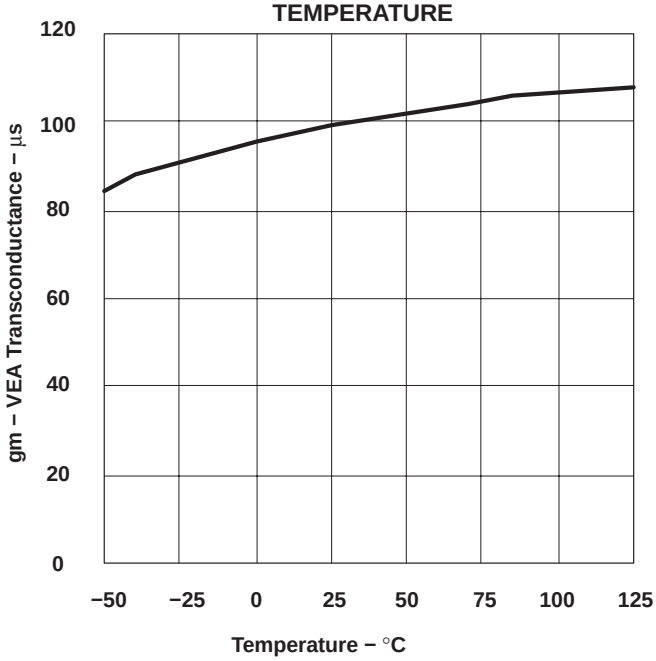


Figure 29

VOLTAGE AMPLIFIER OUTPUT CURRENT CAPABILITY

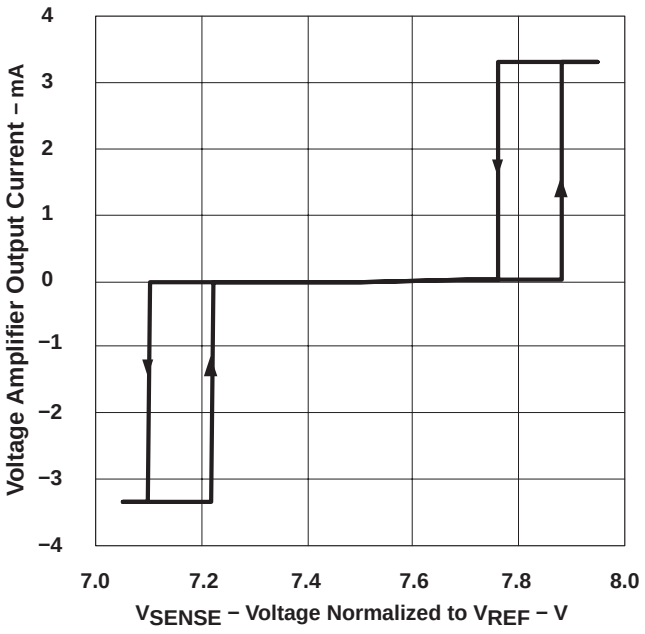


Figure 30

VOLTAGE AMPLIFIER OUTPUT CURRENT IN LINEAR REGION OF OPERATION

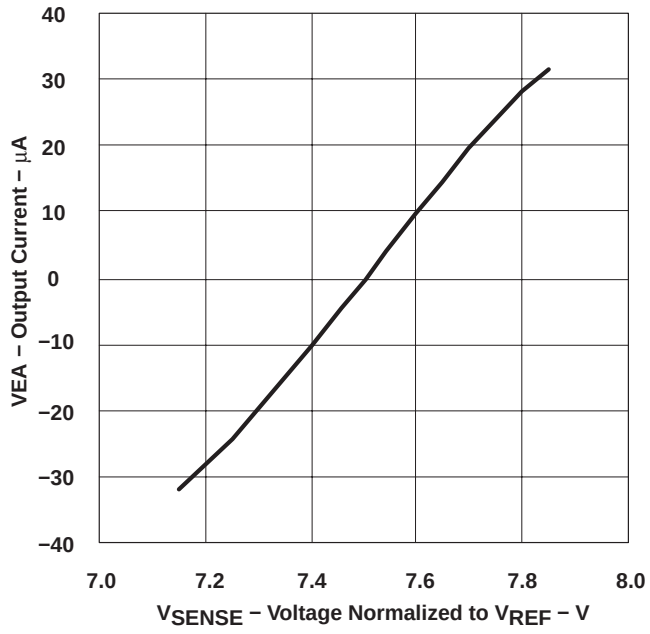


Figure 31

TYPICAL CHARACTERISTICS

**VOLTAGE AMPLIFIER
OPEN LOOP GAIN AND PHASE**

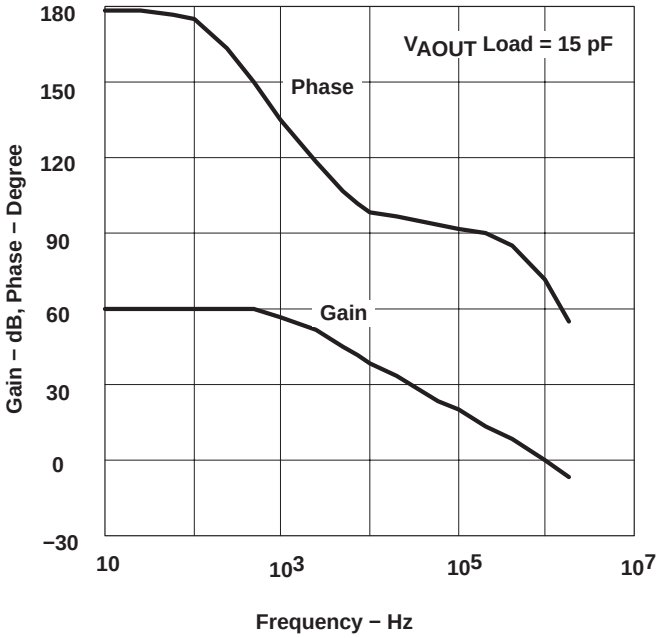


Figure 32

**VOLTAGE AMPLIFIER V_{SENSE} BIAS CURRENT
vs
TEMPERATURE**

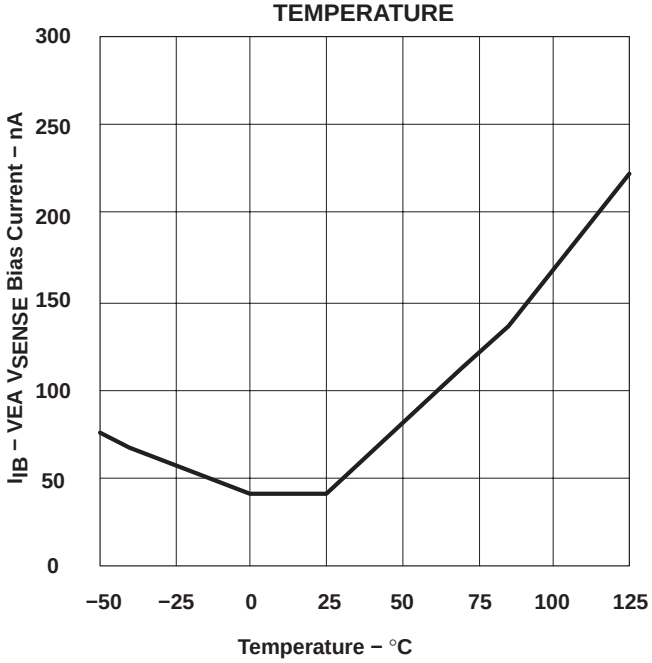


Figure 33

**VOLTAGE AMPLIFIER SLEW CURRENTS
vs
TEMPERATURE**

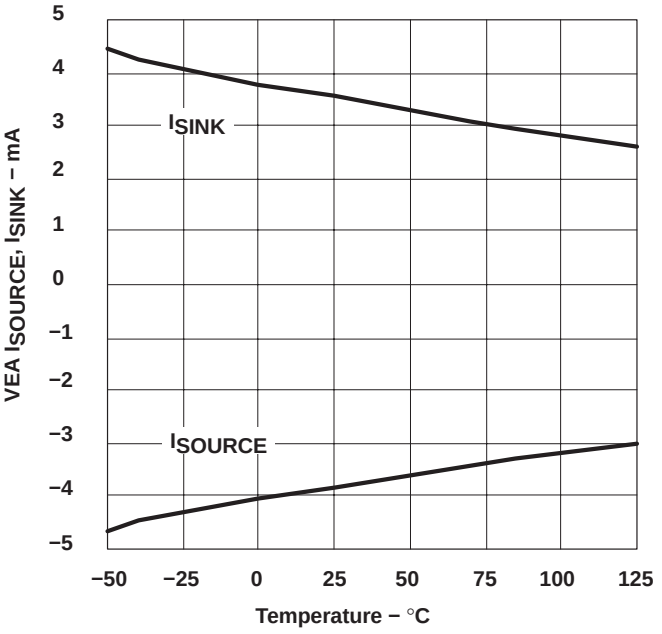


Figure 34

**SOFTSTART CURRENTS
vs
TEMPERATURE**

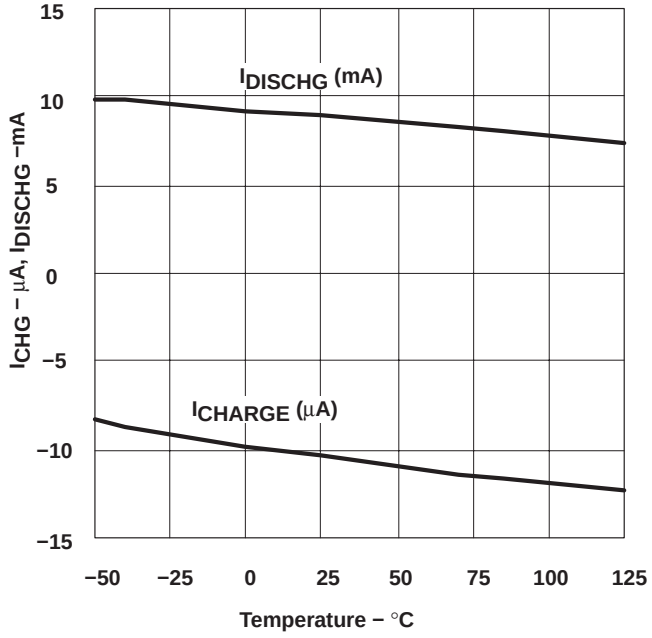


Figure 35

TYPICAL CHARACTERISTICS

**TYPICAL MINIMUM ON TIME
vs
CAPACITANCE**

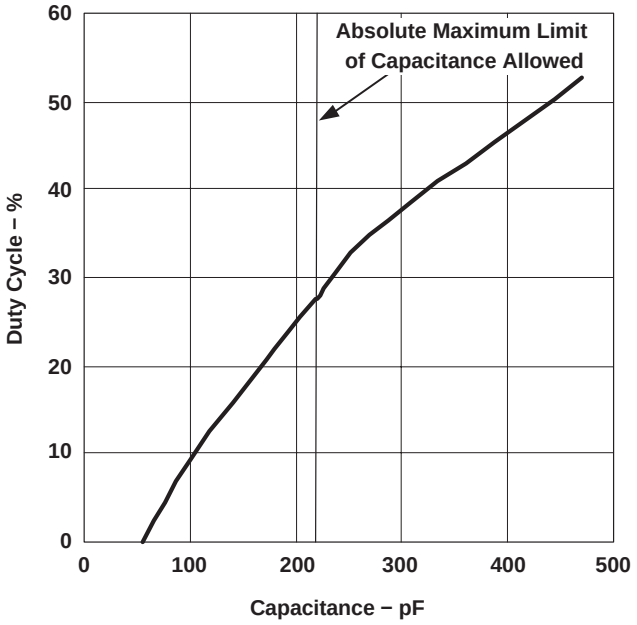


Figure 36

REFERENCES

1. Evaluation Module and associated User's Guide, UCC28517EVM, Texas Instruments Literature Number SLUS419C
2. Datasheet, *UCC38500/1/2/3 BiCMOS PFC/PWM Combination Controller*, Texas Instruments Literature Number SLUS419C
3. Power Supply Seminar SEM−600, *High Power Factor Preregulator for Off-line Power Supplies*, L.H. Dixon, Texas Instruments Literature Number SLUP087
4. Power Supply Seminar SEM−700, *Optimizing the Design of a High Power Factor Switching Preregulator*, L.H. Dixon, Texas Instruments Literature Number SLUP093
5. Power Supply Seminar SEM−1500 Topic 2, *Designing High-Power Factor Off−Line Power Supplies*, by James P. Noon
6. Application Note, *UC3854 Controlled Power Factor Correction Circuit Design* ,Texas Instruments Literature Number SLUA144
7. Design Note, *Optimizing Performance in UC3854 Power Factor Correction*, Texas Instruments Literature Number SLUA172
8. Design Note, *UC3854A and UC3854B Advanced Power Factor Correction Control ICs*, Texas Instruments Literature Number SLUA177
9. Design Note, *UC3854A/B and UC3855A/B Provide Power Limiting with Sinusoidal Input Current for PFC Front Ends*, Texas Instruments Literature Number SLUA196
10. Laszlo Balogh, *A Design and Application Guide for High Speed Power MOSFET Gate Drive Circuits*, 2001 Power Supply Design Seminar Manual SEM1400, 2001
11. Bob Mammano and Bruce Carsten, *Understanding and Optimizing Electromagnetic Compatibility in Switchmode Power Supplies*, 2002 Power Supply Design Seminar Manual SEM1500, 2002

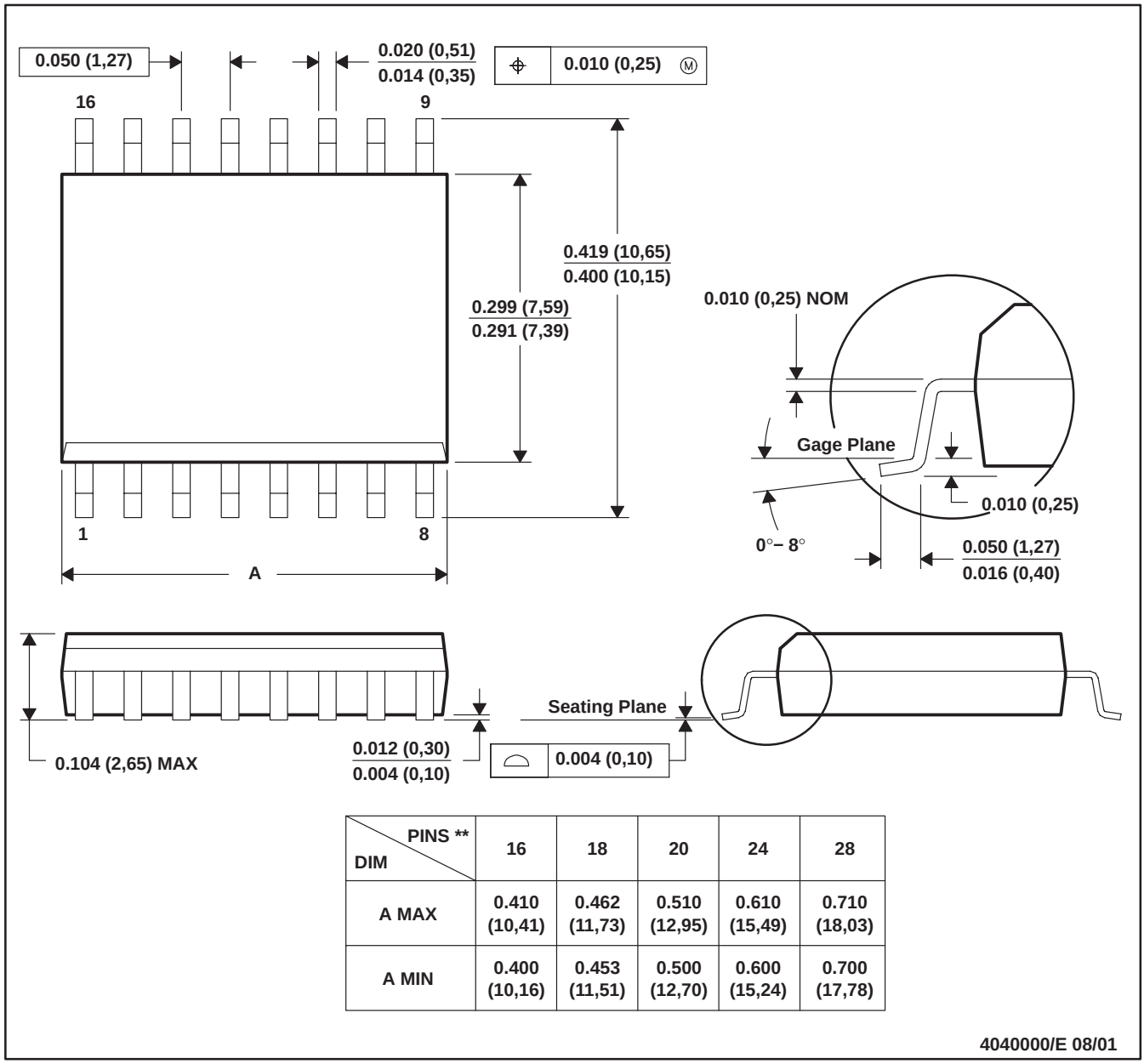
RELATED PRODUCTS

PART NUMBER	DESCRIPTION	COMMENTS
UCC38500/1/2/3	BiCMOS PFC/PWM combination controller	1:1 leading edge, trailing edge modulation, 50% PWM Max dc
UCC3817/18	BiCMOS power factor preregulator	High PF, UC3854 compatible, leading edge trailing edge modulation
UCC3819	Programmable output power factor preregulator	Tracking boost topology for dynamic output voltage adjustments
UC3854	High Power Factor Preregulator	High PF, industry standard PFC controller; 35 V_{CC} max
UC3854A/B	Enhanced high power factor preregulator	Improved high PF, industry standard PFC controller; 22 V_{CC} max
UC3855A/B	High performance power factor preregulator	ZVT output for lower EMI emission & higher efficiencies
UC3853	High power factor preregulator	8-Pin package; simplified architecture to minimized external components
UCC38050	Transition mode PFC controller	Constant on-time transition mode PFC controller
UC3852	High power factor preregulator	Constant off-time transition mode PFC controller; 30 V_{CC} max

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

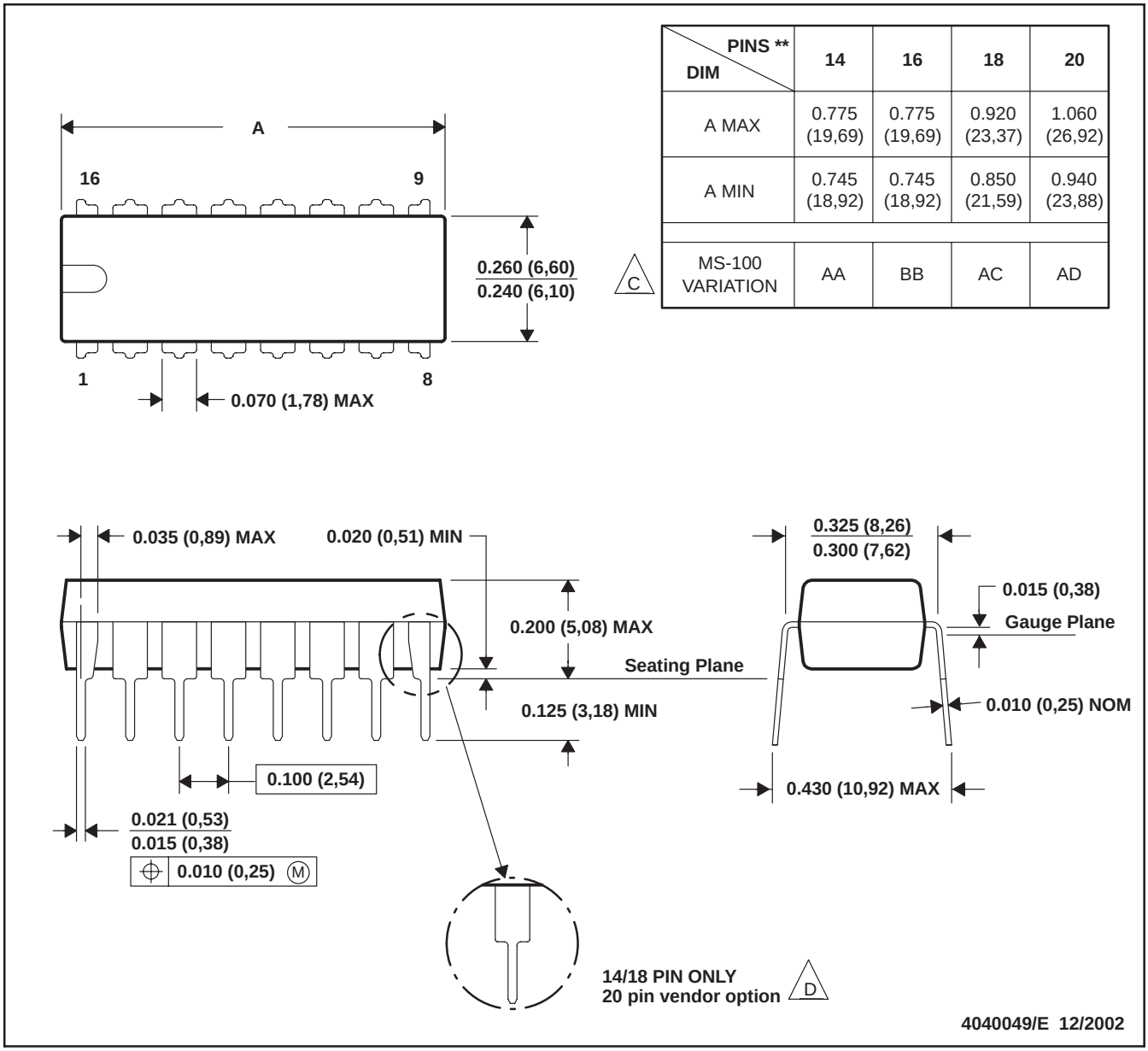
4040000/E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC28510DW	ACTIVE	SOIC	DW	20	25	TBD	CU NIPDAU	Level-1-220C-UNLIM
UCC28510DWR	ACTIVE	SOIC	DW	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
UCC28510N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA
UCC28510NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA
UCC28511DW	ACTIVE	SOIC	DW	20	25	TBD	CU NIPDAU	Level-1-220C-UNLIM
UCC28511DWR	ACTIVE	SOIC	DW	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
UCC28511N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA
UCC28511NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA
UCC28512DW	ACTIVE	SOIC	DW	20	25	TBD	CU NIPDAU	Level-1-220C-UNLIM
UCC28512DWR	ACTIVE	SOIC	DW	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
UCC28512N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA
UCC28512NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA
UCC28513DW	ACTIVE	SOIC	DW	20	25	TBD	CU NIPDAU	Level-1-220C-UNLIM
UCC28513DWR	ACTIVE	SOIC	DW	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
UCC28513N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA
UCC28513NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA
UCC28514DW	ACTIVE	SOIC	DW	20	25	TBD	CU NIPDAU	Level-1-220C-UNLIM
UCC28514DWR	ACTIVE	SOIC	DW	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
UCC28514N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA
UCC28514NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA
UCC28515DW	ACTIVE	SOIC	DW	20	25	TBD	CU NIPDAU	Level-1-220C-UNLIM
UCC28515DWR	ACTIVE	SOIC	DW	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
UCC28515N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA
UCC28515NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA
UCC28516DW	ACTIVE	SOIC	DW	20	25	TBD	CU NIPDAU	Level-1-220C-UNLIM
UCC28516DWR	ACTIVE	SOIC	DW	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
UCC28516N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA
UCC28516NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA
UCC28517DW	ACTIVE	SOIC	DW	20	25	TBD	CU NIPDAU	Level-1-220C-UNLIM
UCC28517DWR	ACTIVE	SOIC	DW	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
UCC28517N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA
UCC28517NE4	ACTIVE	PDIP	N	20	20	Pb-Free	CU NIPDAU	Level-NA-NA-NA

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
						(RoHS)		

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

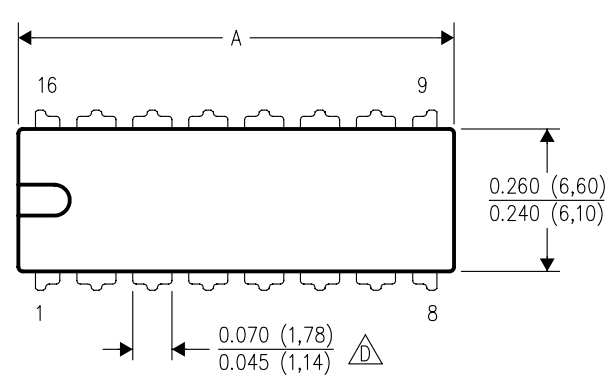
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

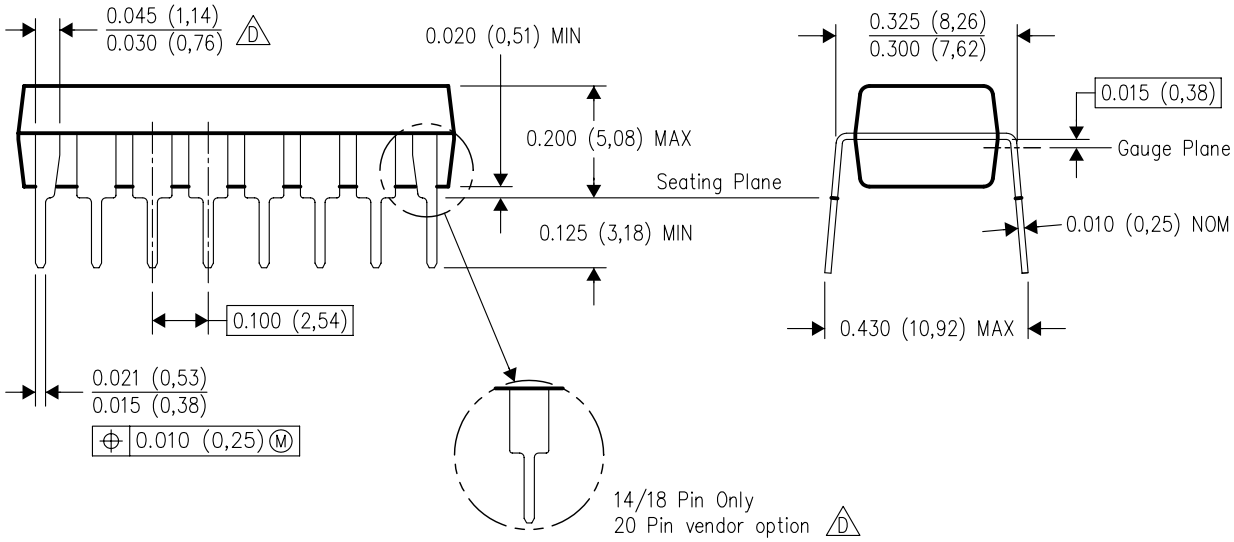
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



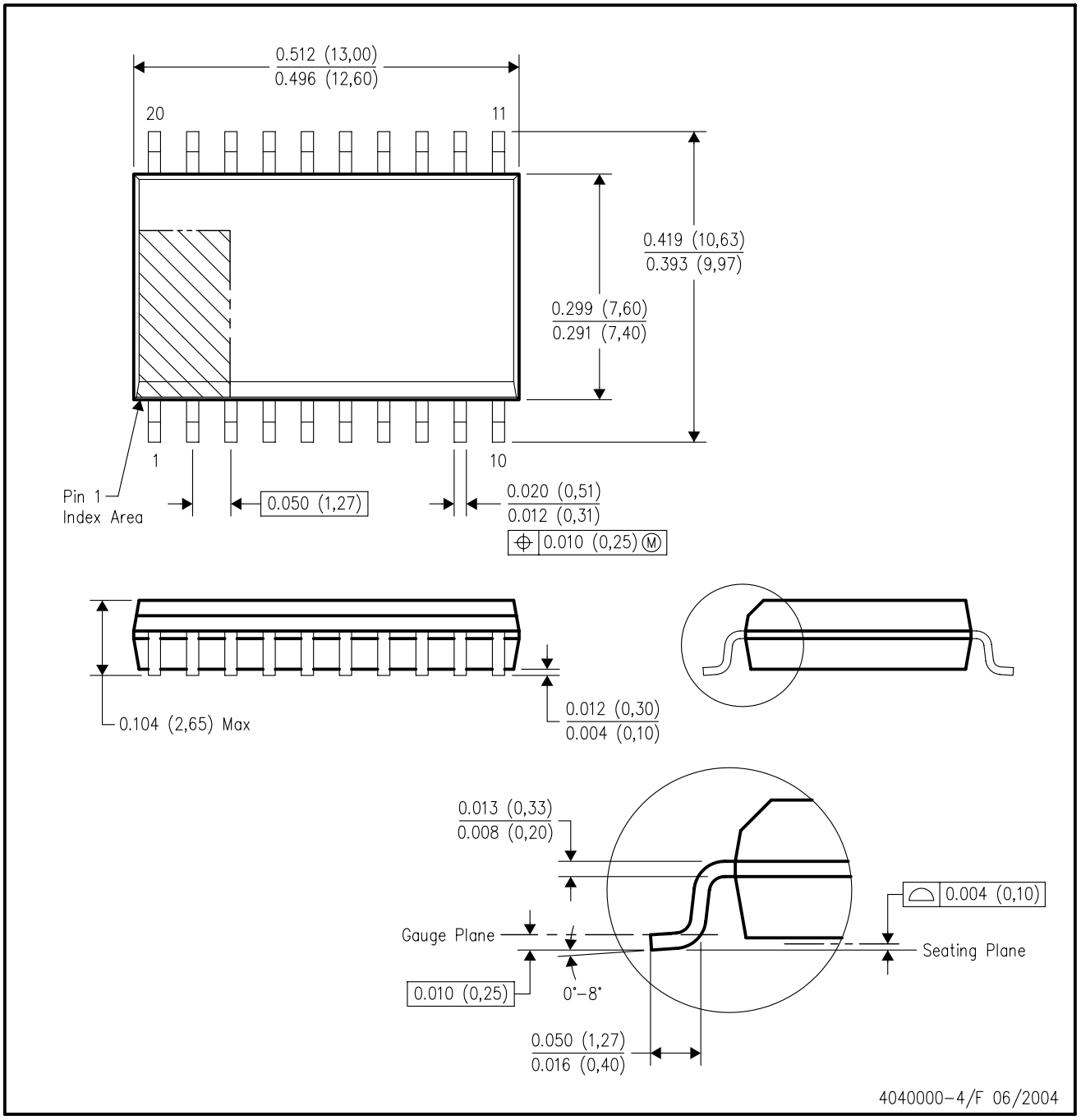
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

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