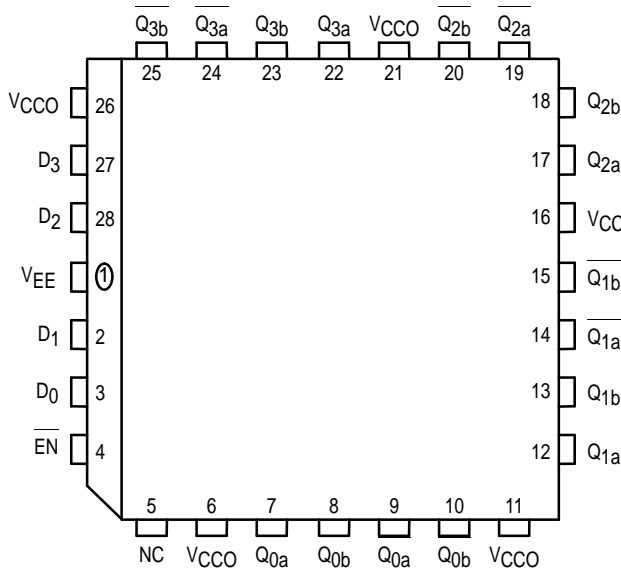


# Quad Driver

The MC10E100E112 is a quad driver with two pairs of OR/NOR outputs from each gate, and a common, buffered enable input. Using the data inputs the device can serve as an ECL memory address fan-out driver. Using just the enable input, the device serves as a clock driver, although the MC10E/100E111 is designed specifically for this purpose, and offers lower skew than the E112. For memory address driver applications where scan capabilities are required, please refer to the E212 device.

- 600ps Max. Propagation Delay
- Common Enable Input
- Extended 100E  $V_{EE}$  Range of  $-4.2V$  to  $-5.46V$
- $75k\Omega$  Input Pulldown Resistors

Pinout: 28-Lead PLCC (Top View)



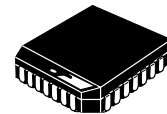
\* All VCC and VCCO pins are tied together on the die.

**PIN NAMES**

Pin	Function
$D_0 - D_3$	Data Inputs
$\overline{EN}$	Enable Input
$Q_{na}, Q_{nb}$	True Outputs
$\overline{Q_{na}}, \overline{Q_{nb}}$	Inverting Outputs

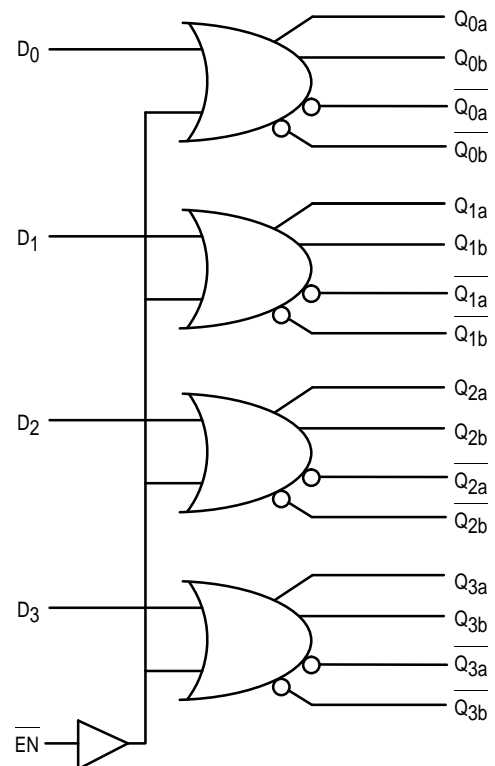
**MC10E112**  
**MC100E112**

**QUAD DRIVER**



**FN SUFFIX**  
PLASTIC PACKAGE  
CASE 776-02

**LOGIC DIAGRAM**



MC10E112 MC100E112

**DC CHARACTERISTICS** ( $V_{EE} = V_{EE}(\text{min})$  to  $V_{EE}(\text{max})$ ;  $V_{CC} = V_{CCO} = \text{GND}$ )

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
$I_{IH}$	Input HIGH Current			200			200			200	$\mu\text{A}$	
	$\frac{D}{EN}$			200			200			200		
$I_{EE}$	Power Supply Current										mA	
	10E		47	56		47	56		47	56		
	100E		47	56		47	56		54	65		

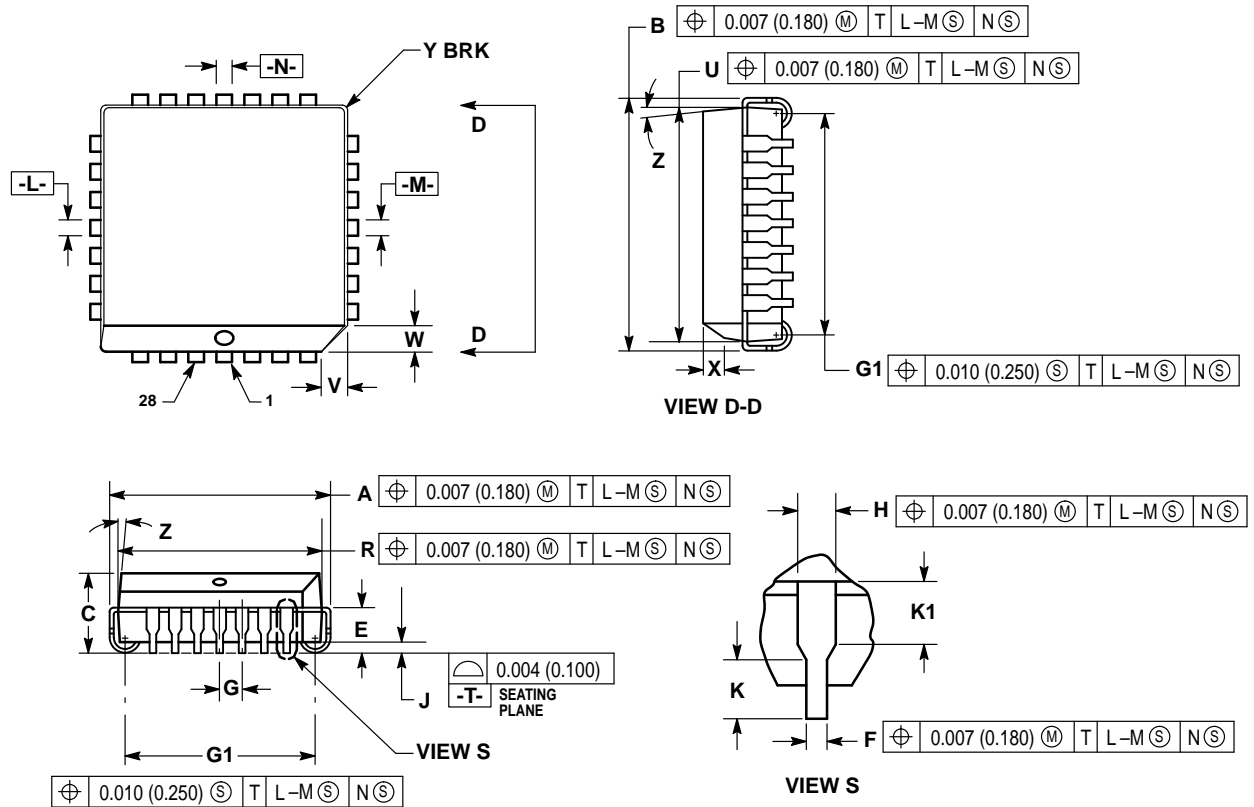
**AC CHARACTERISTICS** ( $V_{EE} = V_{EE}(\text{min})$  to  $V_{EE}(\text{max})$ ;  $V_{CC} = V_{CCO} = \text{GND}$ )

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output										ps	
	$\frac{D}{EN}$	200	400	600	200	400	600	200	400	600		
$t_{SKEW}$	Within-Device Skew										ps	1 2
	Dn to Qn, Qn		80			80			80			
	Qna to Qnb		40			40			40			
$t_r$ $t_f$	Rise/Fall Times 20 - 80%	275	425	700	275	425	700	275	425	700	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Skew defined between common OR or common NOR outputs of a single gate.

OUTLINE DIMENSIONS


FN SUFFIX  
 PLASTIC PLCC PACKAGE  
 CASE 776-02  
 ISSUE D



NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°		10°	
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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