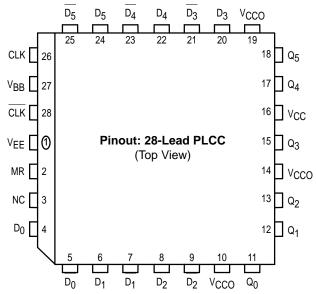
# 6-Bit D Register Differential Data and Clock

The MC10E/100E451 contains six D-type flip-flops with single-ended outputs and differential data inputs. The common clock input is also differential. The registers are triggered by a positive transition of the positive clock (CLK) input.

A HIGH on the Master Reset (MR) input resets all Q outputs to LOW. The V<sub>BB</sub> output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using for this purpose, it is recommended that V<sub>BB</sub> is decoupled to V<sub>CC</sub> via a 0.01 $\mu$ F capacitor.

The differential input structures are clamped so that the inputs of unused registers can be left open without upsetting the bias network of the device. The clamping action will assert the D and the CLK sides of the inputs. Because of the edge triggered flip-flop nature of the device simultaneously opening both the clock and data inputs will result in an output which reaches an unidentified but valid state. Note that the input clamps only operate when both inputs fall to 2.5V below V<sub>CC</sub>.

- Differential Inputs: Data and Clock
- VBB Output
- 1100MHz Min. Toggle Frequency
- Asynchronous Master Reset
- Extended 100E VEE Range of 4.2V to 5.46V
- 75kΩ Input Pulldown Resistors



 $^{\ast}$  All V\_CC and V\_CCO pins are tied together on the die.

**PIN NAMEŠ** 

Pin	Function
$\underline{D}_0 - \underline{D}_5$	+Data Input
$D_0 - D_5$	– Data Input
CLK	+Clock Input
CLK	<ul> <li>Clock Input</li> </ul>
MR	Master Reset Input
VBB	V <sub>BB</sub> Output
$Q_0 - Q_5$	Data Outputs

#### 12/93

## MC10E451 MC100E451 6-BIT D REGISTER DIFFERENTIAL DATA AND CLOCK **FN SUFFIX** PLASTIC PACKAGE CASE 776-02 LOGIC DIAGRAM <u>D</u>0 Q<sub>0</sub> D $D_0$ R <u>D</u>1 D Q1 D1 R $D_2$ Q2 D D<sub>2</sub> R <u>D</u>3 Q3 D D٦ R <u>D</u>4 Q4 D D₄ R $D_5$ Q5 D $D_5$ R CLK CI K



OTOROLA

MR Vod

## **DC CHARACTERISTICS** ( $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$ ; $V_{CC} = V_{CCO} = GND$ )

		O°C		25°C			85°C					
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
V <sub>BB</sub>	Output Reference Voltage										V	
	10E	-1.3 8		-1.2 7	-1.3 5		-1.2 5	-1.3 1		-1.1 9		
	100E	-1.3 8		-1.2 6	-1.3 8		-1.2 6	-1.3 8		-1.2 6		
Iн	Input HIGH Current			150			150			150	μΑ	
IEE	Power Supply Current 10E 100E		84 84	101 101		84 84	101 101		84 97	101 116	mA	
VCMR	Common Mode Range	- 2.0		- 0.4	- 2.0		- 0.4	- 2.0		- 0.4	V	2

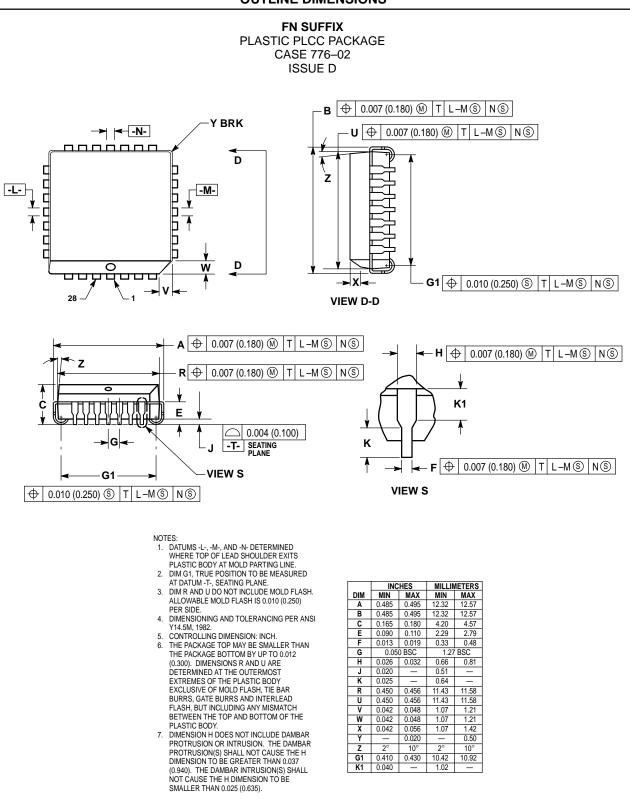
 V<sub>CMR</sub> is referenced to the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V<sub>CMR</sub> range and the input swing is greater than V<sub>PP MIN</sub> and < 1.0V.</li>

### **AC CHARACTERISTICS** (VEE = VEE(min) to VEE(max); VCC = VCCO = GND)

		0°C			25°C			85°C				
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
fMAX	Max, Toggle Frequency	1100	1400		1100	1400		1100	1400		MHz	
<sup>t</sup> PLH <sup>t</sup> PHL	Propagation Delay to Output CLK (Diff) CLK (SE) MR	475 425 425	650 650 600	800 850 850	475 425 425	650 650 600	800 850 850	475 425 425	650 650 600	800 850 850	ps	
t <sub>s</sub>	Setup Time D	150	-100		150	-100		150	-100		ps	
th	Hold Time D	250	100		250	100		250	100		ps	
V <sub>PP</sub> (AC)	Minimum Input Swing	150			150			159			mV	1
<sup>t</sup> RR	Reset Recovery Time	750	600		750	600		750	600		ps	
<sup>t</sup> PW	Minimum Pulse Width CLK, MR	400			400			400			ps	
<sup>t</sup> SKEW	Within-Device Skew		100			100			100		ps	2
t <sub>r</sub> t <sub>f</sub>	Rise/Fall Times 20 - 80%	275	450	800	275	450	800	275	450	800	ps	

1. Minimum input voltage for which AC parameters are guaranteed.

2. Within-device skew is defined as identical transitions on similar paths through a device.



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