

## 2-Input Differential AND/NAND

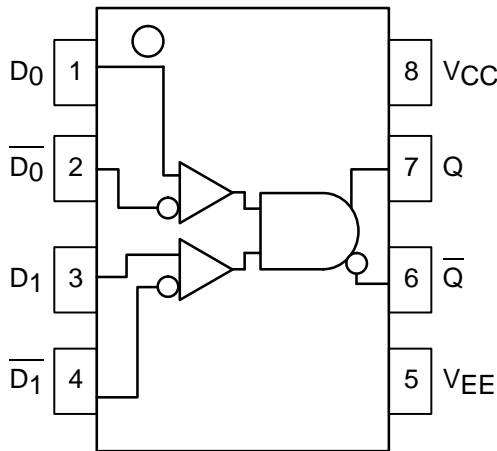
The MC10EL/100EL05 is a 2-input differential AND/NAND gate. The device is functionally equivalent to the E404 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E404 the EL05 is ideally suited for those applications which require the ultimate in AC performance.

Because a negative 2-input NAND is equivalent to a 2-input OR function, the differential inputs and outputs of the device allows the EL05 to also be used as a 2-input differential OR/NOR gate.

The differential inputs employ clamp circuitry so that under open input conditions (pulled down to  $V_{EE}$ ) the input to the AND gate will be HIGH. In this way, if one set of inputs is open, the gate will remain active to the other input.

- 275ps Propagation Delay
- High Bandwidth Output Transitions
- 75k $\Omega$  Internal Input Pulldown Resistors
- >1000V ESD Protection

### LOGIC DIAGRAM AND PINOUT ASSIGNMENT



## MC10EL05 MC100EL05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

### PIN DESCRIPTION

PIN	FUNCTION
D0, D1 Q	Data Inputs Data Outputs



# MC10EL05 MC100EL05

## DC CHARACTERISTICS ( $V_{EE} = V_{EE(\min)}$ to $V_{EE(\max)}$ ; $V_{CC} = \text{GND}$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current 10EL 100EL		18 18	22 22		18 18	22 22		18 18	22 22		18 21	22 25	mA
$V_{EE}$	Power Supply Voltage 10EL 100EL	-4.75 -4.20	-5.2 -4.5	-5.5 -5.5	-4.75 -4.20	-5.2 -4.5	-5.5 -5.5	-4.75 -4.20	-5.2 -4.5	-5.5 -5.5	-4.75 -4.20	-5.2 -4.5	-5.5 -5.5	V
$I_{IH}$	Input HIGH Current			150			150			150			150	$\mu\text{A}$

## AC CHARACTERISTICS ( $V_{EE} = V_{EE(\min)}$ to $V_{EE(\max)}$ ; $V_{CC} = \text{GND}$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output	135	260	440	185	275	390	185	275	390	215	305	420	ps
$V_{PP}$	Minimum Input Swing <sup>1</sup>	150			150			150			150			mV
$V_{CMR}$	Common Mode Range <sup>2</sup>	-0.4		See <sup>2</sup>	-0.4		See <sup>2</sup>	-0.4		See <sup>2</sup>	-0.4		See <sup>2</sup>	V
$t_r$ $t_f$	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	100	225	350	ps

1. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of  $\approx 40$ .

2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PP(\min)}$  and 1V. The lower end of the CMR range is dependent on  $V_{EE}$  and is equal to  $V_{EE} + 3.0\text{V}$ .

OUTLINE DIMENSIONS

D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751-05  
ISSUE P



NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. DIMENSIONS ARE IN MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
6. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.35	0.49
F	0.40	1.25
G	1.27 BSC	
J	0.18	0.25
K	0.10	0.25
M	0°	7°
P	5.80	6.20
R	0.25	0.50

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