

Structure Silicon monolithic integrated circuit

Product series 1ch switching regulator controller

Type **BD9850FVM**

- Functions
- Build-in under voltage lock out circuit
 - High accuracy reference voltage ($2.5V \pm 1.0\%$)
 - .CTL/SS terminal for both stand-by and soft-start function
(Soft-start time can be set by external capacitor)
 - MSOP8 thin and small package

○Absolute Maximum Ratings(Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	VCC	10	V
Storage temperature range	Tsig	-55~+150	°C
Power dissipation	Pd	587* ¹	mW
Junction temperature	Tjmax	+150	°C

*¹ Reduced by 4.7mW for each increase in Ta of 1°C over 25°C. 70X70X1.6mm in foundations mounting.

○Recommended Operating Conditions (Ta=-25~75°C)

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply voltage	VCC	4	7	9	V
Oscillating frequency	fosc	100	—	2000	kHz
Operating temperature range	Topr	-40	—	+85	°C

Status of this document

The Japanese version of this document is the official specification.

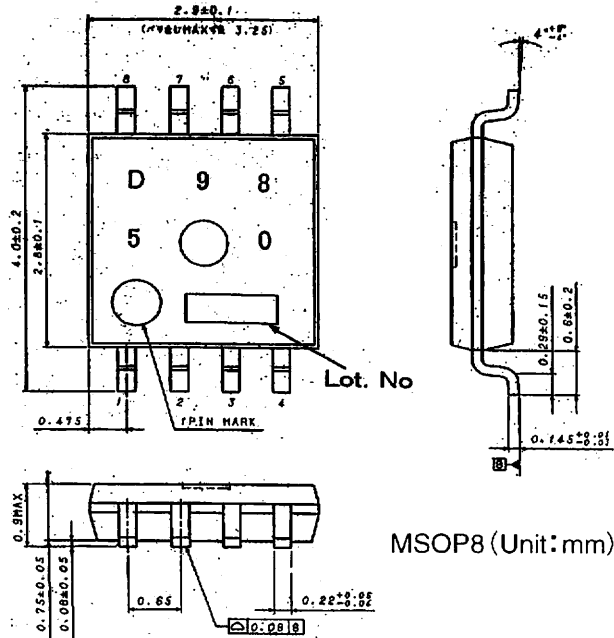
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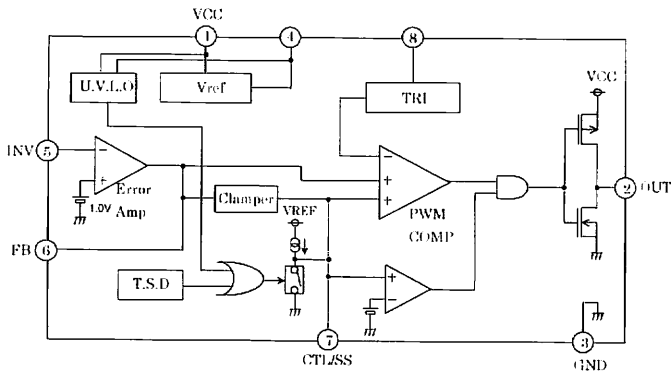
○ Electrical characteristics (Unless otherwise specified, Ta=25°C, Vcc=7V, fosc=600KHz)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
【Oscillator】						
Oscillating frequency	fosc	510	600	690	KHz	RRT=24kΩ
Frequency tolerance	FDV	-5	0	5	%	Vcc=4~9V
Swing voltage	Vpptr	—	0.5	—	V	
【Stand-by, Soft start】						
CTL/SS pin source current	ISS	-1.90	-1.00	-0.55	μA	VCTL/SS=1.5V
CTL/SS pin clamp voltage	VSS	2.2	2.4	2.6	V	
CTL threshold voltage	VCTLTH	1.2	1.3	1.4	V	
【PWM comparator】						
0%threshold voltage	D0	1.5	1.6	1.7	V	fosc=600KHz
100%threshold voltage	D100	2.0	2.1	2.2	V	fosc=600KHz
【Error amplifier】						
Threshold voltage	VIN	0.98	1.00	1.02	V	
Band width	BW	1.5	3.0	—	MHz	AV=0dB
Voltage gain	Av	—	70	—	dB	
Input bias current	IIB	-150	-70	—	nA	
Maximum output voltage	VCH	2.3	2.4	2.6	V	
Minimum output voltage	VCL	—	0.03	0.20	V	
Output source current	IOI	-3.1	-1.6	-1.0	mA	VFB=1.0V
Output sink current	IOO	12	50	125	mA	VFB=1.0V
【Reference voltage】						
Output voltage	VREF	2.475	2.500	2.525	V	IVREF=0mA
Load regulation	ΔVREFlo	-	-	10	mV	IVREF=0~-1mA
Output short current	IVREF	-45	-16	-1	mA	
【Whole device】						
Stand-by current	ICCS	420	610	960	μA	
Circuit current	ICCA	3.4	5.0	7.8	mA	No load
【Output】						
ON resistance	RON	0.9	2.5	8.0	Ω	
Output rise/fall time	Tr/Tf	—	20	—	nsec	Cout=1000pF
【Under voltage lock out】						
Threshold voltage	VUT	3.7	3.8	3.9	V	Vcc sweep down
Hysteresis width	VUThy	0.05	0.10	0.15	V	

○ Package Dimensions



○ Block diagram



○ Pin description

Pin No.	Pin name	Function
1	VCC	Power supply
2	OUT	FET driver output
3	GND	Ground
4	VREF	Reference voltage (2.5V ± 1%) output
5	INV	Inverting input of error amplifier
6	FB	Output of error amplifier
7	CTL/SS	Stand-by switch/ Soft start capacitor connecting pin
8	RT	Timing resistor connecting pin

○ Operation Notes

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC deterioration or damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions. In addition, ensure that no pins other than the GND pin carry a voltage lower than or equal to the GND pin, including during actual transient phenomena.

3) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Inter-pin shorts and mounting errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pin caused by the presence of a foreign object may result in damage to the IC.

5) Operation in a strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6) Thermal shutdown circuit (TSD circuit)

This IC incorporates a built-in thermal shutdown circuit (TSD circuit). The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of the thermal shutdown circuit is assumed.

7) Testing on application boards

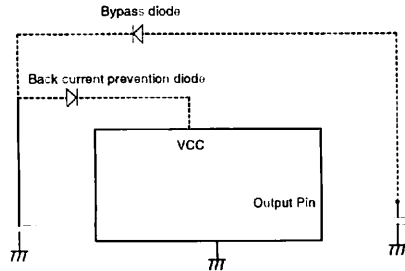
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

8) Common impedance

Power supply and ground wiring should reflect consideration of the need to lower common impedance and minimize ripple as much as possible (by making wiring as short and thick as possible or rejecting ripple by incorporating inductance and capacitance).

9) Applications with modes that reverse VCC and pin potentials may cause damage to internal IC circuits.

For example, such damage might occur when VCC is shorted with the GND pin while an external capacitor is charged. It is recommended to insert a diode for preventing back current flow in series with VCC or bypass diodes between VCC and each pin.



10) Timing resistor

Timing resistor connected between RT and GND, has to be placed near RT terminal (2pin). And pattern has to be short enough.

11) IC pin input

This monolithic IC contains P+ isolation and PCB layers between adjacent elements in order to keep them isolated.

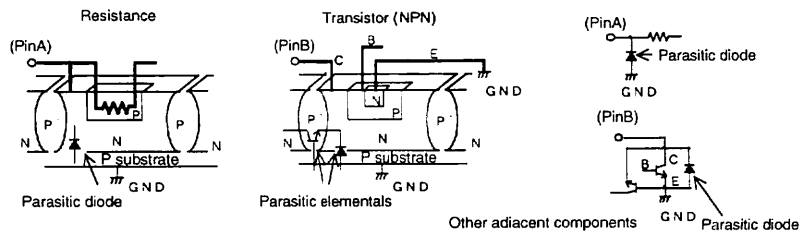
P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, when a resistor and transistor are connected to pins as shown in following chart.

○ The P/N junction functions as a parasitic diode when GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).

○ Similarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (PCB) voltage to input and output pins.



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