

# 9-Bit Latch TTL/ECL Translator

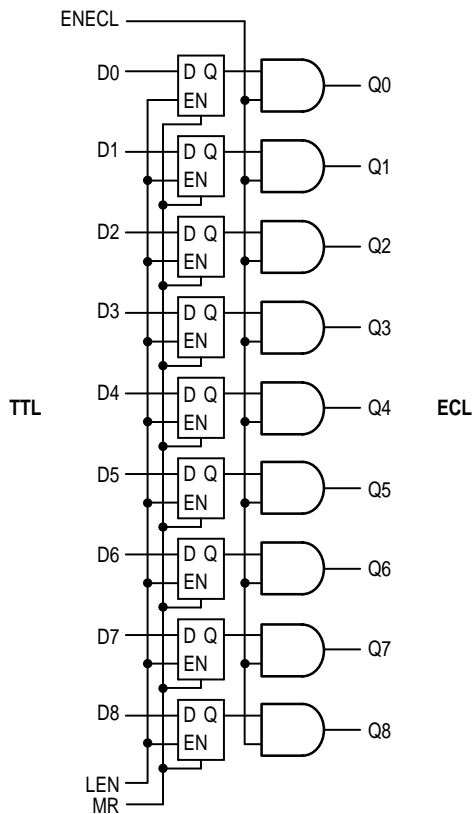
The MC10H/100H602 is a 9-bit, dual supply TTL to ECL translator with latch. Devices in the Motorola 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

The H602 features D-type latches. Latching is controlled by Latch Enable (LEN), while the Master Reset input resets the latches. A post-latch logic enable is also provided (ENECL), allowing control of the output state without destroying latch data. All control inputs are ECL level.

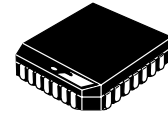
The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

- 9-Bit Ideal for Byte-Parity Applications
- Flow-Through Configuration
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- 3.5 ns Max D to Q
- PNP TTL Inputs for Low Loading

### LOGIC SYMBOL



## MC10H602 MC100H602



**FN SUFFIX**  
PLASTIC PACKAGE  
CASE 776-02

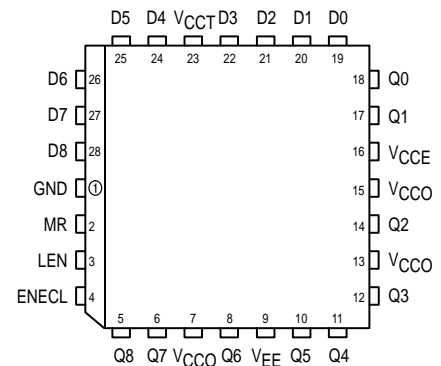
### PIN NAMES

PIN	FUNCTION
GND	TTL Ground (0 V)
V <sub>CCE</sub>	ECL V <sub>CC</sub> (0 V)
V <sub>CCO</sub>	ECL V <sub>CC</sub> (0 V) — Outputs
V <sub>CCT</sub>	TTL Supply (+5.0 V)
V <sub>EE</sub>	ECL Supply (-5.2/-4.5 V)
D0-D8	Data Inputs (TTL)
Q0-Q8	Data Outputs (ECL)
ENECL	Enable Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

### TRUTH TABLE

D	LEN	MR	ENECL	Q
L	L	L	H	L
H	L	L	H	H
X	H	L	H	Q <sub>0</sub>
X	X	H	H	L
X	X	X	L	L

### Pinout: 28-Lead PLCC (Top View)



MC10H602 MC100H602

**DC CHARACTERISTICS:**  $V_{CCT} = 5.0\text{ V} \pm 10\%$ ;  $V_{EE} = -5.2\text{ V} \pm 5\%$  (10H version);  $V_{EE} = -4.2\text{ V}$  to  $-5.5\text{ V}$  (100H version)

Symbol	Parameter		0°C		25°C		75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
	Power Supply Current									
$I_{EE}$	ECL	10H 100H		-125 -122		-125 -123		-125 -132	mA	
$I_{CCH}$ $I_{CCL}$	TTL			48 50		48 50		48 50	mA	

**AC CHARACTERISTICS:**  $V_{CCT} = 5.0\text{ V} \pm 10\%$ ;  $V_{EE} = -5.2\text{ V} \pm 5\%$  (10H version);  $V_{EE} = -4.2\text{ V}$  to  $-5.5\text{ V}$  (100H version)

Symbol	Parameter		0°C		25°C		75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output	D	1.4	3.0	1.5	3.2	1.7	3.5	ns	
		LEN	2.0	3.4	2.1	3.5	2.4	3.7		
		MR	2.0	3.4	2.1	3.5	2.5	3.9		
		ENECL	1.6	3.2	1.7	3.3	1.8	3.7		
$t_s$	Set-Up Time, D to LEN		2.0		2.0		2.0		ns	
$t_h$	Hold Time, D to LEN		1.0		1.0		1.0		ns	
$t_{w(L)}$	LEN Pulse Width, LOW		2.0		2.0		2.0		ns	
$t_R$ $t_F$	Output Rise/Fall Time 20%–80%		0.5	1.5	0.5	1.5	0.5	1.5	ns	

**10H ECL DC CHARACTERISTICS:**  $V_{CCT} = 5.0\text{ V} \pm 10\%$ ;  $V_{EE} = -5.2\text{ V} \pm 5\%$

Symbol	Parameter		0°C		25°C		75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
$I_{IH}$ $I_{IL}$	Input HIGH Current Input LOW Current		0.5	225	0.5	145	0.5	145	$\mu\text{A}$ $\mu\text{A}$	
$V_{IH}$ $V_{IL}$	Input HIGH Voltage Input LOW Voltage		-1170 -1950	-840 -1480	-1130 -1950	-810 -1480	-1070 -1950	-735 -1450	mV	
$V_{OH}$ $V_{OL}$	Output HIGH Voltage Output LOW Voltage		-1020 -1950	-840 -1630	-980 -1950	-810 -1630	-920 -1950	-735 -1600	mV	50 $\Omega$ to -2.0 V

**100H ECL DC CHARACTERISTICS:**  $V_{CCT} = 5.0\text{ V} \pm 10\%$ ;  $V_{EE} = -4.2\text{ V}$  to  $-5.5\text{ V}$

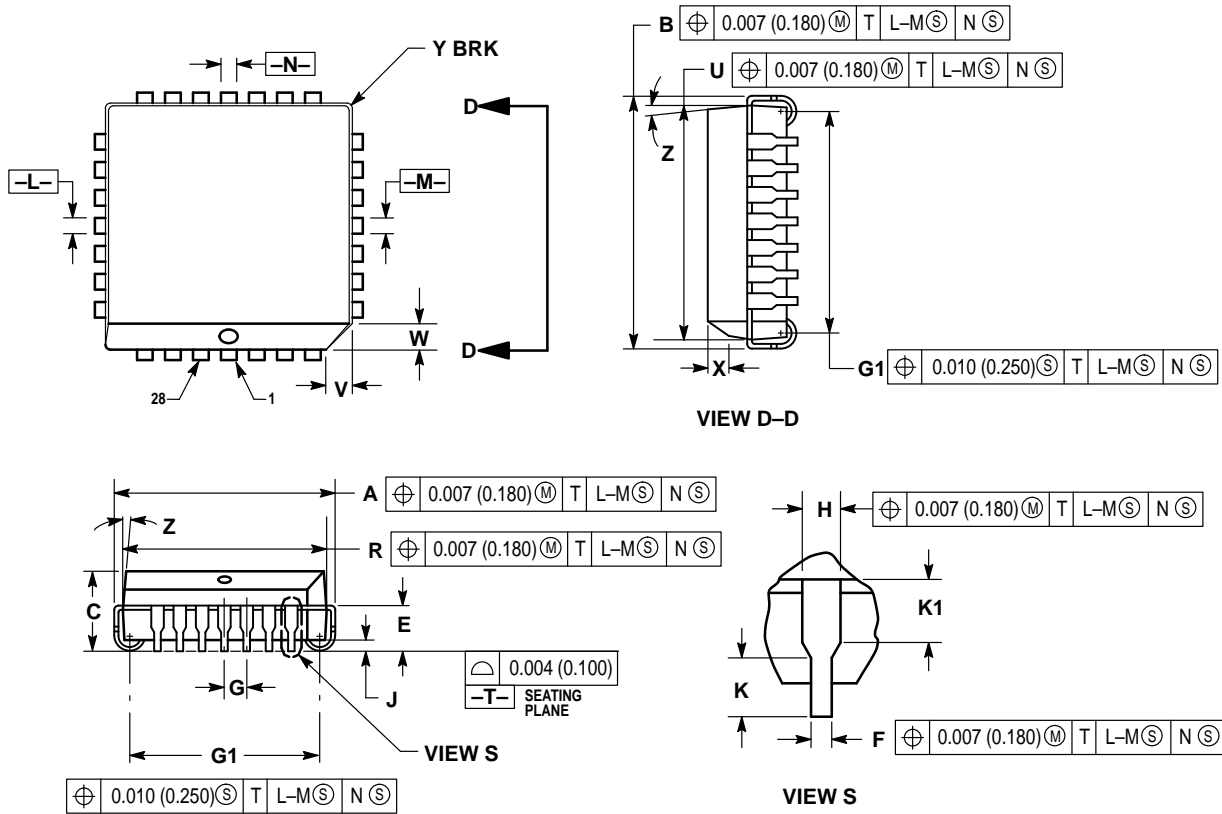
Symbol	Parameter		0°C		25°C		75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
$I_{IH}$ $I_{IL}$	Input HIGH Current Input LOW Current		0.5	225	0.5	145	0.5	145	$\mu\text{A}$ $\mu\text{A}$	
$V_{IH}$ $V_{IL}$	Input HIGH Voltage Input LOW Voltage		-1165 -1810	-880 -1475	-1165 -1810	-880 -1475	-1165 -1810	-880 -1475	mV	
$V_{OH}$ $V_{OL}$	Output HIGH Voltage Output LOW Voltage		-1025 -1810	-880 -1620	-1025 -1810	-880 -1620	-1025 -1810	-880 -1620	mV	50 $\Omega$ to -2.0 V

**TTL DC CHARACTERISTICS:**  $V_{CCT} = 5.0\text{ V} \pm 10\%$ ;  $V_{EE} = -5.2\text{ V} \pm 5\%$  (10H version);  $V_{EE} = -4.2\text{ V}$  to  $-5.5\text{ V}$  (100H version)

Symbol	Parameter		0°C		25°C		75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
$V_{IH}$ $V_{IL}$	Input HIGH Voltage Input LOW Voltage		2.0	0.8	2.0	0.8	2.0	0.8	V V	
$I_{IH}$	Input HIGH Current			20 100		20 100		20 100	$\mu\text{A}$	$V_{IN} = 2.7\text{ V}$ $V_{IN} = 7.0\text{ V}$
$I_{IL}$	Input LOW Current			-0.6		-0.6		-0.6	mA	$V_{IN} = 0.5\text{ V}$
$V_{IK}$	Input Clamp Voltage			-1.2		-1.2		-1.2	V	$I_{IN} = -18\text{ mA}$

OUTLINE DIMENSIONS


FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 776-02  
ISSUE D



NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2° - 10°		2° - 10°	
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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