

# Rail-to-Rail Input and Output, Instrumentation Amplifier

## FEATURES

- **116dB CMRR Independent of Gain**
- **Maximum Offset Voltage: 100 $\mu$ V**
- **Maximum Offset Voltage Drift: 250nV/ $^{\circ}$ C**
- **-40 $^{\circ}$ C to 125 $^{\circ}$ C Operation**
- Rail-to-Rail Input Range
- Rail-to-Rail Output Swing
- Supply Operation: 2.7V to 5.5V
- Available in an MS8 and 3mm  $\times$  3mm  $\times$  0.8mm DFN Packages

## APPLICATIONS


- Thermocouple Amplifiers
- Electronic Scales
- Medical Instrumentation
- Strain Gauge Amplifiers
- High Resolution Data Acquisition

## DESCRIPTION

The LTC<sup>®</sup>6800 is a precision instrumentation amplifier. The CMRR is typically 116dB with a single 5V supply and is independent of gain. The input offset voltage is guaranteed below 100 $\mu$ V with a temperature drift of less than 250nV/ $^{\circ}$ C. The LTC6800 is easy to use; the gain is adjustable with two external resistors, like a traditional op amp.

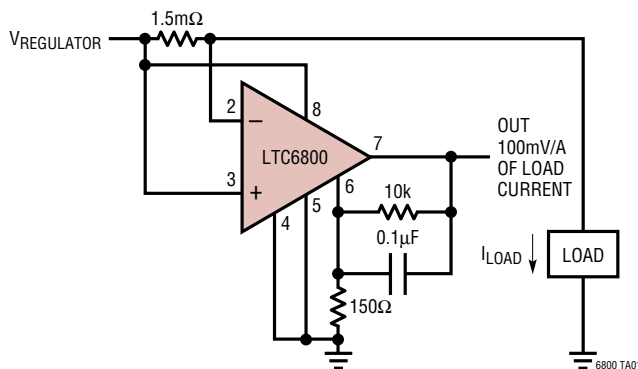
The LTC6800 uses charge balanced sampled data techniques to convert a differential input voltage into a single ended signal that is in turn amplified by a zero-drift operational amplifier.

The differential inputs operate from rail-to-rail and the single ended output swings from rail-to-rail. The LTC6800 is available in an MS8 surface mount package. For space limited applications, the LTC6800 is available in a 3mm  $\times$  3mm  $\times$  0.8mm dual fine pitch leadless package (DFN).

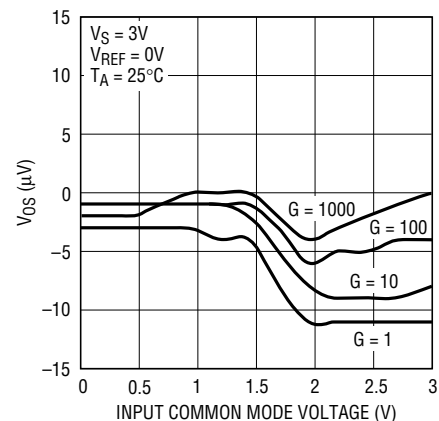
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## TYPICAL APPLICATION

High Side Power Supply Current Sense



Typical Input Referred Offset vs  
Input Common Mode Voltage ( $V_S = 3V$ )



6800 TA02

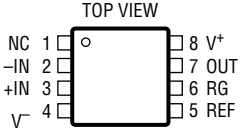
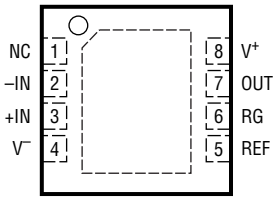
## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage ( $V^+$ to $V^-$ )	5.5V
Input Current	$\pm 10\text{mA}$
$ V_{IN^+} - V_{REF} $	5.5V
$ V_{IN^-} - V_{REF} $	5.5V
Output Short Circuit Duration	Indefinite

Operating Temperature Range (Note 7)	$-40^\circ\text{C}$ to $125^\circ\text{C}$
Storage Temperature Range	
MS8 Package	$-65^\circ\text{C}$ to $150^\circ\text{C}$
DD Package	$-65^\circ\text{C}$ to $125^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$300^\circ\text{C}$

## PACKAGE/ORDER INFORMATION

 <p>MS8 PACKAGE 8-LEAD PLASTIC MSOP <math>T_{JMAX} = 150^\circ\text{C}</math>, <math>\theta_{JA} = 200^\circ\text{C/W}</math></p>	ORDER PART NUMBER	 <p>DD PACKAGE 8-LEAD (3mm x 3mm) PLASTIC DFN <math>T_{JMAX} = 125^\circ\text{C}</math>, <math>\theta_{JA} = 160^\circ\text{C/W}</math> UNDERSIDE METAL INTERNALLY CONNECTED TO <math>V^-</math> (PCB CONNECTION OPTIONAL)</p>	ORDER PART NUMBER
	LTC6800HMS8		LTC6800HDD
	MS8 PART MARKING		DD PART MARKING
	LTAD E		LAEP

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V^+ = 3\text{V}$ ,  $V^- = 0\text{V}$ ,  $REF = 200\text{mV}$ . Output voltage swing is referenced to  $V^-$ . All other specifications reference the OUT pin to the REF pin.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 2)	$V_{CM} = 200\text{mV}$				$\pm 100$	$\mu\text{V}$
Average Input Offset Drift (Note 2)	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	●			$\pm 250$	$\text{nV}/^\circ\text{C}$
	$T_A = 85^\circ\text{C}$ to $125^\circ\text{C}$	●		-1	-2.5	$\mu\text{V}/^\circ\text{C}$
Common Mode Rejection Ratio (Notes 4, 5)	$A_V = 1$ , $V_{CM} = 0\text{V}$ to $3\text{V}$	●	90	113		dB
Integrated Input Bias Current (Note 3)	$V_{CM} = 1.2\text{V}$			4	10	nA
Integrated Input Offset Current (Note 3)	$V_{CM} = 1.2\text{V}$			1	3	nA
Input Noise Voltage	DC to 10Hz			2.5		$\mu\text{V}_{P-P}$
Power Supply Rejection Ratio (Note 6)	$V_S = 2.7\text{V}$ to $5.5\text{V}$	●	110	116		dB
Output Voltage Swing High	$R_L = 2\text{k}$ to $V^-$	●	2.85	2.94		V
	$R_L = 10\text{k}$ to $V^-$	●	2.95	2.98		V
Output Voltage Swing Low		●			20	mV
Gain Error	$A_V = 1$				0.1	%
Gain Nonlinearity	$A_V = 1$				100	ppm

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V^+ = 3\text{V}$ ,  $V^- = 0\text{V}$ ,  $\text{REF} = 200\text{mV}$ . Output voltage swing is referenced to  $V^-$ . All other specifications reference the OUT pin to the REF pin.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	No Load ●			1.2	mA
Internal Op Amp Gain Bandwidth			200		kHz
Slew Rate			0.2		V/ $\mu\text{s}$
Internal Sampling Frequency			3		kHz

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $\text{REF} = 200\text{mV}$ . Output voltage swing is referenced to  $V^-$ . All other specifications reference the OUT pin to the REF pin.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 2)	$V_{\text{CM}} = 200\text{mV}$			$\pm 100$	$\mu\text{V}$
Average Input Offset Drift (Note 2)	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ $T_A = 85^\circ\text{C}$ to $125^\circ\text{C}$	● ●	 -1	$\pm 250$ -2.5	$\text{nV}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$
Common Mode Rejection Ratio (Notes 4, 5)	$A_V = 1$ , $V_{\text{CM}} = 0\text{V}$ to $5\text{V}$	●	90	116	dB
Integrated Input Bias Current (Note 3)	$V_{\text{CM}} = 1.2\text{V}$		4	10	nA
Integrated Input Offset Current (Note 3)	$V_{\text{CM}} = 1.2\text{V}$		1	3	nA
Power Supply Rejection Ratio (Note 6)	$V_S = 2.7\text{V}$ to $5.5\text{V}$	●	110	116	dB
Output Voltage Swing High	$R_L = 2\text{k}$ to $V^-$ $R_L = 10\text{k}$ to $V^-$	● ●	4.85 4.95	4.94 4.98	V V
Output Voltage Swing Low		●		20	mV
Gain Error	$A_V = 1$			0.1	%
Gain Nonlinearity	$A_V = 1$			100	ppm
Supply Current	No Load	●		1.3	mA
Internal Op Amp Gain Bandwidth			200		kHz
Slew Rate			0.2		V/ $\mu\text{s}$
Internal Sampling Frequency			3		kHz

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic test systems.  $V_{\text{OS}}$  is measured to a limit determined by test equipment capability.

**Note 3:** If the total source resistance is less than  $10\text{k}$ , no DC errors result from the input bias currents or the mismatch of the input bias currents or the mismatch of the resistances connected to  $-IN$  and  $+IN$ .

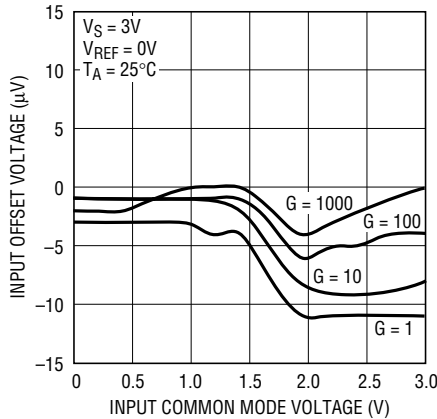
**Note 4:** The CMRR with a voltage gain,  $A_V$ , larger than 10 is 120dB (typ).

**Note 5:** At temperatures above  $70^\circ\text{C}$ , the common mode rejection ratio lowers when the common mode input voltage is within 100mV of the supply rails.

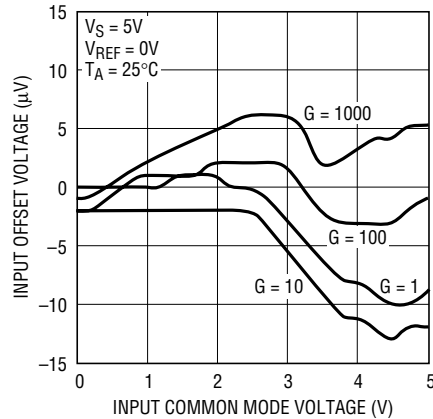
**Note 6:** The power supply rejection ratio (PSRR) measurement accuracy depends on the proximity of the power supply bypass capacitor to the device under test. Because of this, the PSRR is 100% tested to relaxed limits at final test. However, their values are guaranteed by design to meet the data sheet limits.

**Note 7:** The LTC6800H is guaranteed functional over the operating temperature range of  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ . Specifications over the  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  range (denoted by ●) are assured by design and characterization but are not tested or QA sampled at these temperatures.

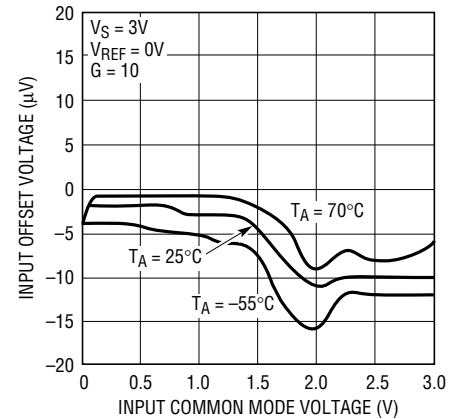
## TYPICAL PERFORMANCE CHARACTERISTICS

Input Offset Voltage  
vs Input Common Mode Voltage

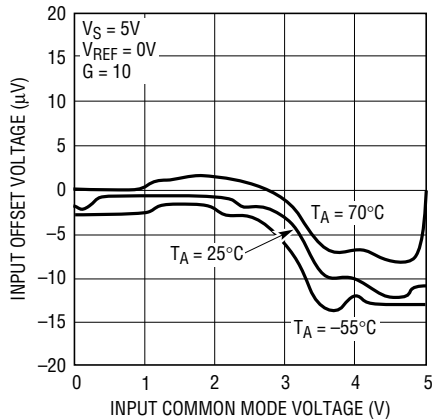
6800 G01

Input Offset Voltage  
vs Input Common Mode Voltage

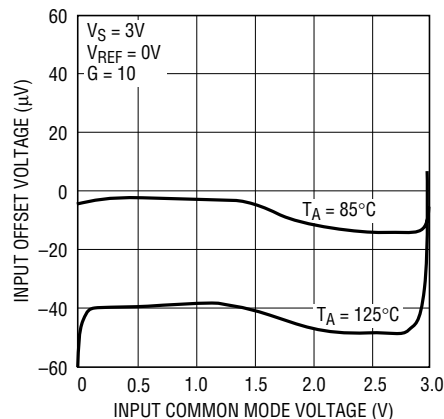
2053 G02

Input Offset Voltage  
vs Input Common Mode Voltage

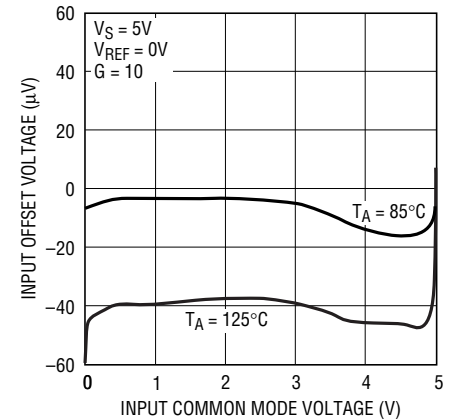
6800 G03

Input Offset Voltage  
vs Input Common Mode Voltage

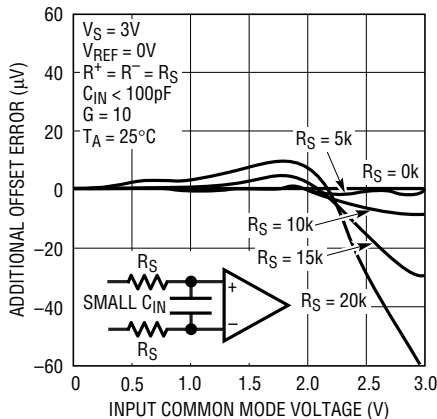
6800 G04

Input Offset Voltage vs Input  
Common Mode Voltage,  
 $85^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ 

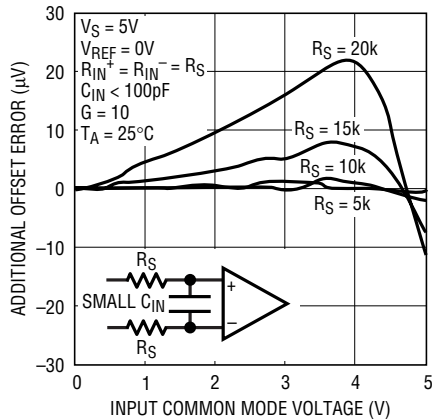
6800 G05

Input Offset Voltage vs Input  
Common Mode Voltage,  
 $85^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ 

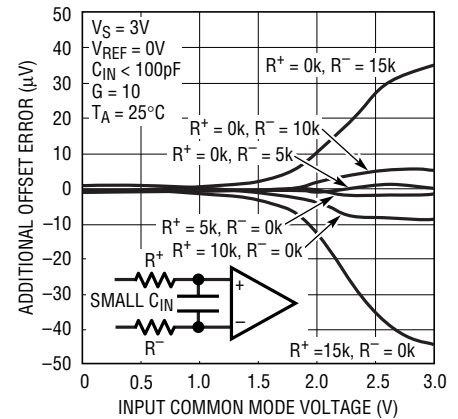
6800 G06

Additional Input Offset Due to  
Input  $R_S$  vs Input Common Mode  
( $C_{\text{IN}} < 100\text{pF}$ )

6800 G07

Additional Input Offset Due to  
Input  $R_S$  vs Input Common Mode  
( $C_{\text{IN}} < 100\text{pF}$ )

6800 G08

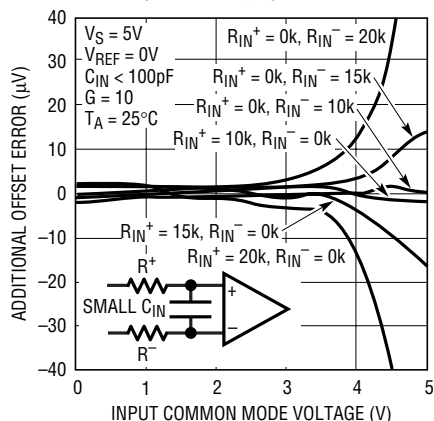
Additional Input Offset Due to Input  
 $R_S$  Mismatch vs Input Common  
Mode ( $C_{\text{IN}} < 100\text{pF}$ )

6800 G09

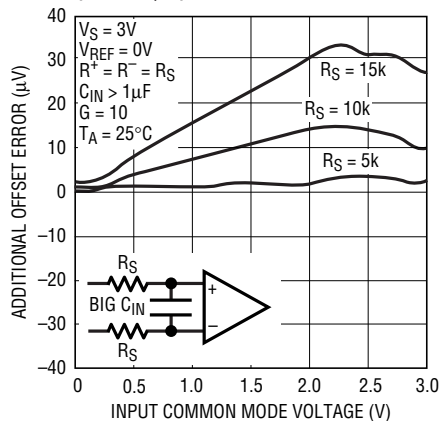
6800fa

# TYPICAL PERFORMANCE CHARACTERISTICS

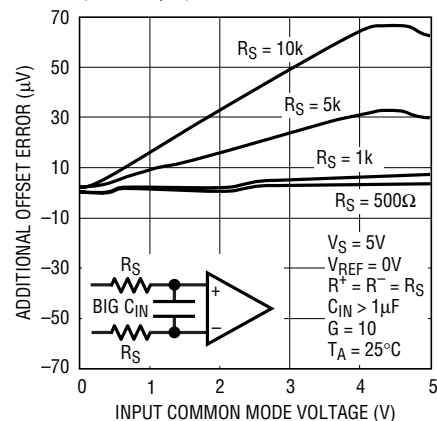
**Additional Input Offset Due to Input  $R_S$  Mismatch vs Input Common Mode ( $C_{IN} < 100\text{pF}$ )**



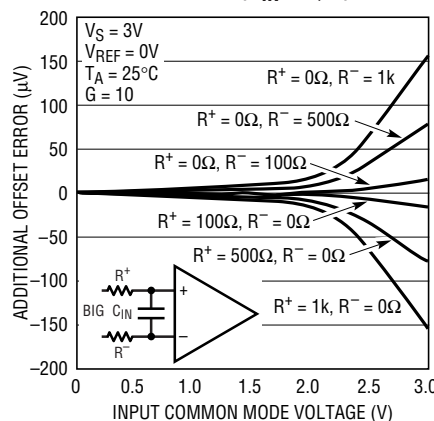
**Additional Input Offset Due to Input  $R_S$  vs Input Common Mode ( $C_{IN} > 1\mu\text{F}$ )**



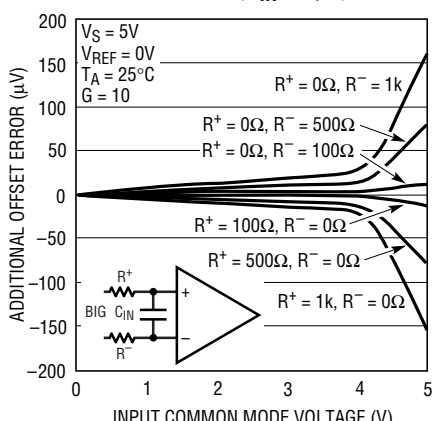
**Additional Input Offset Due to Input  $R_S$  vs Input Common Mode ( $C_{IN} > 1\mu\text{F}$ )**



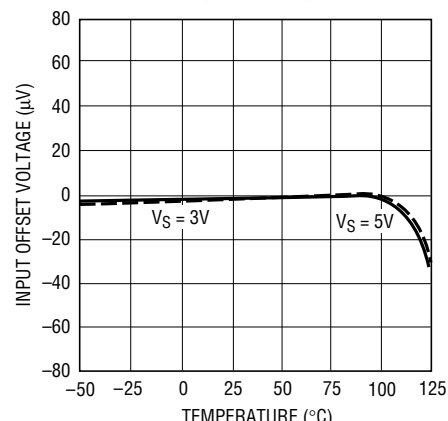
**Additional Input Offset Due to Input  $R_S$  Mismatch vs Input Common Mode ( $C_{IN} > 1\mu\text{F}$ )**



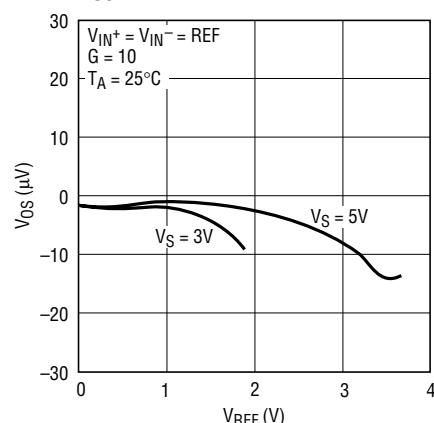
**Additional Input Offset Due to Input  $R_S$  Mismatch vs Input Common Mode ( $C_{IN} > 1\mu\text{F}$ )**



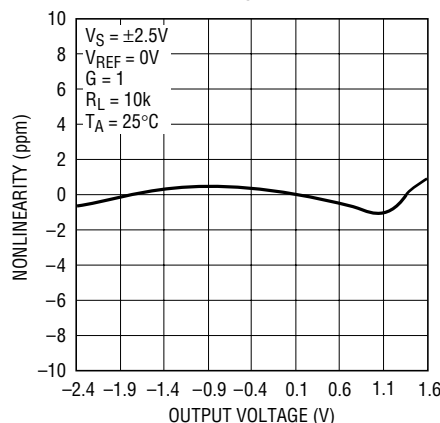
**Offset Voltage vs Temperature**



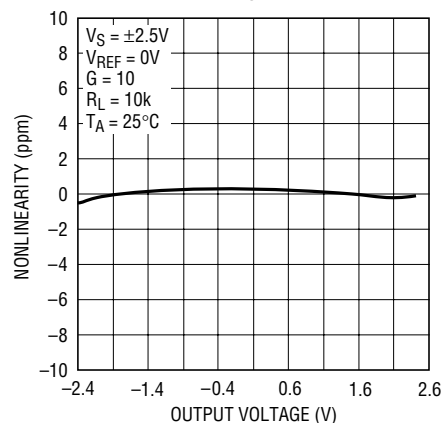
**$V_{OS}$  vs  $V_{REF}$**



**Gain Nonlinearity,  $G = 1$**

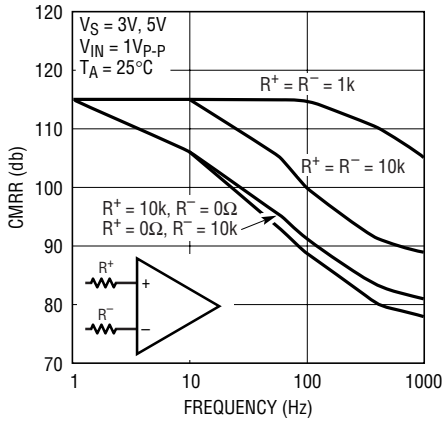


**Gain Nonlinearity,  $G = 10$**



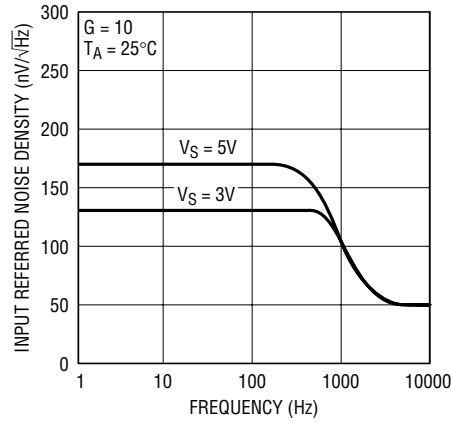
# TYPICAL PERFORMANCE CHARACTERISTICS

CMRR vs Frequency



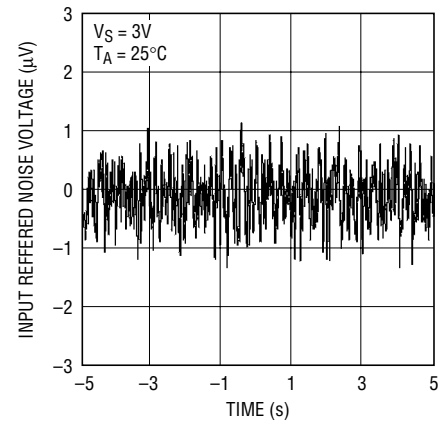
6800 G19

Input Voltage Noise Density vs Frequency



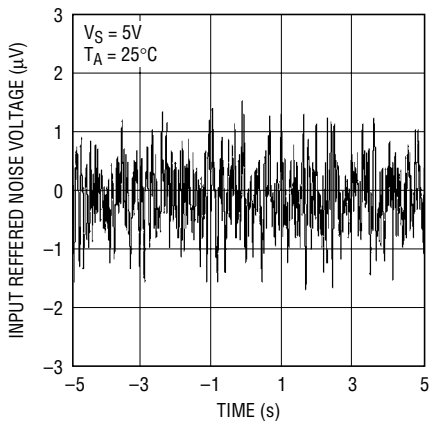
6800 G20

Input Referred Noise in 10Hz Bandwidth



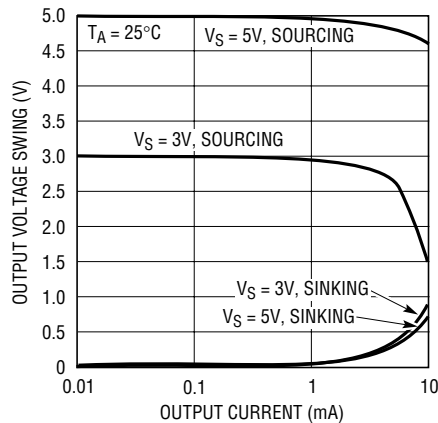
6800 G21

Input Referred Noise in 10Hz Bandwidth



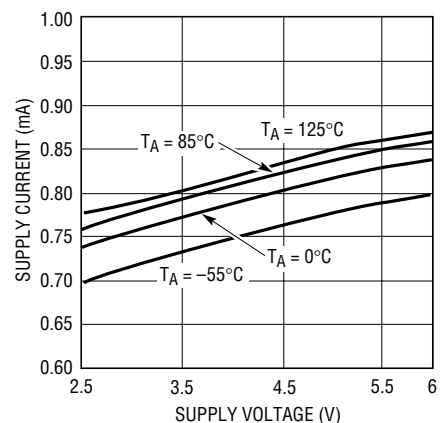
6800 G22

Output Voltage Swing vs Output Current



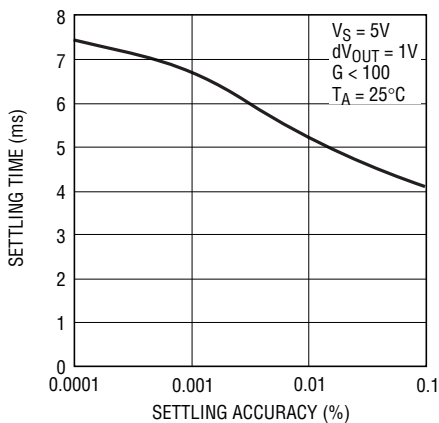
6800 G23

Supply Current vs Supply Voltage



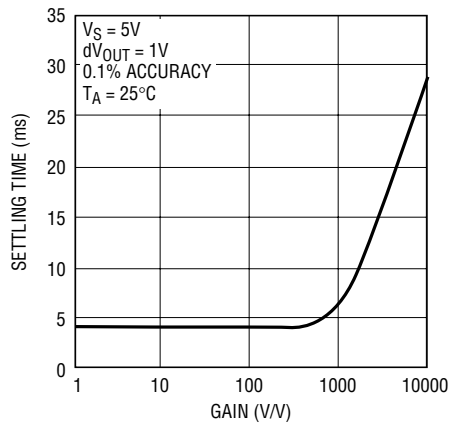
6800 G24

Low Gain Settling Time vs Settling Accuracy



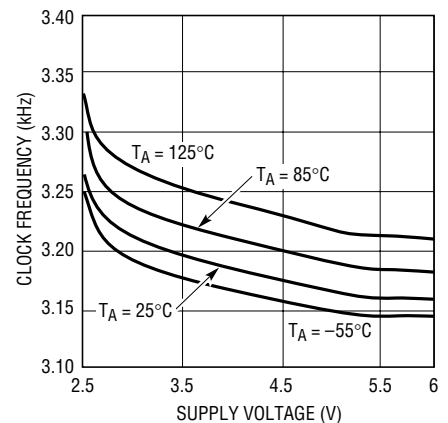
6800 G25

Settling Time vs Gain



6800 G26

Internal Clock Frequency vs Supply Voltage



6800 G27

## PIN FUNCTIONS

**NC (Pin 1):** Not Connected.

**–IN (Pin 2):** Inverting Input.

**+IN (Pin 3):** Noninverting Input.

**V<sup>–</sup> (Pin 4):** Negative Supply.

**REF (Pin 5):** Voltage Reference ( $V_{REF}$ ) for Amplifier Output.

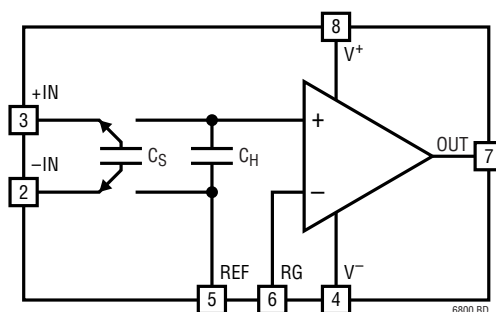
**RG (Pin 6):** Inverting Input of Internal Op Amp. With a resistor,  $R_2$ , connected between the OUT pin and the RG pin and a resistor,  $R_1$ , between the RG pin and the REF pin, the DC gain is given by  $1 + R_2 / R_1$ .

**OUT (Pin 7):** Amplifier Output.

$$V_{OUT} = GAIN (V_{+IN} - V_{-IN}) + V_{REF}$$

**V<sup>+</sup> (Pin 8):** Positive Supply.

## BLOCK DIAGRAM



## APPLICATIONS INFORMATION

### Theory of Operation

The LTC6800 uses an internal capacitor ( $C_S$ ) to sample a differential input signal riding on a DC common mode voltage (see Block Diagram). This capacitor's charge is transferred to a second internal hold capacitor ( $C_H$ ) translating the common mode of the input differential signal to that of the REF pin. The resulting signal is amplified by a zero-drift op amp in the noninverting configuration. The RG pin is the negative input of this op amp and allows external programmability of the DC gain. Simple filtering can be realized by using an external capacitor across the feedback resistor.

### Input Voltage Range

The input common mode voltage range of the LTC6800 is rail-to-rail. However, the following equation limits the size of the differential input voltage:

$$V^- \leq (V_{+IN} - V_{-IN}) + V_{REF} \leq V^+ - 1.3$$

where  $V_{+IN}$  and  $V_{-IN}$  are the voltages of the +IN and -IN pins respectively,  $V_{REF}$  is the voltage at the REF pin and  $V^+$  is the positive supply voltage.

For example, with a 3V single supply and a 0V to 100mV differential input voltage,  $V_{REF}$  must be between 0V and 1.6V.

### Settling Time

The sampling rate is 3kHz and the input sampling period during which  $C_S$  is charged to the input differential voltage  $V_{IN}$  is approximately 150 $\mu$ s. First assume that on each input sampling period,  $C_S$  is charged fully to  $V_{IN}$ . Since  $C_S = C_H (= 1000\text{pF})$ , a change in the input will settle to N bits of accuracy at the op amp noninverting input after N clock cycles or 333 $\mu$ s(N). The settling time at the OUT pin is also affected by the settling of the internal op amp. Since the gain bandwidth of the internal op amp is typically 200kHz, the settling time is dominated by the switched capacitor front end for gains below 100 (see Typical Performance Characteristics).

SINGLE SUPPLY, UNITY GAIN

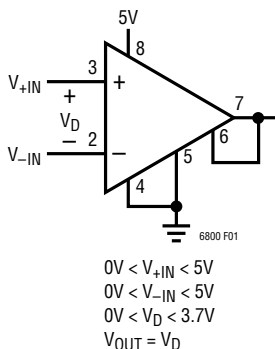


Figure 1



## APPLICATIONS INFORMATION

### Input Current

Whenever the differential input  $V_{IN}$  changes,  $C_H$  must be charged up to the new input voltage via  $C_S$ . This results in an input charging current during each input sampling period. Eventually,  $C_H$  and  $C_S$  will reach  $V_{IN}$  and, ideally, the input current would go to zero for DC inputs.

In reality, there are additional parasitic capacitors which disturb the charge on  $C_S$  every cycle even if  $V_{IN}$  is a DC voltage. For example, the parasitic bottom plate capacitor on  $C_S$  must be charged from the voltage on the REF pin to the voltage on the  $-IN$  pin every cycle. The resulting input charging current decays exponentially during each input sampling period with a time constant equal to  $R_S C_S$ . **If the voltage disturbance due to these currents settles before the end of the sampling period, there will be no errors due to source resistance or the source resistance mismatch between  $-IN$  and  $+IN$ . With  $R_S$  less than 10k, no DC errors occur due to this input current.**

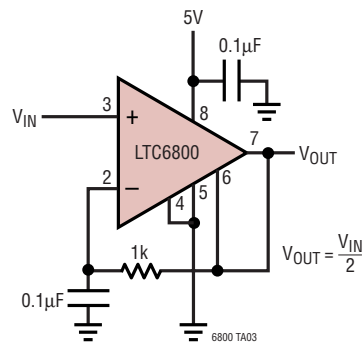
In the Typical Performance Characteristics section of this data sheet, there are curves showing the additional error from nonzero source resistance in the inputs. If there are no large capacitors across the inputs, the amplifier is less sensitive to source resistance and source resistance mismatch. When large capacitors are placed across the inputs, the input charging currents described above result in larger DC errors, especially with source resistor mismatches.

### Power Supply Bypassing

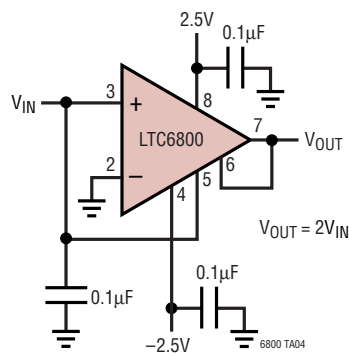
The LTC6800 uses a sampled data technique and therefore contains some clocked digital circuitry. It is therefore sensitive to supply bypassing. A 0.1 $\mu$ F ceramic capacitor must be connected between Pin 8 ( $V^+$ ) and Pin 4 ( $V^-$ ) with leads as short as possible.

TYPICAL APPLICATIONS

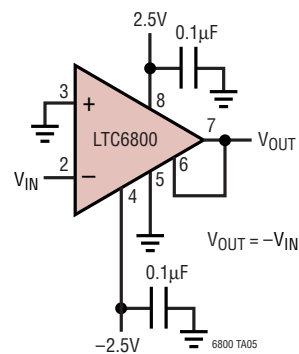
Precision ÷2



Precision Doubler (General Purpose)

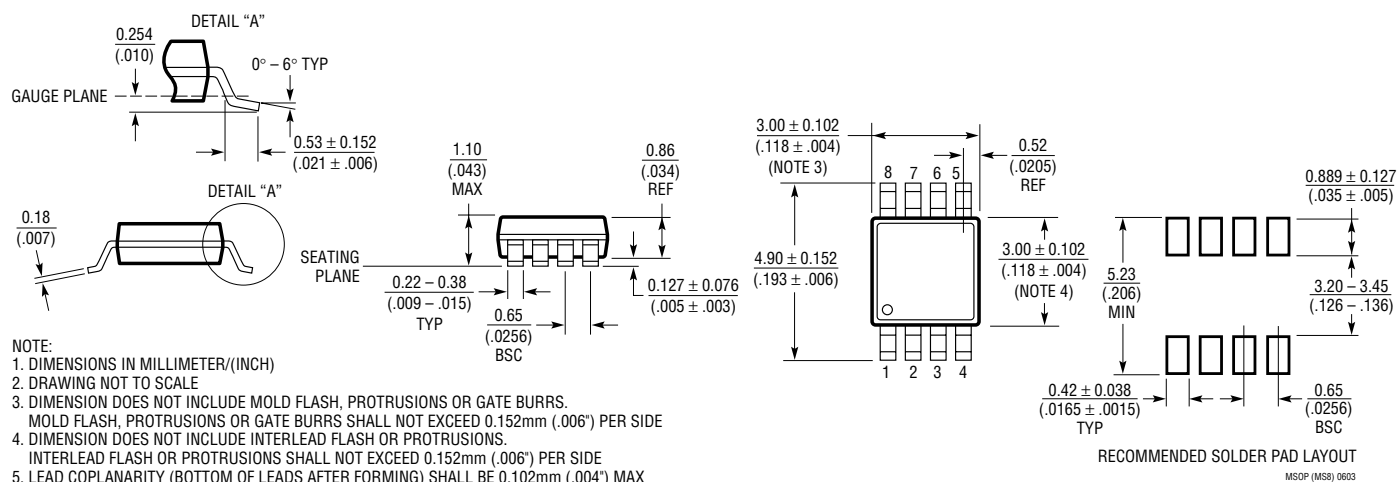


Precision Inversion (General Purpose)

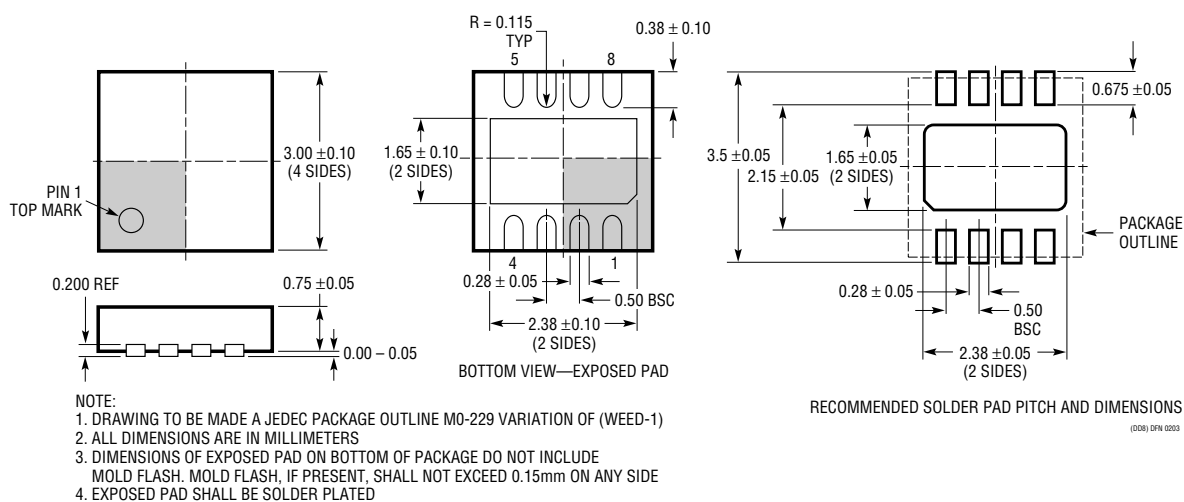


# PACKAGE DESCRIPTION

## MS8 Package 8-Lead Plastic MSOP (Reference LTC DWG # 05-08-1660)

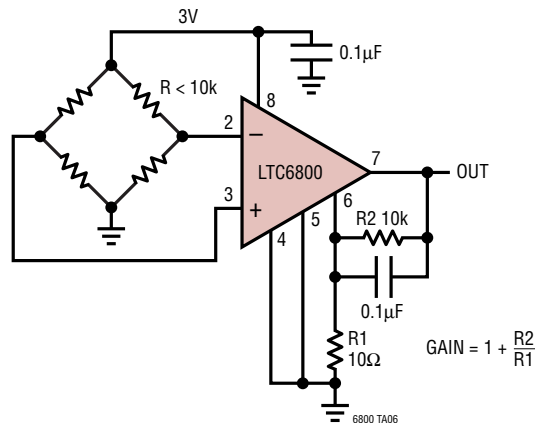


## DD Package 8-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1698)



## TYPICAL APPLICATION

Differential Bridge Amplifier



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1100	Precision Zero Drift Instrumentation Amplifier	Fixed Gains of 10 or 100, 10µV Offset, 50pA Input Bias Current
LT <sup>®</sup> 1101	Precision, Micropower, Single Supply Instrumentation Amplifier	Fixed Gains of 10 or 100, $I_S < 105\mu A$
LT1167	Single Resistor Gain Programmable, Precision Instrumentation Amplifier	Single Gain Set Resistor: $G = 1$ to 10,000, Low Noise: 7.5nV/√Hz
LT1168	Low Power Single Resistor Gain Programmable, Precision Instrumentation Amplifier	$I_{SUPPLY} = 530\mu A$
LTC1043	Dual Precision Instrumentation Switched-Capacitor Building Block	Rail-to-Rail Input, 120dB CMRR
LT1789-1	Single Supply, Rail-to-Rail Output, Micropower Instrumentation Amplifier	$I_{SUPPLY} = 80\mu A$ Maximum
LTC2050	Zero-Drift Operation Amplifier	SOT-23 Package, 3µV Max $V_{OS}$ , 30nV/°C Max Drift
LTC2051	Dual Zero-Drift Operational Amplifier	MS8 Package, 3µV Max $V_{OS}$ , 30nV/°C Max Drift
LTC2052	Quad Zero-Drift Operational Amplifier	GN-16 Package, 3µV Max $V_{OS}$ , 30nV/°C Max Drift
LTC2053	Single Supply, Zero Drift, Rail-to-Rail Input and Output Instrumentation Amplifier	MS8 Package, 10µV Max $V_{OS}$ , 50nV/°C Max Drift

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