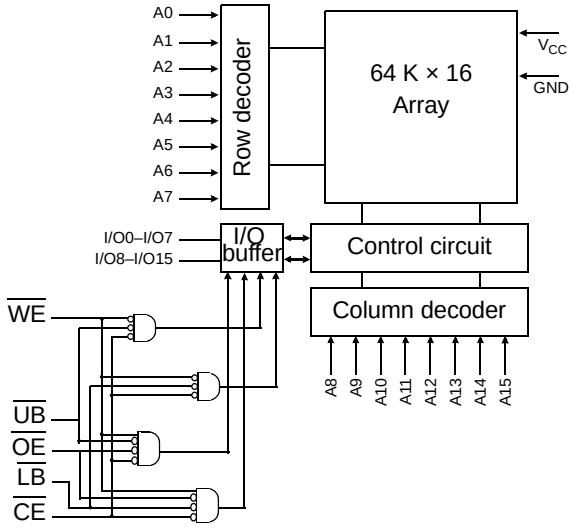
3.3 V 64K X 16 CMOS SRAM

Features

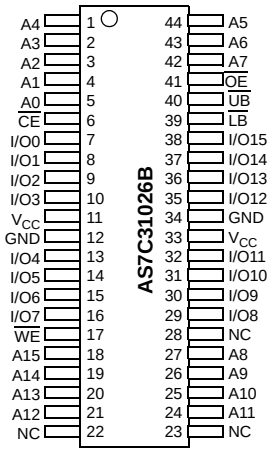
- Industrial and commercial versions
- Organization: 65,536 words × 16 bits
- Center power and ground pins for low noise
- High speed
  - 10/12/15/20 ns address access time
  - 5, 6, 7, 8 ns output enable access time
- Low power consumption: ACTIVE
  - 288 mW / max @ 10 ns
- Low power consumption: STANDBY
  - 18 mW / max CMOS I/O
- 6 T 0.18 u CMOS technology
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- JEDEC standard packaging
  - 44-pin 400 mil SOJ
  - 44-pin TSOP 2-400
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangement

44-Pin SOJ (400 mil), TSOP 2



Selection guide

	-10	-12	-15	-20	Unit
Maximum address access time	10	12	15	20	ns
Maximum output enable access time	5	6	7	8	ns
Maximum operating current	80	75	70	65	mA
Maximum CMOS standby current	5	5	5	5	mA

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Functional description

The AS7C31026B is a high-performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) device organized as 65,536 words × 16 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 5, 6, 7, 8 ns are ideal for high-performance applications.

When $\overline{CE}$ is high, the device enters standby mode. A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O0 through I/O15 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$) with write enable ($\overline{WE}$) high. The chips drive I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive or write enable is active, output drivers stay in high-impedance mode.

The device provides multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. $\overline{LB}$ controls the lower bits, I/O0 through I/O7, and $\overline{UB}$ controls the higher bits, I/O8 through I/O15.

All chip inputs and outputs are TTL-compatible, and operation is from a single 3.3 V supply. The device is packaged in common industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	V_{t1}	–0.50	+5.0	V
Voltage on any pin relative to GND	V_{t2}	–0.50	V_{CC} +0.50	V
Power dissipation	P_D	–	1.0	W
Storage temperature (plastic)	T_{stg}	–65	+150	°C
Ambient temperature with VCC applied	T_{bias}	–55	+125	°C
DC current into outputs (low)	I_{OUT}	–	20	mA

Note: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0–I/O7	I/O8–I/O15	Mode
H	X	X	X	X	High Z	High Z	Standby (I_{SB}), I_{SBI})
L	H	L	L	H	D_{OUT}	High Z	Read I/O0–I/O7 (I_{CC})
L	H	L	H	L	High Z	D_{OUT}	Read I/O8–I/O15 (I_{CC})
L	H	L	L	L	D_{OUT}	D_{OUT}	Read I/O0–I/O15 (I_{CC})
L	L	X	L	L	D_{IN}	D_{IN}	Write I/O0–I/O15 (I_{CC})
L	L	X	L	H	D_{IN}	High Z	Write I/O0–I/O7 (I_{CC})
L	L	X	H	L	High Z	D_{IN}	Write I/O8–I/O15 (I_{CC})
L L	H X	H X	X H	X H	High Z	High Z	Output disable (I_{CC})

Key: H = high, L = low, X = don't care.

Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage		V_{CC}	3.0	3.3	3.6	V
Input voltage		V_{IH}	2.0	–	V_{CC} + 0.5	V
		V_{IL}	–0.5	–	0.8	V
Ambient operating temperature	commercial	T_A	0	–	70	^{o} C
	industrial	T_A	–40	–	85	^{o} C

V_{IL} = -1.0V for pulse width less than 5ns

V_{IH} = V_{CC} + 1.5V for pulse width less than 5ns

DC operating characteristics (over the operating range)[1]

Parameter	Sym	Test conditions	-10		-12		-15		-20		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = Max V_{IN} = GND to V_{CC}	–	1	–	1	–	1	–	1	µA
Output leakage current	$\lvert I_{LO} \rvert$	V_{CC} = Max $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	1	–	1	–	1	–	1	µA
Operating power supply current	I_{CC}	V_{CC} = Max, $\overline{CE} \le V_{IL}$, I_{OUT} = 0mA f = f_{Max}	–	80	–	75	–	70	–	65	mA
Standby power supply current	I_{SB}	V_{CC} = Max, $\overline{CE} \ge V_{IH}$, f = f_{Max}	–	30	–	25	–	20	–	20	mA
	I_{SB1}	V_{CC} = Max, $\overline{CE} \ge V_{CC}$–0.2 V, $V_{IN} \le$ 0.2 V or $V_{IN} \ge V_{CC}$–0.2 V, f = 0	–	5	–	5	–	5	–	5	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min	–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min	2.4	–	2.4	–	2.4	–	2.4	–	V

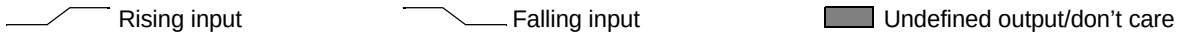
Capacitance (f = 1MHz, T_a = 25 °C, V_{CC} = NOMINAL)[2]

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, $\overline{LB}$, $\overline{UB}$	V_{IN} = 0 V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{IN} = V_{OUT} = 0 V	7	pF

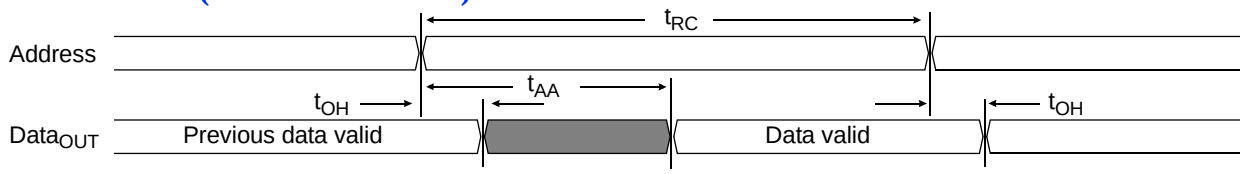
Read cycle (over the operating range)[3,9]

Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	10	–	12	–	15	–	20	–	ns	
Address access time	t_{AA}	–	10	–	12	–	15	–	20	ns	3
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	10	–	12	–	15	–	20	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	5	–	6	–	7	–	8	ns	
Output hold from address change	t_{OH}	3	–	3	–	3	–	3	–	ns	5
$\overline{CE}$ low to output in low Z	t_{CLZ}	3	–	3	–	3	–	3	–	ns	4, 5
$\overline{CE}$ high to output in high Z	t_{CHZ}	–	3	–	3	–	4	–	5	ns	4, 5
$\overline{OE}$ low to output in low Z	t_{OLZ}	0	–	0	–	0	–	0	–	ns	4, 5
Byte select access time	t_{BA}	–	5	–	6	–	7	–	8	ns	
Byte select Low to low Z	t_{BLZ}	0	–	0	–	0	–	0	–	ns	4, 5
Byte select High to high Z	t_{BHZ}	–	5	–	6	–	6	–	8	ns	4, 5
$\overline{OE}$ high to output in high Z	t_{OHZ}	–	5	–	6	–	7	–	8	ns	4, 5
Power up time	t_{PU}	0	–	0	–	0	–	0	–	ns	4, 5
Power down time	t_{PD}	–	10	–	12	–	15		20	ns	4, 5

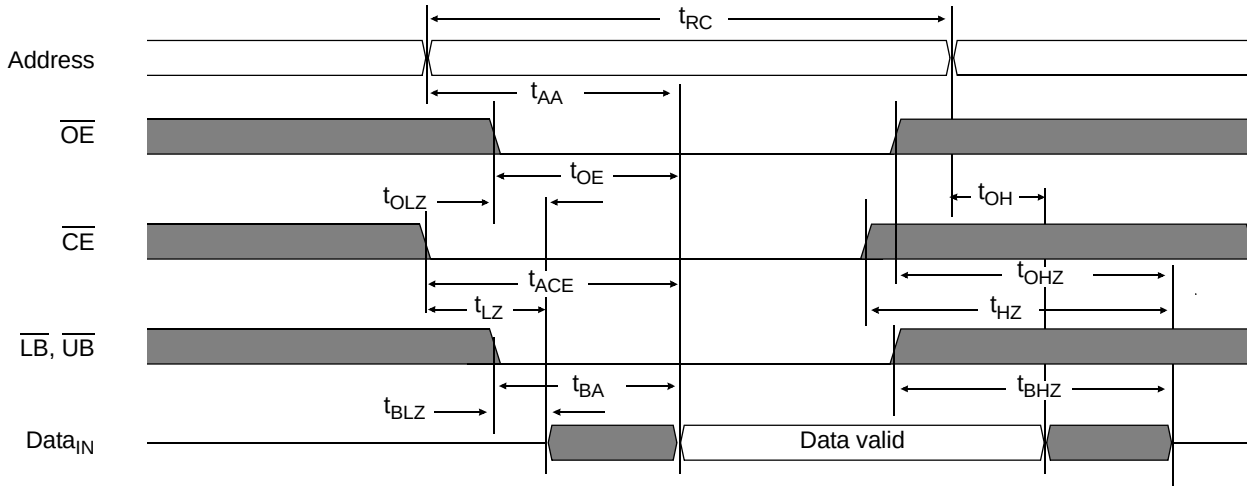
Key to switching waveforms



Read waveform 1 (address controlled)[3,6,7,9]



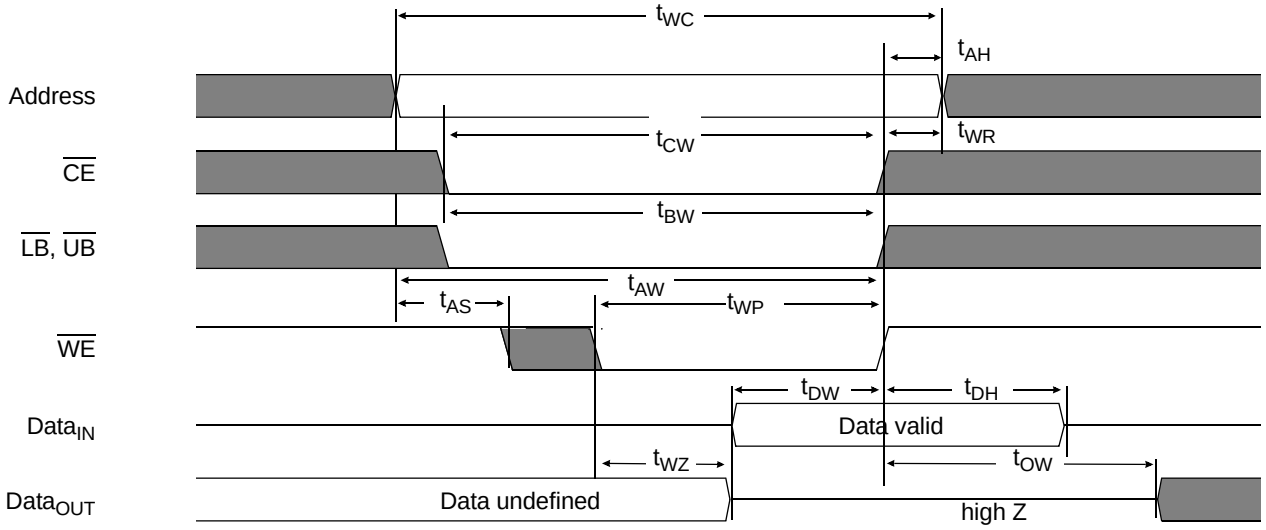
Read waveform 2 ($\overline{OE}$, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ controlled)[3,6,8,9]



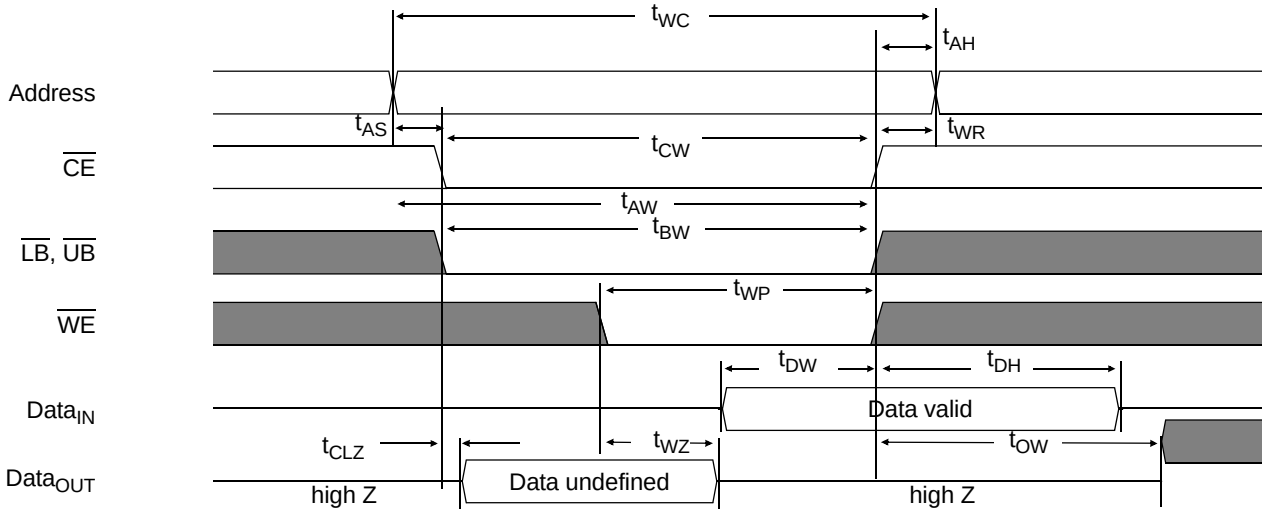
Write cycle (over the operating range) [11]

Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	10	–	12	–	15	–	20	–	ns	
Chip enable ($\overline{CE}$) to write end	t_{CW}	8	–	9	–	10	–	12	–	ns	
Address setup to write end	t_{AW}	8	–	9	–	10	–	12	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns	
Write pulse width	t_{WP}	7	–	8	–	9	–	12	–	ns	
Write recovery time	t_{WR}	0	–	0	–	0	–	0	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	5	–	6	–	8	–	10	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	ns	5
Write enable to output in high Z	t_{WZ}	–	5	–	6	–	7	–	8	ns	4, 5
Output active from write end	t_{OW}	1	–	1	–	1	–	2	–	ns	4, 5
Byte select low to end of write	t_{BW}	7	–	8	–	9	–	9	–	ns	

Write waveform 1 ($\overline{WE}$ controlled)[10,11]



Write waveform 2 ($\overline{CE}$ controlled)[10,11]



AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to 3.0 V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5

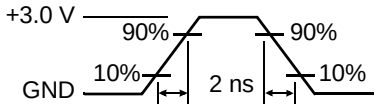


Figure A: Input pulse

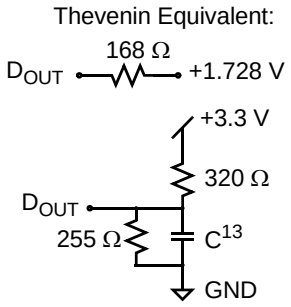
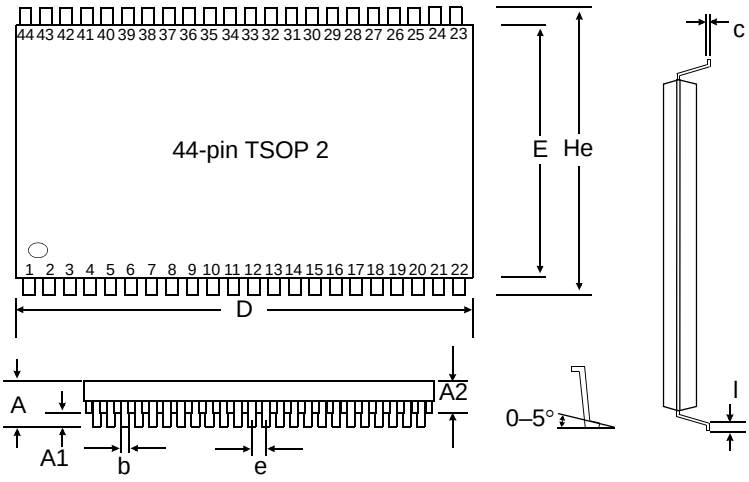


Figure B: 3.3 V Output load

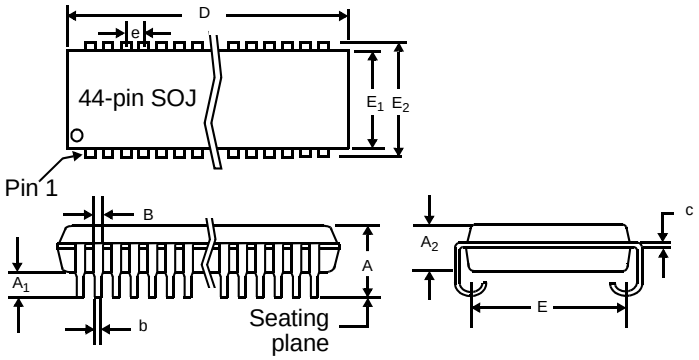
Notes

1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled, but not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A and B.
4 These parameters are specified with C_L = 5 pF, as in Figures B. Transition is measured ± 500 mV from steady-state voltage.
5 This parameter is guaranteed, but not tested.
6 $\overline{WE}$ is high for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are low for read cycle.
8 Address is valid prior to or coincident with $\overline{CE}$ transition low.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 N/A
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 Not applicable.
13 C = 30 pF, except all high Z and low Z parameters where C = 5 pF.

Package dimensions



	44-pin TSOP 2	
	Min (mm)	Max (mm)
A		1.2
A1	0.05	0.15
A2	0.95	1.05
b	0.30	0.45
c	0.120	0.21
D	18.31	18.52
E	10.06	10.26
He	11.68	11.94
e	0.80 (typical)	
l	0.40	0.60



	44-pin SOJ 400 mil	
	Min (in)	Max (in)
A	0.128	0.148
A_1	0.025	–
A_2	0.105	0.115
B	0.026	0.032
b	0.015	0.020
c	0.007	0.013
D	1.120	1.130
E	0.370 NOM	
E_1	0.395	0.405
E_2	0.435	0.445
e	0.050 NOM	

Ordering codes

Package\Access time	Volt/Temp	10 ns	12 ns	15 ns	20 ns
Plastic SOJ, 400 mil	3.3 V commercial	AS7C31026B-10JC	AS7C31026B-12JC	AS7C31026B-15JC	AS7C31026B-20JC
	3.3 V industrial	AS7C31026B-10JI	AS7C31026B-12JI	AS7C31026B-15JI	AS7C31026B-20JI
TSOP 2, 10.2 x 18.4 mm	3.3 V commercial	AS7C31026B-10TC	AS7C31026B-12TC	AS7C31026B-15TC	AS7C31026B-20TC
	3.3 V industrial	AS7C31026B-10TI	AS7C31026B-12TI	AS7C31026B-15TI	AS7C31026B-20TI

Note:
Add suffix 'N' to the above part number for lead free parts (Ex. AS7C31026B-10JCN)

Part numbering system

AS7C	X	1026B	–XX	X	X	X
SRAM prefix	Voltage: 3 = 3.3 V CMOS	Device number	Access time	Package: J = SOJ 400 mil T = TSOP 2, 10.2 x 18.4 mm	Temperature range: C = commercial: 0° C to 70° C I = industrial: -40° C to 85° C	N=Lead Free Part

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