Integrated Circuit Systems, Inc.

ICS9120-11

Frequency Generator for Multimedia Audio Synthesis

General Description

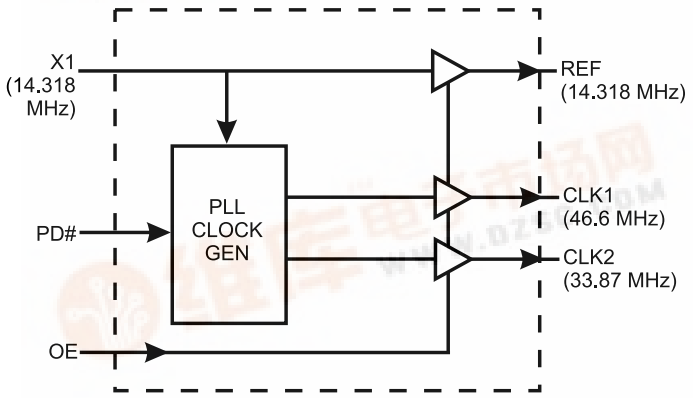
The **ICS9120-11** is a high performance frequency generator. The **ICS9120-11** provides high accuracy; low jitter PLLs meet the 0.20% frequency tolerance and -96dB signal-to-noise ratios. Fast output clock edge rates minimize board induced jitter.

The **ICS9120-11** operates over the entire 3.0 - 5.5V range and provides power-down to minimize energy consumption.

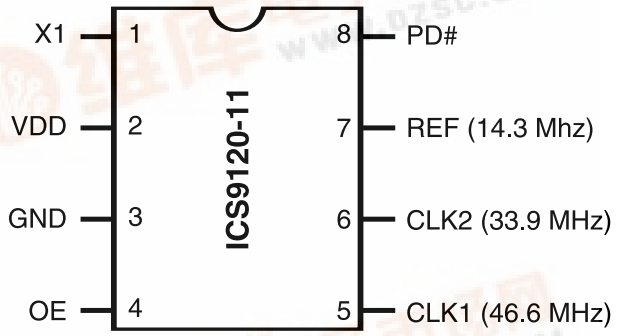
Features

- Generates 46.6 MHz and 33.868 MHz clocks
- Buffered REFCLK output
- 0.20% frequency accuracy
- 100ps one sigma jitter maintains 16-bit performance
- Output rise/fall times less than 2.5ns
- On-chip loop filter components
- 3.0V - 5.5V supply range
- 8-pin, 150-mil SOIC package Advance Information

Block Diagram



Pin Configuration



8-Pin SOIC

Functionality

X1 (MHz)	PD#	33.9 (MHz)	46.6 (MHz)	14.3 (MHz)
-	0	Low	Low	Low
14.318	1	33.868	46.6	14.318

Note: PD# (Pin 8) and OE (Pin 4) are internally pulled-up to VDD and therefore may be left disconnected or driven by open collector logic.

Pin Descriptions for ICS9120-11

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	X1	Input	External clock source.*
2	VDD	Power	+Power supply input.
3	GND	Power	Ground return for Pin 2.
4	OE	Input	Output Enable (tristates all outputs when at logic low level); has pull-up.
5	CLK1	Input	46.6 MHz clock output.
6	CLK2	Output	33.9 MHz clock output.
7	REF	Output	14.318 MHz reference clock output.
8	PD#	Input	Power-down input (powers-down entire device when low); has pull-up.

* Pin 1 contains no loading capacitor.

Absolute Maximum Ratings

AVDD, VDD referenced to GND 7V
Operating temperature under bias ..... 0°C to +70°C
Storage temperature ..... -65°C to +150°C
Voltage on I/O pins referenced to GND ..... GND -0.5V to VDD +0.5V
Power dissipation ..... 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5V

Operating V_{DD} = +4.5V to +5.5V; T_A =0°C to 70°C unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics						
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-18.0	-8.3	-	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-	-	5.0	µA
Output Low Voltage	V_{OL}*	I_{OL}=+10mA	-	0.15	0.4	V
Output High Voltage	V_{OH}*	I_{OH}=-30mA	2.4	3.7	-	V
Output Low Current	I_{OL}*	V_{OL}=0.8V	25.0	45.0	-	mA
Output High Current	I_{OH}*	V_{OH}=2.4V	-	-53.0	-35.0	mA
Supply Current	I_{DD}	Unloaded	-	23.0	50.0	mA
Supply Current, Power-down	I_{DD} (PD)	Unloaded	-	250.0	500.0	µA
Pull-up Resistor Valve	R_{pu}*		-	400.0	800.0	k ohm
AC Characteristics						
Rise Time 0.8 to 2.0V	T_r*	15pF load	-	0.9	2.0	ns
Fall Time 2.0 to 0.8V	T_f*	15pF load	-	0.7	1.5	ns
Rise Time 20% to 80%	T_r*	15pF load	-	1.8	3.25	ns
Fall Time 80% to 20%	T_f*	15pF load	-	1.4	2.5	ns
Duty Cycle	D_t*	15pF load @ 50% of VDD; Except REFCLK	45.0	50.0	55.0	%
Duty Cycle	D_t*	15pF load @ 50% of VDD; REFCLK only	40.0	53.0	60.0	%
Jitter, One Sigma	T_{jis}*	For all frequencies except REFCLK	-	100.0	150.0	ps
Jitter, Absolute	T_{jab}*	For all frequencies except REFCLK	-550.0	330.0	550.0	ps
Jitter, One Sigma	T_{jis}*	REFCLK only	-	350.0	500.0	ps
Jitter, Absolute	T_{jab}*	REFCLK only	-1200	750.0	1200	ps
Input Frequency	F_i*		11.0	14.0	17.0	MHz
Output Frequency	F_o*		11.0	-	42.0	MHz
Power-up Time	T_{pu}*	0 to 33.8 MHz	-	5.5	12.0	ms
Crystal Input Capacitance	C_{INX}*	X1 (Pin 1)	-	5	-	pF

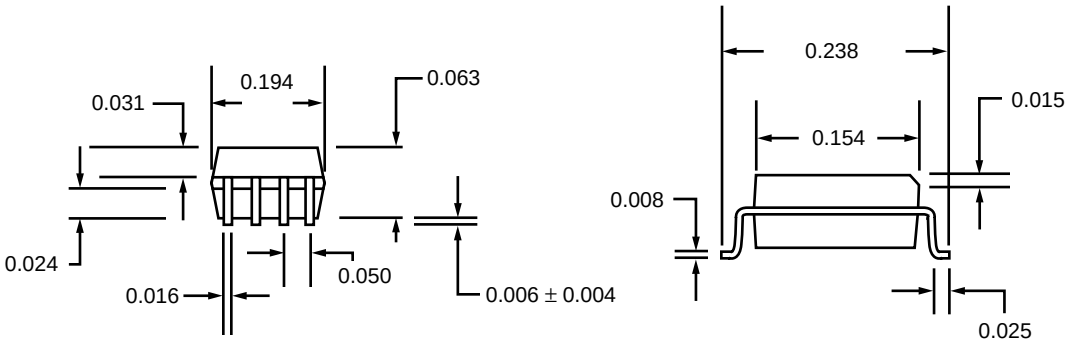
*Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

Operating V_{DD} = +3.0V to +3.7V; T_A =0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.2V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-8.0	-3.6	-	µA
Input High Current	I_{IH}	$V_{IN}=V_{DD}$	-	-	5.0	µA
Output Low Voltage	V_{OL}*	I_{OL}=6mA	-	$0.05V_{DD}$	0.1	V
Output High Voltage	V_{OH}*	I_{OH}=-4.0mA	$0.85V_{DD}$	$0.94V_{DD}$	-	V
Output Low Current	I_{OL}*	$V_{OL}=0.2V_{DD}$	15.0	24.0	-	mA
Output High Current	I_{OH}*	$V_{OH}=0.7V_{DD}$	-	-13.0	-8.0	mA
Supply Current	I_{DD}	Unloaded	-	14.0	32.0	mA
Supply Current, Power-down	I_{DD} (PD)	Unloaded	-	60.0	110.0	µA
Pull-up Resistor Valve	R_{pu}*		-	620.0	900.0	k ohm
AC Characteristics						
Rise Time 0.8 to 2.0V	T_r*	15pF load	-	1.5	4.0	ns
Fall Time 2.0 to 0.8V	T_f*	15pF load	-	1.0	3.0	ns
Rise Time 20% to 80%	T_r*	15pF load	-	2.2	4.0	ns
Fall Time 80% to 20%	T_f*	15pF load	-	1.5	3.0	ns
Duty Cycle	D_t*	15pF load @ 50% of VDD; REFCLK only	45.0	50.0	55.0	%
Duty Cycle	D_t*	15pF load @ 50% of VDD; Except REFCLK	40.0	45.0	60.0	%
Jitter, One Sigma	T_{jis}*	For all frequencies except REFCLK	-	140.0	200.0	ps
Jitter, Absolute	T_{jab}*	For all frequencies except REFCLK	-600.0	420.0	600.0	ps
Jitter, One Sigma	T_{jis}*	REFCLK only	-	230.0	400.0	ps
Jitter, Absolute	T_{jab}*	REFCLK only	-1000	600	1000	ps
Input Frequency	F_i*		11.0	14.3	15.0	MHz
Output Frequency	F_o*		11.0	-	38.0	MHz
Power-up Time	T_{pu}*	0 to 33.8 MHz	-	5.5	12.0	ms
Crystal Input Capacitance	C_{INX}*	X1 (Pin 1)	-	5	-	pF

*Parameter is guaranteed by design and characterization. Not 100% tested in production.



8-Pin SOIC Package

Ordering Information

ICS9120M-11

Example:

XXX XXXX M-PPP

Pattern Number (2 or 3-digit number for parts with ROM code patterns)

Package Type
N=DIP (Plastic)

Device Type (consists of 3 or 4-digit numbers)

Prefix
ICS, AV=Standard Device