



PRELIMINARY INFORMATION

ICS650-07C Networking Clock Source

Description

The ICS650-07C is a low cost, low jitter, high performance clock synthesizer for networking applications. Using analog Phase-Locked Loop (PLL) techniques, the device accepts a 12.5 MHz or 25.00 MHz clock or fundamental mode crystal input to produce multiple output clocks for networking chips, PCI devices, SDRAM, and ASICs. The ICS650-07C outputs all have 0 ppm synthesis error.

See the MK74CB214, ICS551, and ICS552-01 for non-PLL buffer devices which produce multiple low-skew copies of these output clocks.

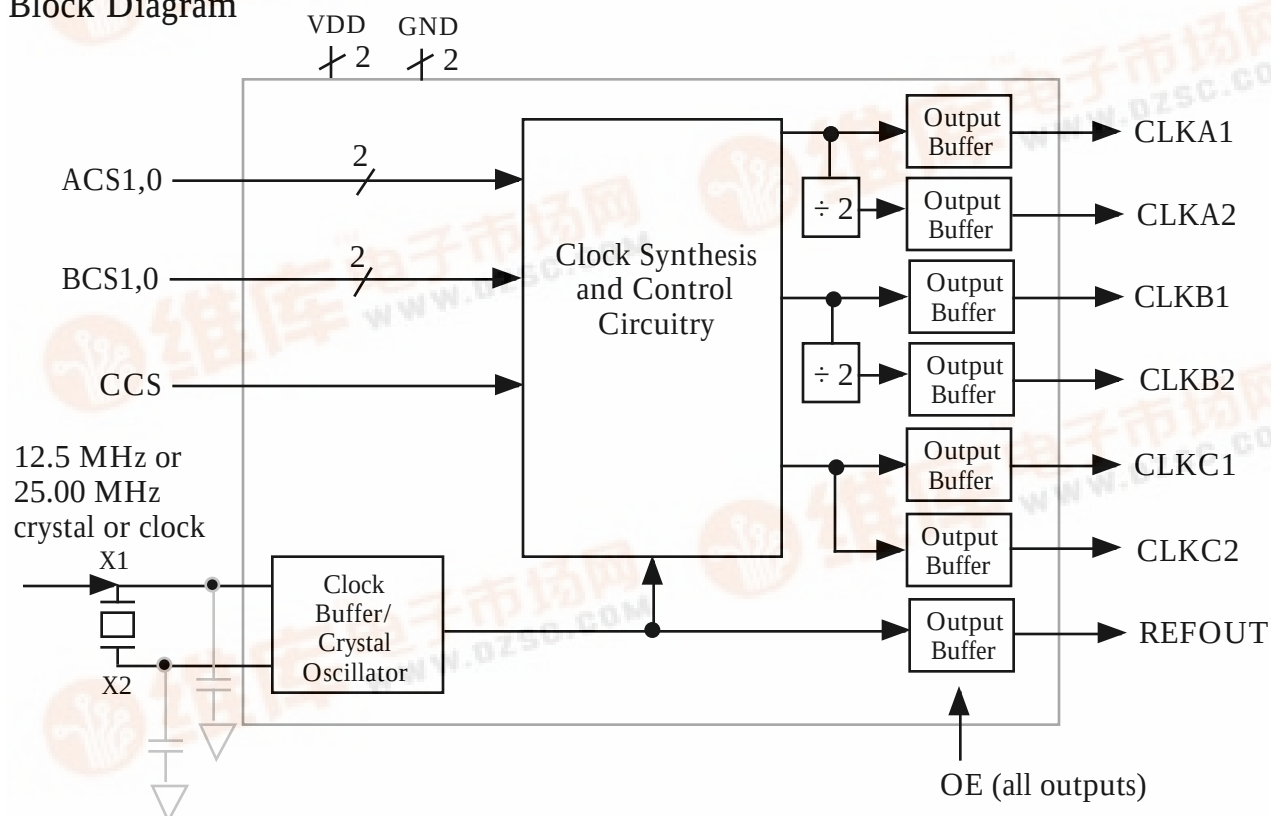
See the ICS570, ICS9112-16/17/18 for zero delay buffers that can synchronize outputs and other needed clocks.

Features

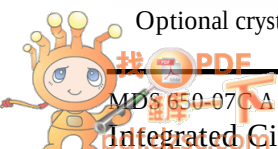


- Packaged in 20 pin narrow (150 mil) SSOP (QSOP)
- 12.5 MHz or 25.00 MHz fundamental crystal or clock input
- Six output clocks with selectable frequencies
- SDRAM frequencies of 67, 83, 100, and 133 MHz
- Buffered crystal reference output
- Zero ppm synthesis error in all clocks
- Ideal for PMC-Sierra's ATM switch chips
- Full CMOS output swing with 25 mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- 3.0V to 5.5V operating voltage

Block Diagram



Optional crystal capacitors are shown and may be required for tuning of initial accuracy (determined once per board).





For a 25 MHz fundamental crystal or clock input, the following four tables apply :

A Clocks Select Table (outputs in MHz)

ACS1	ACS0	CLKA1	CLKA2
0	0	100	off (low)
0	M	Test	Test
0	1	75	off (low)
1	0	33.3333	16.6667
1	M	Test	Test
1	1	66.6667	33.3333

B Clocks Select Table (outputs in MHz)

BCS1	BCS0	CLKB1	CLKB2
0	0	Test	Test
0	M	66.6667	33.3333
0	1	100	50
1	0	83.3333	41.6667
1	M	Test	Test
1	1	133.3333	66.6667

C Clocks Select Table (outputs in MHz)

CCS	CLKC1	CLKC2
0	125	125
M	Test	Test
1	75	75

REFOUT
25 MHz

0 = connect directly to GND

M = leave unconnected (automatically self biases to VDD/2)

1 = connect directly to VDD

For a 12.5 MHz crystal or clock input, the following four tables apply :

A Clocks Select Table (outputs in MHz)

ACS1	ACS0	CLKA1	CLKA2
0	0	50	off (low)
0	M	Test	Test
0	1	37.5	off (low)
1	0	16.6667	8.3333
1	M	Test	Test
1	1	33.3333	16.6667

B Clocks Select Table (outputs in MHz)

BCS1	BCS0	CLKB1	CLKB2
0	0	Test	Test
0	M	33.3333	16.6667
0	1	50	25
1	0	41.6667	20.8333
1	M	Test	Test
1	1	66.6667	33.3333

C Clocks Select Table (outputs in MHz)

CCS	CLKC1	CLKC2
0	62.5	62.5
M	Test	Test
1	37.5	37.5

REFOUT
12.5 MHz

0 = connect directly to GND

M = leave unconnected (automatically self biases to VDD/2)

1 = connect directly to VDD



Pin Assignment

ACS0	☐	1	20	☐	BCS1
X2	☐	2	19	☐	BCS0
X1/ICLK	☐	3	18	☐	REFOUT
VDD	☐	4	17	☐	CLKA1
ACS1	☐	5	16	☐	VDD
GND	☐	6	15	☐	OE
CLKC1	☐	7	14	☐	GND
CLKC2	☐	8	13	☐	CLKA2
CLKB2	☐	9	12	☐	DC
CLKB1	☐	10	11	☐	CCS

20 pin (150 mil) SSOP

Pin Descriptions

Number	Name	Type	Description
1	ACS0	TI	A Clock Select 0. Selects outputs on CLKA1 and CLKA2 per table on page 2.
2	X2	XO	Crystal connection. Connect to a crystal or leave unconnected for a clock input.
3	X1/ICLK	XI	Crystal connection. Connect to a fundamental crystal or clock input.
4	VDD	P	Connect to +3.3 V or +5 V. Must be same as other VDD.
5	ACS1	I	A Clock Select 1. Selects outputs on CLKA1 and CLKA2 per table on page 2.
6	GND	P	Connect to ground.
7	CLKC1	O	Clock C output 1. Depends on setting of CCS per table on page 2.
8	CLKC2	O	Clock C output 2. Depends on setting of CCS per table on page 2. Same as CLKC1.
9	CLKB2	O	Clock B output 2. Depends on setting of BCS1, 0 per table on page 2.
10	CLKB1	O	Clock B output 1. Depends on setting of BCS1, 0 per table on page 2.
11	CCS	TI	Clock C Select pin. Selects outputs on CLKC1 and CLKC2 per table on page 2.
12	DC	-	Don't Connect. Do not connect anything to this pin.
13	CLKA2	O	Clock A output 2. Depends on setting of ACS1, 0 per table on page 2.
14	GND	P	Connect to ground.
15	OE	I	Output Enable. Tri-states all outputs when low.
16	VDD	P	Connect to +3.3 V or +5 V. Must be same as other VDD.
17	CLKA1	O	Clock A output 1. Depends on setting of ACS1, 0 per table on page 2.
18	REFOUT	O	Buffered Reference clock Output. Same frequency as crystal or clock input.
19	BCS0	TI	B Clock Select 0. Selects outputs on CLKB1 and CLKB2 per table on page 2.
20	BCS1	I	B Clock Select 1. Selects outputs on CLKB1 and CLKB2 per table on page 2.

Key: TI = tri-level input; XI, XO = crystal connections; I = Input with internal pull-up resistor;
O = Output; P = power supply connection



Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Ambient Operating Temperature, I version	Industrial temp	-40		85	°C
Soldering Temperature	Max of 20 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 5.0V unless noted)					
Operating Voltage, VDD		3		5.5	V
Input High Voltage, VIH, X1 pin only	Clock input	VDD/2 + 1	VDD/2		V
Input Low Voltage, VIL, X1 pin only	Clock input		VDD/2	VDD/2 - 1	V
Input High Voltage, VIH, all TI type inputs		VDD-0.5			V
Input Low Voltage, VIL, all TI type inputs				0.5	V
Input High Voltage, VIH, all I type inputs		2			V
Input Low Voltage, VIL, all I type inputs				0.8	V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-8mA	VDD-0.4			V
Operating Supply Current, IDD	No Load		60		mA
Short Circuit Current	Each output		±100		mA
Internal pull-up resistor	ACS1, BCS1, OE		200		kΩ
AC CHARACTERISTICS (VDD = 5.0V unless noted)					
Input Frequency		10	12.5 or 25	27	MHz
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	At VDD/2	40	50	60	%
Frequency error	All clocks			0	ppm
Absolute Jitter, short term	Variation from mean		150		ps

Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.

External Components

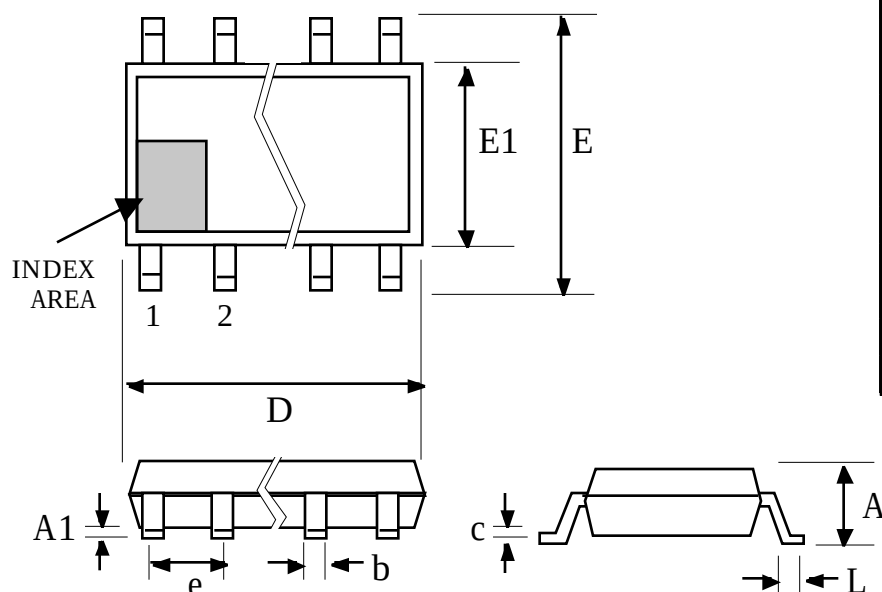
The ICS650-07C requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01μF should be connected between each VDD and GND (pins 4 and 6, pins 16 and 14), as close to the ICS650-07 as possible. A series termination resistor of 33 Ω may be used for each clock output. The crystal must be connected as close to the chip as possible. The crystal should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation, where C_L is the crystal load capacitance: Crystal caps (pF) = $(C_L - 6) \times 2$. So for a crystal with 16 pF load capacitance, two 20 pF caps should be used.



Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)

20 pin SSOP



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.19	0.25
D	0.337	0.344	8.56	8.74
e	.025 BSC		0.635 BSC	
E	0.228	0.244	5.79	6.20
E1	0.150	0.157	3.81	3.99
L	0.016	0.050	0.41	1.27

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
ICS650R-07	ICS650R-07	tubes	20 pin SSOP	0-70°C
ICS650R-07T	ICS650R-07	tape and reel	20 pin SSOP	0-70°C
ICS650R-07I	ICS650R-07I	tubes	20 pin SSOP	-40 to +85°C
ICS650R-07IT	ICS650R-07I	tape and reel	20 pin SSOP	-40 to +85°C

Note: The C on the data sheet (ICS650-07C) is not significant when ordering this chip.

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