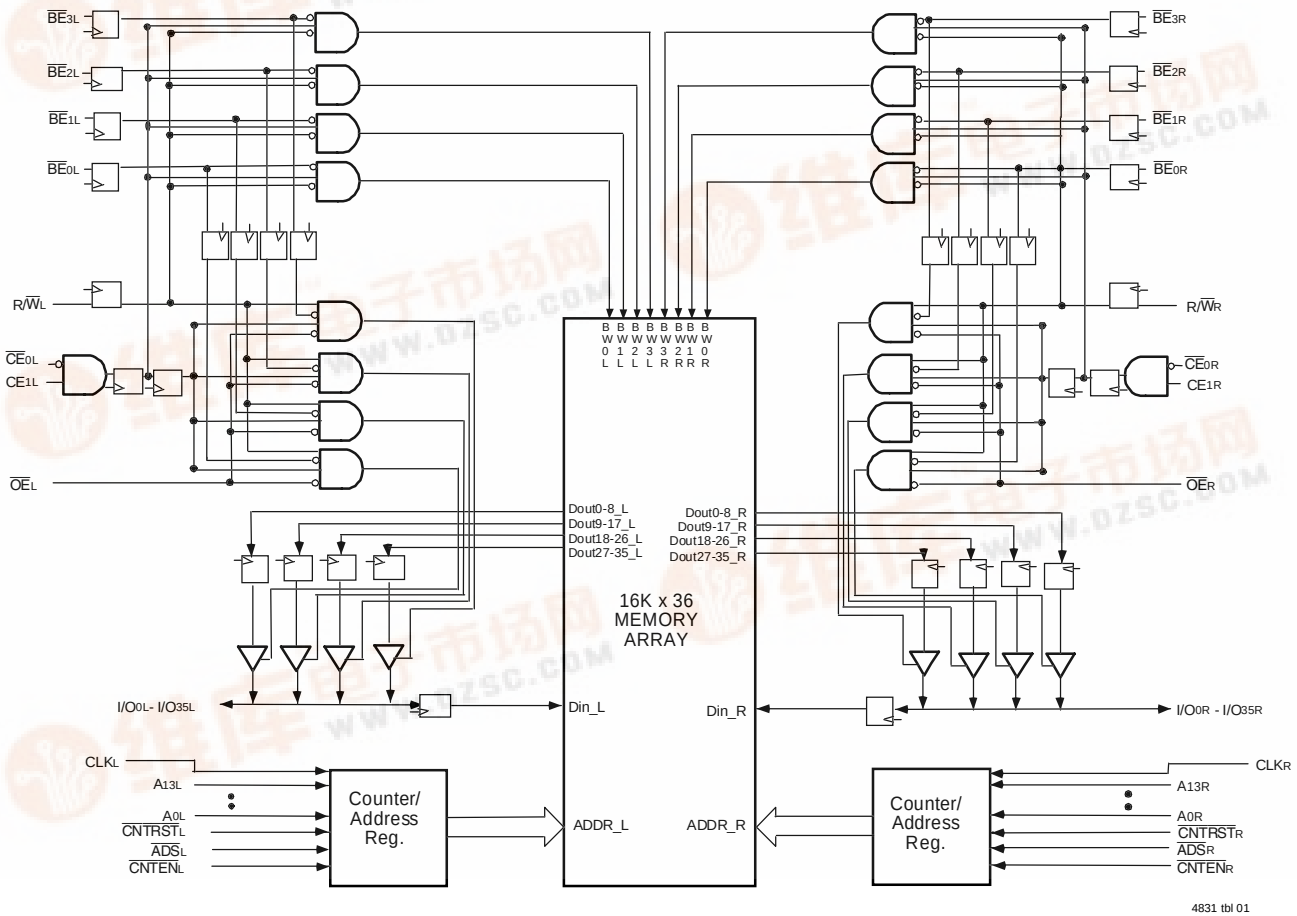
HIGH-SPEED 3.3V 16K x 36 SYNCHRONOUS PIPELINED DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

IDT70V3569S

Features:

- True Dual-Port memory cells which allow simultaneous access of the same memory location
- High-speed clock to data access
  - *Commercial: 4.2/5/6ns (max.)*
  - *Industrial: 5/6ns (max)*
- Pipelined output mode
- Counter enable and reset features
- Dual chip enables allow for depth expansion without additional logic
- Full synchronous operation on both ports
  - *7.5ns cycle time, 133MHz operation (9.6 Gbps bandwidth)*
  - *Fast 4.2ns clock to data out*
  - *1.8ns setup to clock and 0.7ns hold on all control, data, and address inputs @ 133MHz*
  - *Data input, address, byte enable and control registers*
  - *Self-timed write allows fast cycle time*
- Separate byte controls for multiplexed bus and bus matching compatibility
- LVTTL- compatible, single 3.3V (±150mV) power supply for core
- LVTTL- compatible, selectable 3.3V (±150mV)/2.5V (±125mV) power supply for I/Os and control signals on each port
- Industrial temperature range (-40°C to +85°C) is available for selected speeds
- Available in a 208-pin Plastic Quad Flatpack (PQFP), 208-ball fine-pitch Ball Grid Array, and 256-pin Ball Grid Array

Functional Block Diagram



Description:

The IDT70V3569 is a high-speed 16K x 36 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70V3569 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and CE_1, permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70V3569 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (V_{DD}) remains at 3.3V.

Pin Configuration[1,2,3,4]

A1 IO_{19L}	A2 IO_{18L}	A3 V_{SS}	A4 NC	A5 NC	A6 NC	A7 A_{12L}	A8 A_{8L}	A9 $\overline{BE}_{1L}$	A10 V_{DD}	A11 CLK_L	A12 $\overline{CNTEN}_L$	A13 A_{4L}	A14 A_{0L}	A15 OPT_L	A16 I/O_{17L}	A17 V_{SS}
B1 I/O_{20R}	B2 V_{SS}	B3 I/O_{18R}	B4 V_{SS}	B5 NC	B6 A_{13L}	B7 A_{9L}	B8 $\overline{BE}_{2L}$	B9 $\overline{CE}_{0L}$	B10 V_{SS}	B11 $\overline{ADS}_L$	B12 A_{5L}	B13 A_{1L}	B14 V_{SS}	B15 V_{DDQR}	B16 I/O_{16L}	B17 I/O_{15R}
C1 V_{DDQL}	C2 I/O_{19R}	C3 V_{DDQR}	C4 V_{DD}	C5 NC	C6 NC	C7 A_{10L}	C8 $\overline{BE}_{3L}$	C9 CE_{1L}	C10 V_{SS}	C11 $R/\overline{W}_L$	C12 A_{6L}	C13 A_{2L}	C14 V_{DD}	C15 I/O_{16R}	C16 I/O_{15L}	C17 V_{SS}
D1 I/O_{22L}	D2 V_{SS}	D3 I/O_{21L}	D4 I/O_{20L}	D5 NC	D6 A_{11L}	D7 A_{7L}	D8 $\overline{BE}_{0L}$	D9 V_{DD}	D10 $\overline{OE}_L$	D11 $\overline{CNTRST}_L$	D12 A_{3L}	D13 V_{DD}	D14 I/O_{17R}	D15 V_{DDQL}	D16 I/O_{14L}	D17 I/O_{14R}
E1 I/O_{23L}	E2 I/O_{22R}	E3 V_{DDQR}	E4 I/O_{21R}										E14 I/O_{12L}	E15 I/O_{13R}	E16 V_{SS}	E17 I/O_{13L}
F1 V_{DDQL}	F2 I/O_{23R}	F3 I/O_{24L}	F4 V_{SS}										F14 V_{SS}	F15 I/O_{12R}	F16 I/O_{11L}	F17 V_{DDQR}
G1 I/O_{26L}	G2 V_{SS}	G3 I/O_{25L}	G4 I/O_{24R}										G14 I/O_{9L}	G15 V_{DDQL}	G16 I/O_{10L}	G17 I/O_{11R}
H1 V_{DD}	H2 I/O_{26R}	H3 V_{DDQR}	H4 I/O_{25R}										H14 V_{DD}	H15 IO_{9R}	H16 V_{SS}	H17 I/O_{10R}
J1 V_{DDQL}	J2 V_{DD}	J3 V_{SS}	J4 V_{SS}										J14 V_{SS}	J15 V_{DD}	J16 V_{SS}	J17 V_{DDQR}
K1 I/O_{28R}	K2 V_{SS}	K3 I/O_{27R}	K4 V_{SS}										K14 I/O_{7R}	K15 V_{DDQL}	K16 I/O_{8R}	K17 V_{SS}
L1 I/O_{29R}	L2 I/O_{28L}	L3 V_{DDQR}	L4 I/O_{27L}										L14 I/O_{6R}	L15 I/O_{7L}	L16 V_{SS}	L17 I/O_{8L}
M1 V_{DDQL}	M2 I/O_{29L}	M3 I/O_{30R}	M4 V_{SS}										M14 V_{SS}	M15 I/O_{6L}	M16 I/O_{5R}	M17 V_{DDQR}
N1 I/O_{31L}	N2 V_{SS}	N3 I/O_{31R}	N4 I/O_{30L}										N14 I/O_{3R}	N15 V_{DDQL}	N16 I/O_{4R}	N17 I/O_{5L}
P1 I/O_{32R}	P2 I/O_{32L}	P3 V_{DDQR}	P4 I/O_{35R}	P5 NC	P6 NC	P7 A_{12R}	P8 A_{8R}	P9 $\overline{BE}_{1R}$	P10 V_{DD}	P11 CLK_R	P12 $\overline{CNTEN}_R$	P13 A_{4R}	P14 I/O_{2L}	P15 I/O_{3L}	P16 V_{SS}	P17 I/O_{4L}
R1 V_{SS}	R2 I/O_{33L}	R3 I/O_{34R}	R4 NC	R5 NC	R6 A_{13R}	R7 A_{9R}	R8 $\overline{BE}_{2R}$	R9 $\overline{CE}_{0R}$	R10 V_{SS}	R11 $\overline{ADS}_R$	R12 A_{5R}	R13 A_{1R}	R14 V_{SS}	R15 V_{DDQL}	R16 I/O_{1R}	R17 V_{DDQR}
T1 I/O_{33R}	T2 I/O_{34L}	T3 V_{DDQL}	T4 V_{SS}	T5 NC	T6 NC	T7 A_{10R}	T8 $\overline{BE}_{3R}$	T9 CE_{1R}	T10 V_{SS}	T11 $R/\overline{W}_R$	T12 A_{6R}	T13 A_{2R}	T14 V_{SS}	T15 I/O_{0R}	T16 V_{SS}	T17 I/O_{2R}
U1 V_{SS}	U2 I/O_{35L}	U3 V_{DD}	U4 NC	U5 NC	U6 A_{11R}	U7 A_{7R}	U8 $\overline{BE}_{0R}$	U9 V_{DD}	U10 $\overline{OE}_R$	U11 $\overline{CNTRST}_R$	U12 A_{3R}	U13 A_{0R}	U14 V_{DD}	U15 OPT_R	U16 I/O_{0L}	U17 I/O_{1L}

70V3569BF
BF-208[5]

208-Pin fpBGA
Top View[6]

4831 drw 02c

NOTES:

1. All V_{DD} pins must be connected to 3.3V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
3. All V_{SS} pins must be connected to ground supply.
4. Package body is approximately 15mm x 15mm x 1.4mm, with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration[1,2,3,4] (con't.)

70V3569BC
BC-256[5]

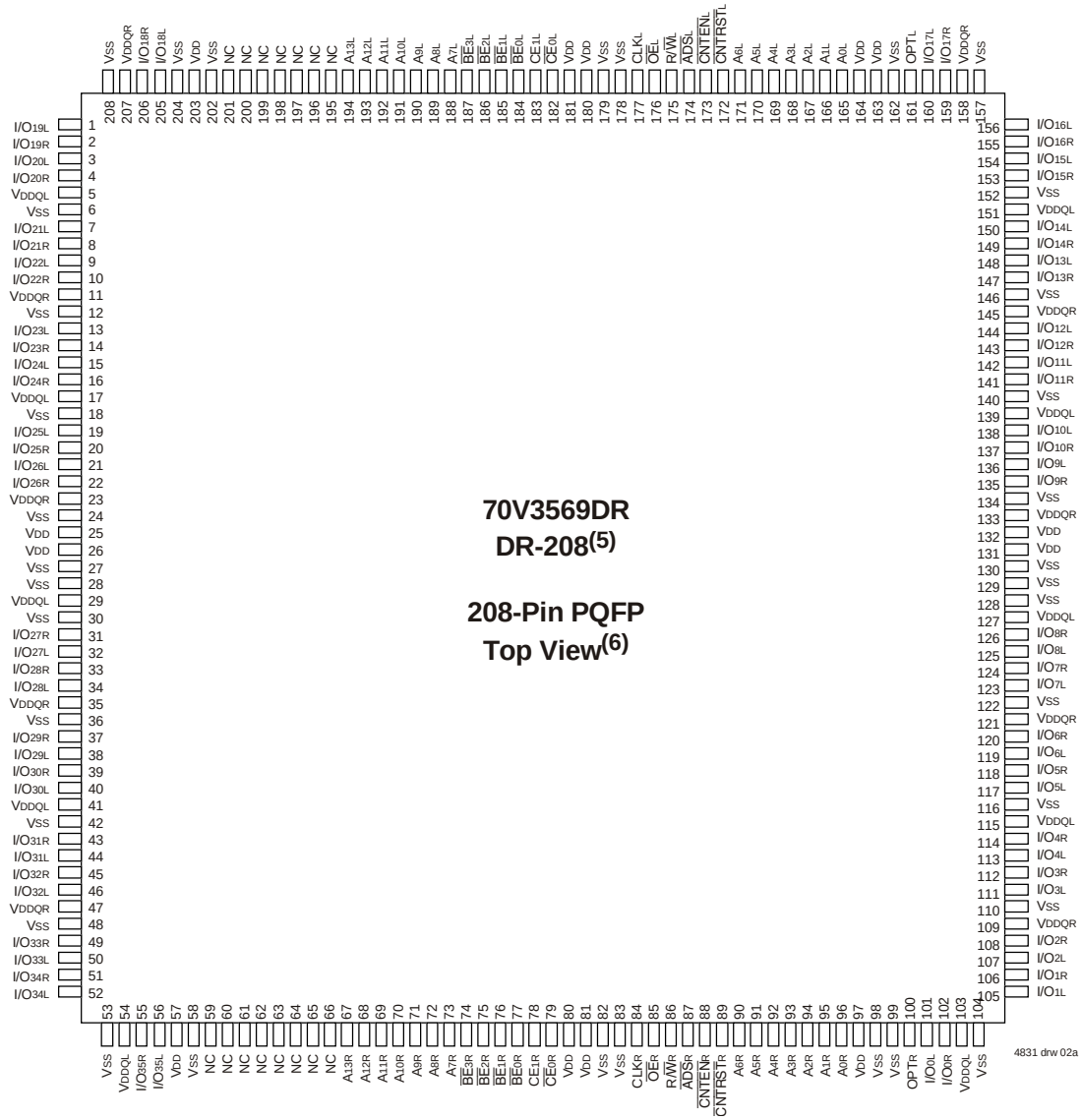
256-Pin BGA
Top View[6]

A1 NC	A2 NC	A3 NC	A4 NC	A5 NC	A6 A_{11L}	A7 A_{8L}	A8 $\overline{BE}_{2L}$	A9 CE_{1L}	A10 $\overline{OE}_L$	A11 $\overline{CNTEN}_L$	A12 A_{5L}	A13 A_{2L}	A14 A_{0L}	A15 NC	A16 NC
B1 I/O_{18L}	B2 NC	B3 NC	B4 NC	B5 NC	B6 A_{12L}	B7 A_{9L}	B8 $\overline{BE}_{3L}$	B9 $\overline{CE}_{0L}$	B10 $R/\overline{W}_L$	B11 $\overline{CNTRST}_L$	B12 A_{4L}	B13 A_{1L}	B14 V_{DD}	B15 I/O_{17L}	B16 NC
C1 I/O_{18R}	C2 I/O_{19L}	C3 V_{SS}	C4 NC	C5 A_{13L}	C6 A_{10L}	C7 A_{7L}	C8 $\overline{BE}_{1L}$	C9 $\overline{BE}_{0L}$	C10 CLK_L	C11 $\overline{ADS}_L$	C12 A_{6L}	C13 A_{3L}	C14 OPT_L	C15 I/O_{17R}	C16 I/O_{16L}
D1 I/O_{20R}	D2 I/O_{19R}	D3 I/O_{20L}	D4 V_{DD}	D5 V_{DDQL}	D6 V_{DDQL}	D7 V_{DDQR}	D8 V_{DDQR}	D9 V_{DDQL}	D10 V_{DDQL}	D11 V_{DDQR}	D12 V_{DDQR}	D13 V_{DD}	D14 I/O_{15R}	D15 I/O_{15L}	D16 I/O_{16R}
E1 I/O_{21R}	E2 I/O_{21L}	E3 I/O_{22L}	E4 V_{DDQL}	E5 V_{DD}	E6 V_{DD}	E7 V_{SS}	E8 V_{SS}	E9 V_{SS}	E10 V_{SS}	E11 V_{DD}	E12 V_{DD}	E13 V_{DDQR}	E14 I/O_{13L}	E15 I/O_{14L}	E16 I/O_{14R}
F1 I/O_{23L}	F2 I/O_{22R}	F3 I/O_{23R}	F4 V_{DDQL}	F5 V_{DD}	F6 V_{SS}	F7 V_{SS}	F8 V_{SS}	F9 V_{SS}	F10 V_{SS}	F11 V_{SS}	F12 V_{DD}	F13 V_{DDQR}	F14 I/O_{12R}	F15 I/O_{13R}	F16 I/O_{12L}
G1 I/O_{24R}	G2 I/O_{24L}	G3 I/O_{25L}	G4 V_{DDQR}	G5 V_{SS}	G6 V_{SS}	G7 V_{SS}	G8 V_{SS}	G9 V_{SS}	G10 V_{SS}	G11 V_{SS}	G12 V_{SS}	G13 V_{DDQL}	G14 I/O_{10L}	G15 I/O_{11L}	G16 I/O_{11R}
H1 I/O_{26L}	H2 I/O_{25R}	H3 I/O_{26R}	H4 V_{DDQR}	H5 V_{SS}	H6 V_{SS}	H7 V_{SS}	H8 V_{SS}	H9 V_{SS}	H10 V_{SS}	H11 V_{SS}	H12 V_{SS}	H13 V_{DDQL}	H14 I/O_{9R}	H15 IO_{9L}	H16 I/O_{10R}
J1 I/O_{27L}	J2 I/O_{28R}	J3 I/O_{27R}	J4 V_{DDQL}	J5 V_{SS}	J6 V_{SS}	J7 V_{SS}	J8 V_{SS}	J9 V_{SS}	J10 V_{SS}	J11 V_{SS}	J12 V_{SS}	J13 V_{DDQR}	J14 I/O_{8R}	J15 I/O_{7R}	J16 I/O_{8L}
K1 I/O_{29R}	K2 I/O_{29L}	K3 I/O_{28L}	K4 V_{DDQL}	K5 V_{SS}	K6 V_{SS}	K7 V_{SS}	K8 V_{SS}	K9 V_{SS}	K10 V_{SS}	K11 V_{SS}	K12 V_{SS}	K13 V_{DDQR}	K14 I/O_{6R}	K15 I/O_{6L}	K16 I/O_{7L}
L1 I/O_{30L}	L2 I/O_{31R}	L3 I/O_{30R}	L4 V_{DDQR}	L5 V_{DD}	L6 V_{SS}	L7 V_{SS}	L8 V_{SS}	L9 V_{SS}	L10 V_{SS}	L11 V_{SS}	L12 V_{DD}	L13 V_{DDQL}	L14 I/O_{5L}	L15 I/O_{4R}	L16 I/O_{5R}
M1 I/O_{32R}	M2 I/O_{32L}	M3 I/O_{31L}	M4 V_{DDQR}	M5 V_{DD}	M6 V_{DD}	M7 V_{SS}	M8 V_{SS}	M9 V_{SS}	M10 V_{SS}	M11 V_{DD}	M12 V_{DD}	M13 V_{DDQL}	M14 I/O_{3R}	M15 I/O_{3L}	M16 I/O_{4L}
N1 I/O_{33L}	N2 I/O_{34R}	N3 I/O_{33R}	N4 V_{DD}	N5 V_{DDQR}	N6 V_{DDQR}	N7 V_{DDQL}	N8 V_{DDQL}	N9 V_{DDQR}	N10 V_{DDQR}	N11 V_{DDQL}	N12 V_{DDQL}	N13 V_{DD}	N14 I/O_{2L}	N15 I/O_{1R}	N16 I/O_{2R}
P1 I/O_{35R}	P2 I/O_{34L}	P3 NC	P4 NC	P5 A_{13R}	P6 A_{10R}	P7 A_{7R}	P8 $\overline{BE}_{1R}$	P9 $\overline{BE}_{0R}$	P10 CLK_R	P11 $\overline{ADS}_R$	P12 A_{6R}	P13 A_{3R}	P14 I/O_{0L}	P15 I/O_{0R}	P16 I/O_{1L}
R1 I/O_{35L}	R2 NC	R3 NC	R4 NC	R5 NC	R6 A_{12R}	R7 A_{9R}	R8 $\overline{BE}_{3R}$	R9 $\overline{CE}_{0R}$	R10 $R/\overline{W}_R$	R11 $\overline{CNTRST}_R$	R12 A_{4R}	R13 A_{1R}	R14 OPT_R	R15 NC	R16 NC
T1 NC	T2 NC	T3 NC	T4 NC	T5 NC	T6 A_{11R}	T7 A_{8R}	T8 $\overline{BE}_{2R}$	T9 CE_{1R}	T10 $\overline{OE}_R$	T11 $\overline{CNTEN}_R$	T12 A_{5R}	T13 A_{2R}	T14 A_{0R}	T15 NC	T16 NC

4831 drw 02d

NOTES:
1. All V_{DD} pins must be connected to 3.3V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
3. All V_{SS} pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration[1,2,3,4] (con't.)



NOTES:

1. All V_{DD} pins must be connected to 3.3V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
3. All V_{SS} pins must be connected to ground supply.
4. Package body is approximately 28mm x 28mm x 3.5mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables
R/$\overline{W}_L$	R/$\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{13L}	A_{0R} - A_{13R}	Address
I/O_{0L} - I/O_{35L}	I/O_{0R} - I/O_{35R}	Data Input/Output
CLK_L	CLK_R	Clock
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter Reset
$\overline{BE}_{0L}$ - $\overline{BE}_{3L}$	$\overline{BE}_{0R}$ - $\overline{BE}_{3R}$	Byte Enables (9-bit bytes)
V_{DDQL}	V_{DDQR}	Power (I/O Bus) (3.3V or 2.5V)(1)
OPT_L	OPT_R	Option for selection V_{DDQX}(1,2)
V_{DD}		Power (3.3V)(1)
V_{SS}		Ground (0V)

4831 tbl 01

NOTES:
1. V_{DD}, OPT_X, and V_{DDQX} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
2. OPT_X selects the operating voltage levels for the I/Os and controls on that port. If OPT_X is set to VIH (3.3V), then that port's I/Os and controls will operate at 3.3V levels and V_{DDQX} must be supplied at 3.3V. If OPT_X is set to VIL (0V), then that port's I/Os and controls will operate at 2.5V levels and V_{DDQX} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.

Truth Table I—Read/Write and Enable Control(1,2,3,4)

$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	$\overline{BE}_3$	$\overline{BE}_2$	$\overline{BE}_1$	$\overline{BE}_0$	R/$\overline{W}$	Byte 3 I/O_{27-35}	Byte 2 I/O_{18-26}	Byte 1 I/O_{9-17}	Byte 0 I/O_{0-8}	MODE
X	↑	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected–Power Down
X	↑	X	L	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected–Power Down
X	↑	L	H	H	H	H	H	X	High-Z	High-Z	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	H	H	L	L	High-Z	High-Z	High-Z	D_{IN}	Write to Byte 0 Only
X	↑	L	H	H	H	L	H	L	High-Z	High-Z	D_{IN}	High-Z	Write to Byte 1 Only
X	↑	L	H	H	L	H	H	L	High-Z	D_{IN}	High-Z	High-Z	Write to Byte 2 Only
X	↑	L	H	L	H	H	H	L	D_{IN}	High-Z	High-Z	High-Z	Write to Byte 3 Only
X	↑	L	H	H	H	L	L	L	High-Z	High-Z	D_{IN}	D_{IN}	Write to Lower 2 Bytes Only
X	↑	L	H	L	L	H	H	L	D_{IN}	D_{IN}	High-Z	High-Z	Write to Upper 2 bytes Only
X	↑	L	H	L	L	L	L	L	D_{IN}	D_{IN}	D_{IN}	D_{IN}	Write to All Bytes
L	↑	L	H	H	H	H	L	H	High-Z	High-Z	High-Z	D_{OUT}	Read Byte 0 Only
L	↑	L	H	H	H	L	H	H	High-Z	High-Z	D_{OUT}	High-Z	Read Byte 1 Only
L	↑	L	H	H	L	H	H	H	High-Z	D_{OUT}	High-Z	High-Z	Read Byte 2 Only
L	↑	L	H	L	H	H	H	H	D_{OUT}	High-Z	High-Z	High-Z	Read Byte 3 Only
L	↑	L	H	H	H	L	L	H	High-Z	High-Z	D_{OUT}	D_{OUT}	Read Lower 2 Bytes Only
L	↑	L	H	L	L	H	H	H	D_{OUT}	D_{OUT}	High-Z	High-Z	Read Upper 2 Bytes Only
L	↑	L	H	L	L	L	L	H	D_{OUT}	D_{OUT}	D_{OUT}	D_{OUT}	Read All Bytes
H	↑	L	H	L	L	L	L	X	High-Z	High-Z	High-Z	High-Z	Outputs Disabled

4831 tbl 02

NOTES:
1. "H" = VIH, "L" = VIL, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = VIH.
3. OE is an asynchronous input signal.
4. It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

Truth Table II—Address Counter Control(1,2)

Address	Previous Address	Addr Used	CLK(6)	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{CNTRST}$	I/O(3)	MODE
X	X	0	↑	X	X	L(4)	DI/O(0)	Counter Reset to Address 0
An	X	An	↑	L(4)	X	H	DI/O (n)	External Address Used
An	Ap	Ap	↑	H	H	H	DI/O(p)	External Address Blocked—Counter disabled (Ap reused)
X	Ap	Ap + 1	↑	H	L(5)	H	DI/O(p+1)	Counter Enabled—Internal Address generation

4831 tbl 03

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. Read and write operations are controlled by the appropriate setting of R/$\overline{W}$, $\overline{CE}_0$, CE_1, $\overline{BE}$n and $\overline{OE}$.
3. Outputs are in Pipelined mode: the data out will be delayed by one cycle.
4. $\overline{ADS}$ and $\overline{CNTRST}$ are independent of all other memory control signals including $\overline{CE}_0$, CE_1 and $\overline{BE}$n
5. The address counter advances if $\overline{CNTEN}$ = V_{IL} on the rising edge of CLK, regardless of all other memory control signals including $\overline{CE}_0$, CE_1, $\overline{BE}$n.

Recommended Operating Temperature and Supply Voltage(1,2)

Grade	Ambient Temperature	GND	V_{DD}
Commercial	0°C to +70°C	0V	3.3V ± 150mV
Industrial	-40°C to +85°C	0V	3.3V ± 150mV

4831 tbl 04

NOTES:
1. Industrial temperature: for specific speeds, packages and powers contact your sales office.
2. This is the parameter T_A. This is the "instant on" case temperature.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	50	mA

4831 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{DD} + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ V_{DD} + 150mV.

Recommended DC Operating Conditions with V_{DDQ} at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V_{DDQ}	I/O Supply Voltage(3)	2.375	2.5	2.625	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage(3) (Address & Control Inputs)	1.7	—	V_{DDQ} + 125mV(2)	V
V_{IH}	Input High Voltage - I/O(3)	1.7	—	V_{DDQ} + 125mV(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.7	V

4831 tbl 05a

NOTES:
1. V_{IL} ≥ -1.5V for pulse width less than 10 ns.
2. V_{TERM} must not exceed V_{DDQ} + 125mV.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IL} (0V), and V_{DDQX} for that port must be supplied as indicated above.

Recommended DC Operating Conditions with V_{DDQ} at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V_{DDQ}	I/O Supply Voltage(3)	3.15	3.3	3.45	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage (Address & Control Inputs)(3)	2.0	—	V_{DDQ} + 150mV(2)	V
V_{IH}	Input High Voltage - I/O(3)	2.0	—	V_{DDQ} + 150mV(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V

4831 tbl 05b

NOTES:
1. V_{IL} ≥ -1.5V for pulse width less than 10 ns.
2. V_{TERM} must not exceed V_{DDQ} + 150mV.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IH} (3.3V), and V_{DDQX} for that port must be supplied as indicated above.

Capacitance[1]

(T_A = +25°C, F = 1.0MHz) PQFP ONLY

Symbol	Parameter	Conditions[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
C_{OUT}[3]	Output Capacitance	V_{OUT} = 3dV	10.5	pF

4831 tbl 07

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C_{OUT} also references $C_{I/O}$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Conditions	70V3569S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{DDQ} = Max., V_{IN} = 0V to V_{DDQ}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL}, V_{OUT} = 0V to V_{DDQ}	—	10	µA
V_{OL} (3.3V)	Output Low Voltage[2]	I_{OL} = +4mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (3.3V)	Output High Voltage[2]	I_{OH} = -4mA, V_{DDQ} = Min.	2.4	—	V
V_{OL} (2.5V)	Output Low Voltage[2]	I_{OL} = +2mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (2.5V)	Output High Voltage[2]	I_{OH} = -2mA, V_{DDQ} = Min.	2.0	—	V

4831 tbl 08

NOTE:
1. At V_{DD} ≤ - 2.0V input leakages are undefined.
2. V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to p.4 for details.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[3] (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Condition	Version		70V3569S4 Com'l Only		70V3569S5 Com'l & Ind		70V3569S6 Com'l & Ind		Unit
					Typ.[4]	Max.	Typ.[4]	Max.	Typ.[4]	Max.	
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL}, Outputs Disabled, f = f_{MAX}[1]	COM'L	S	375	460	285	360	245	310	mA
			IND	S	—	—	285	415	245	360	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} f = f_{MAX}[1]	COM'L	S	145	190	105	145	95	125	mA
			IND	S	—	—	105	175	95	150	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Disabled, f=f_{MAX}[1]	COM'L	S	265	325	190	260	175	225	mA
			IND	S	—	—	190	300	175	260	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{DD} - 0.2V, V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, f = 0[2]	COM'L	S	6	15	6	15	6	15	mA
			IND	S	—	—	6	30	6	30	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{DD} - 0.2V[5] V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, Active Port, Outputs Disabled, f = f_{MAX}[1]	COM'L	S	265	325	180	260	170	225	mA
			IND	S	—	—	180	300	170	260	

4831 tbl 09

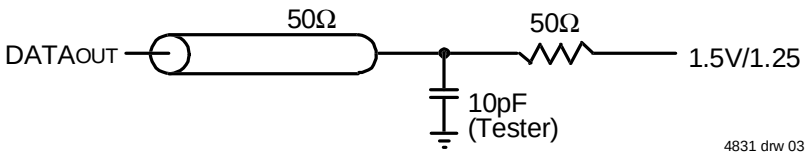
NOTES:

1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{DD} = 3.3V, T_A = 25°C for Typ, and are not production tested. $I_{DD\,DC}$(f=0) = 120mA (Typ).
5. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE_{1X} = V_{IL}
   $\overline{CE}_X$ ≤ 0.2V means $\overline{CE}_{0X}$ ≤ 0.2V and CE_{1X} ≥ V_{CC} - 0.2V
   $\overline{CE}_X$ ≥ V_{CC} - 0.2V means $\overline{CE}_{0X}$ ≥ V_{CC} - 0.2V or CE_{1X} - 0.2V
   "X" represents "L" for left port or "R" for right port.

AC Test Conditions

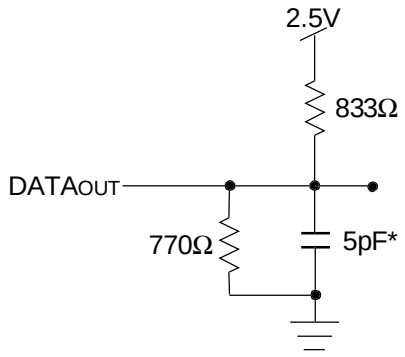
Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.35V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.35V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1, 2, and 3

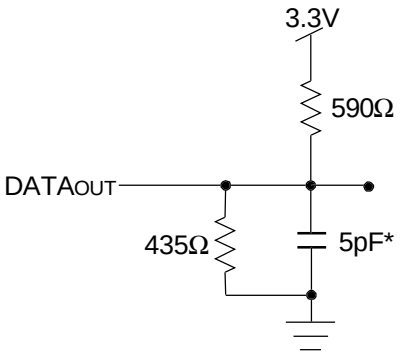
4831 tbl 10



4831 drw 03

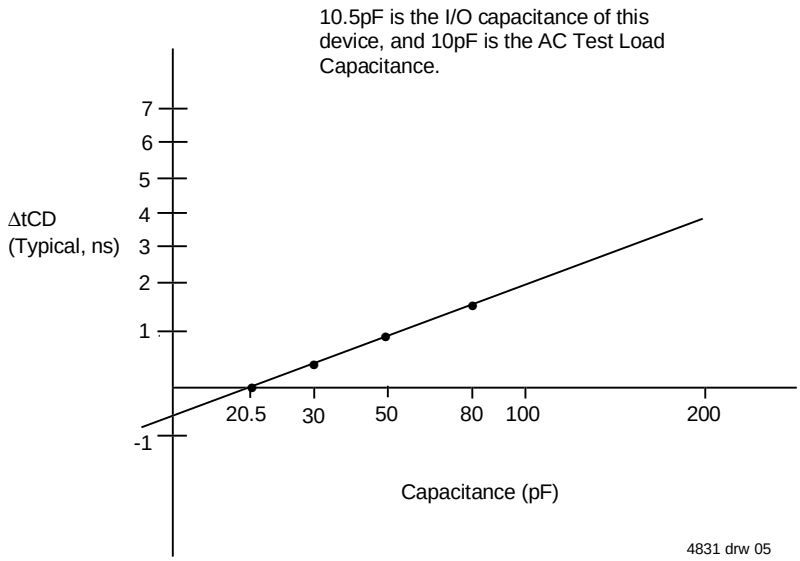
Figure 1. AC Output Test load.





4831 drw 04

Figure 2. Output Test Load (For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ}).
*Including scope and jig.



4831 drw 05

Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)[1,2]

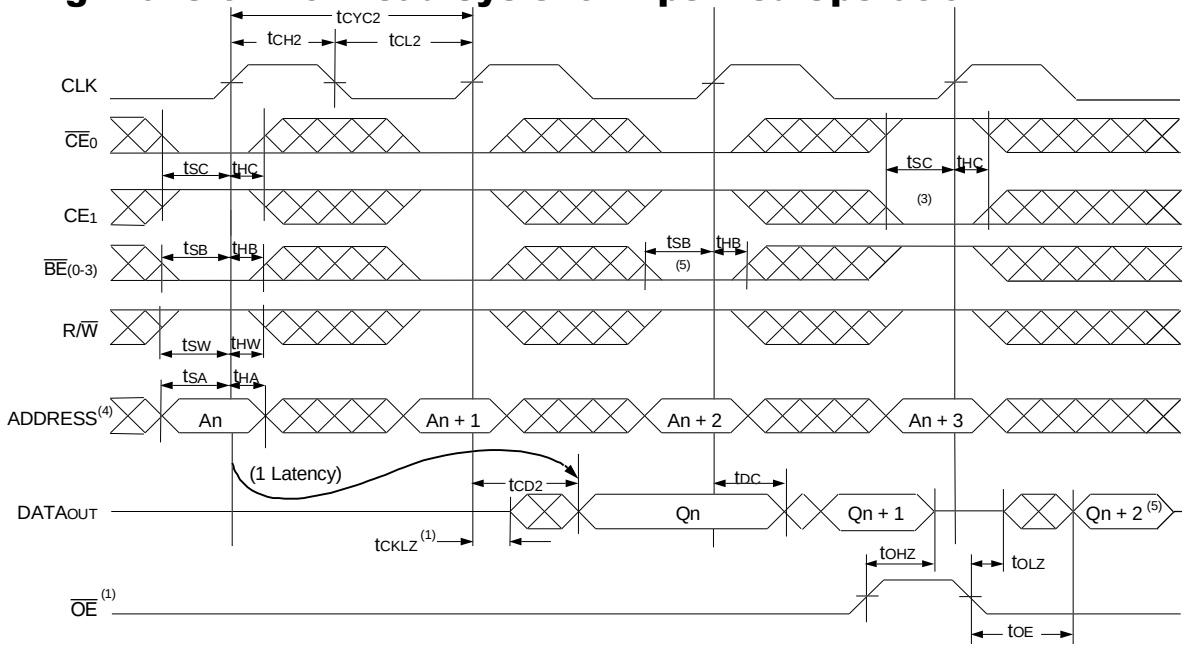
(V_{DD} = 3.3V ± 150mV, T_A = 0°C to +70°C)

Symbol	Parameter	70V3569S4 Com'l Only		70V3569S5 Com'l & Ind		70V3569S6 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC2}	Clock Cycle Time (Pipelined)	7.5	—	10	—	12	—	ns
t_{CH2}	Clock High Time (Pipelined)	3	—	4	—	5	—	ns
t_{CL2}	Clock Low Time (Pipelined)	3	—	4	—	5	—	ns
t_R	Clock Rise Time	—	3	—	3	—	3	ns
t_F	Clock Fall Time	—	3	—	3	—	3	ns
t_{SA}	Address Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HA}	Address Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SC}	Chip Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HC}	Chip Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SB}	Byte Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HB}	Byte Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SW}	R/$\overline{W}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HW}	R/$\overline{W}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SD}	Input Data Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HD}	Input Data Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SAD}	$\overline{ADS}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HAD}	$\overline{ADS}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SRST}	$\overline{CNTRST}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HRST}	$\overline{CNTRST}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{OE}[1]	Output Enable to Data Valid	—	4	—	5	—	6	ns
t_{OLZ}	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
t_{OHZ}	Output Enable to Output High-Z	1	4	1	4.5	1	5	ns
t_{CD2}	Clock to Data Valid (Pipelined)	—	4.2	—	5	—	6	ns
t_{DC}	Data Output Hold After Clock High	1	—	1	—	1	—	ns
t_{CKHZ}	Clock High to Output High-Z	1	3	1	4.5	1.5	6	ns
t_{CKLZ}	Clock High to Output Low-Z	1	—	1	—	1	—	ns
Port-to-Port Delay								
t_{CO}	Clock-to-Clock Offset	6	—	8	—	10	—	ns

4831 tbl 11

NOTES:
1. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$).
2. These values are valid for either level of V_{DDQ} (3.3V/2.5V). See page 4 for details on selecting the desired I/O voltage levels for each port.

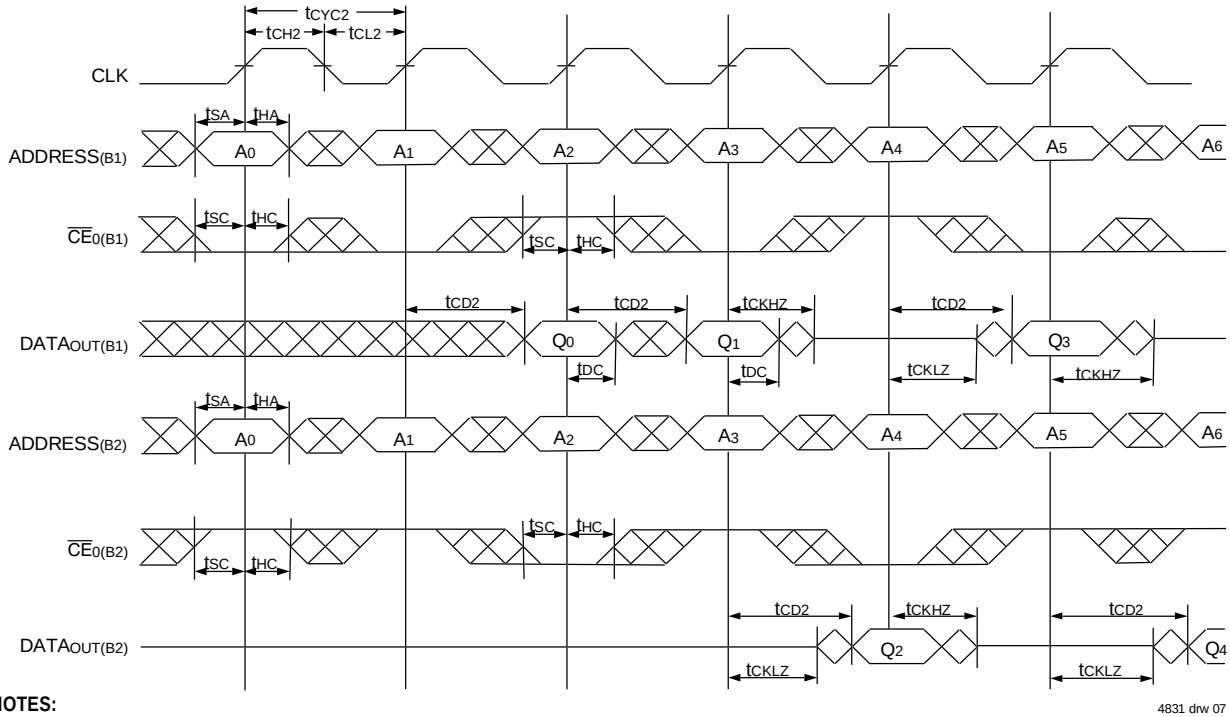
Timing Waveform of Read Cycle for Pipelined Operation(2)



4831 drw 06

NOTES:
1. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2. $\overline{ADS}$ = V_{IL}, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}.
3. The output is disabled (High-Impedance state) by $\overline{CE}_0$ = V_{IH}, CE_1 = V_{IL}, $\overline{BE}_n$ = V_{IH} following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If $\overline{BE}_n$ was HIGH, then the appropriate Byte of $DATA_{OUT}$ for Qn + 2 would be disabled (High-Impedance state).

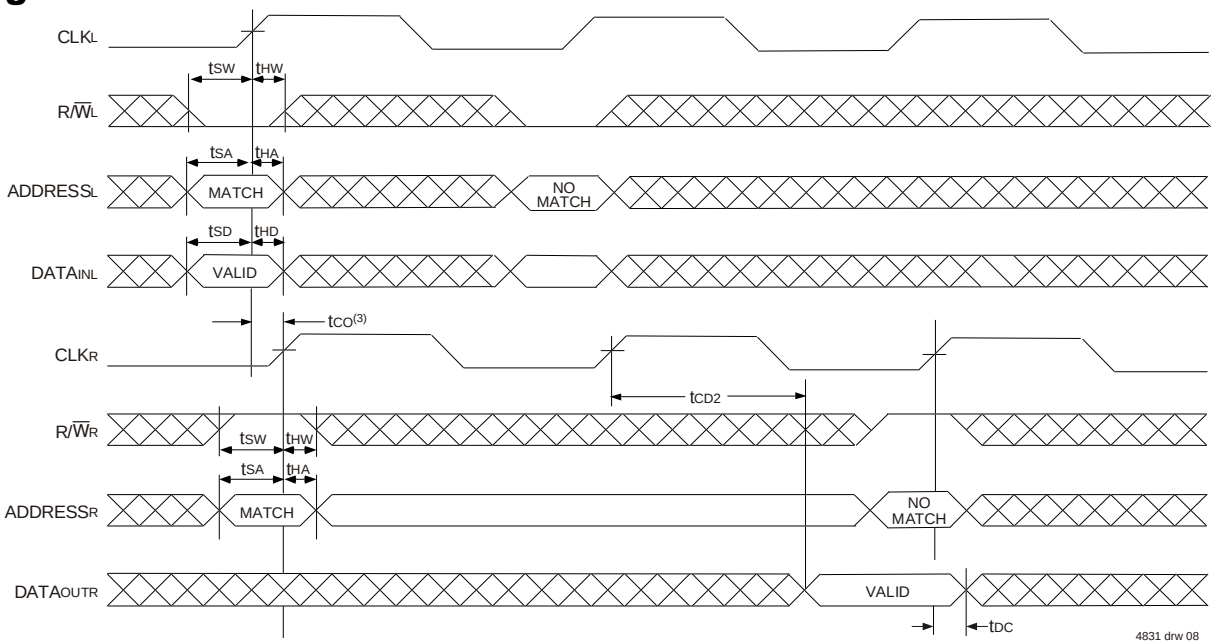
Timing Waveform of a Multi-Device Pipelined Read(1,2)



4831 drw 07

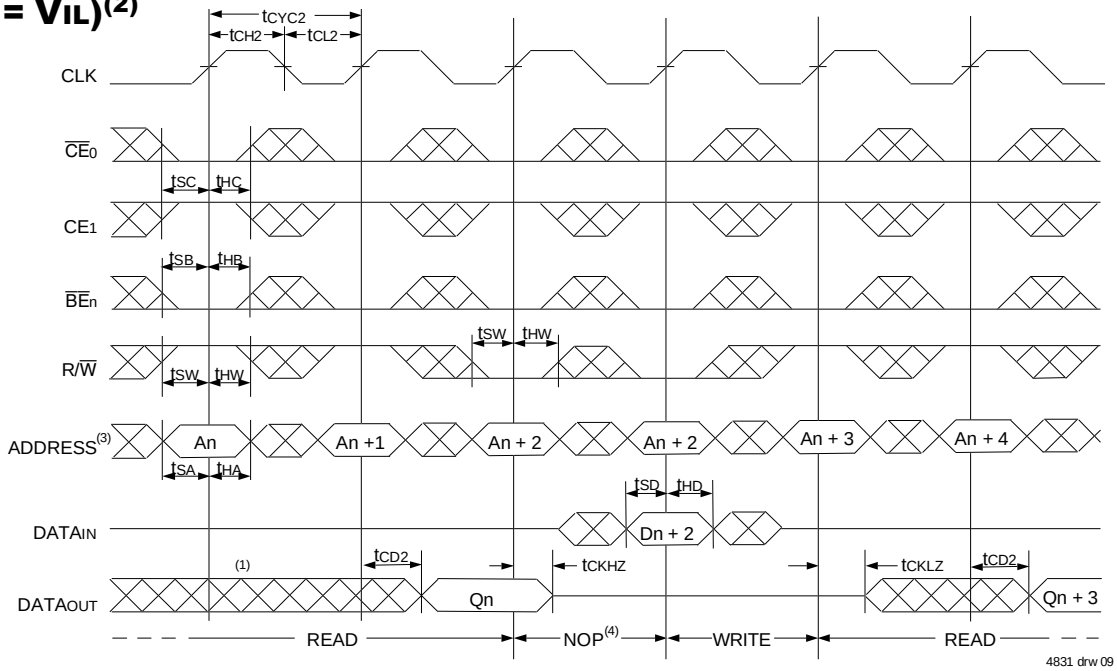
NOTES:
1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V3569 for this waveform, and are setup for depth expansion in this example. $ADDRESS_{(B1)}$ = $ADDRESS_{(B2)}$ in this situation.
2. $\overline{BE}_n$, $\overline{OE}$, and $\overline{ADS}$ = V_{IL}; $CE_{1(B1)}$, $CE_{1(B2)}$, R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.

Timing Waveform of Left Port Write to Pipelined Right Port Read(1,2)



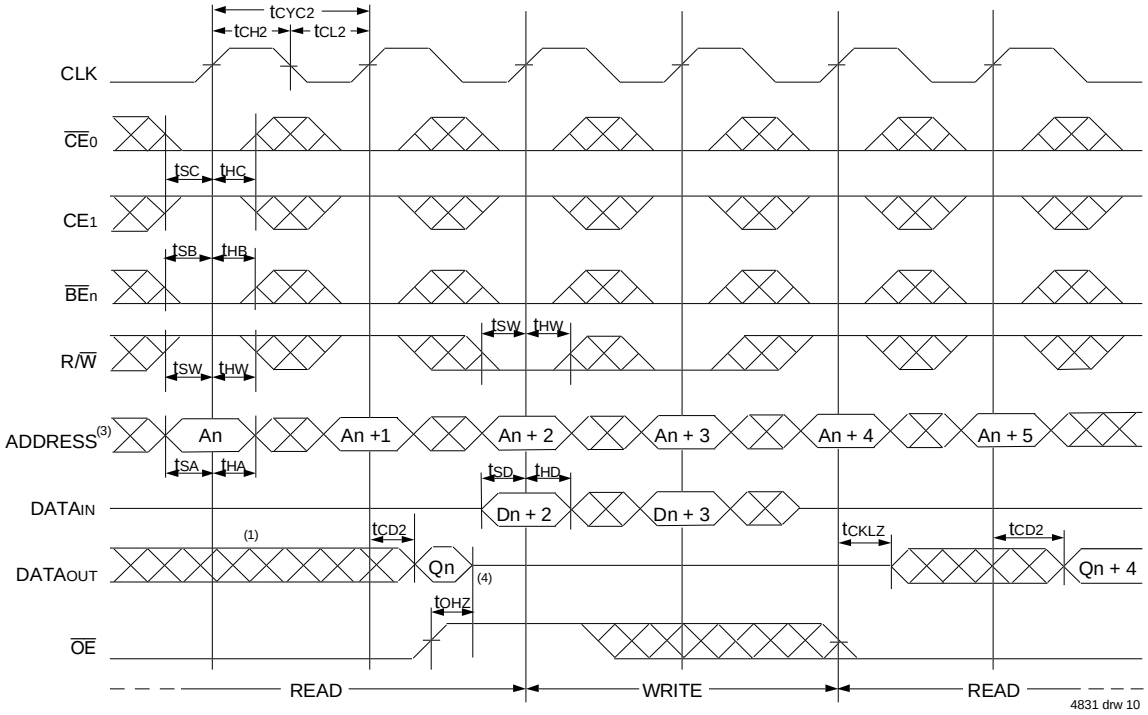
NOTES:
1. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL} for the Right Port, which is being read from. $\overline{OE}$ = V_{IH} for the Left Port, which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from right port read is not valid until following right port clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + 2\ t_{CYC2} + t_{CD2}$). If t_{CO} > minimum, then data from right port read is available on first right port clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + t_{CYC} + t_{CD2}$).

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ = V_{IL})(2)



NOTES:
1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

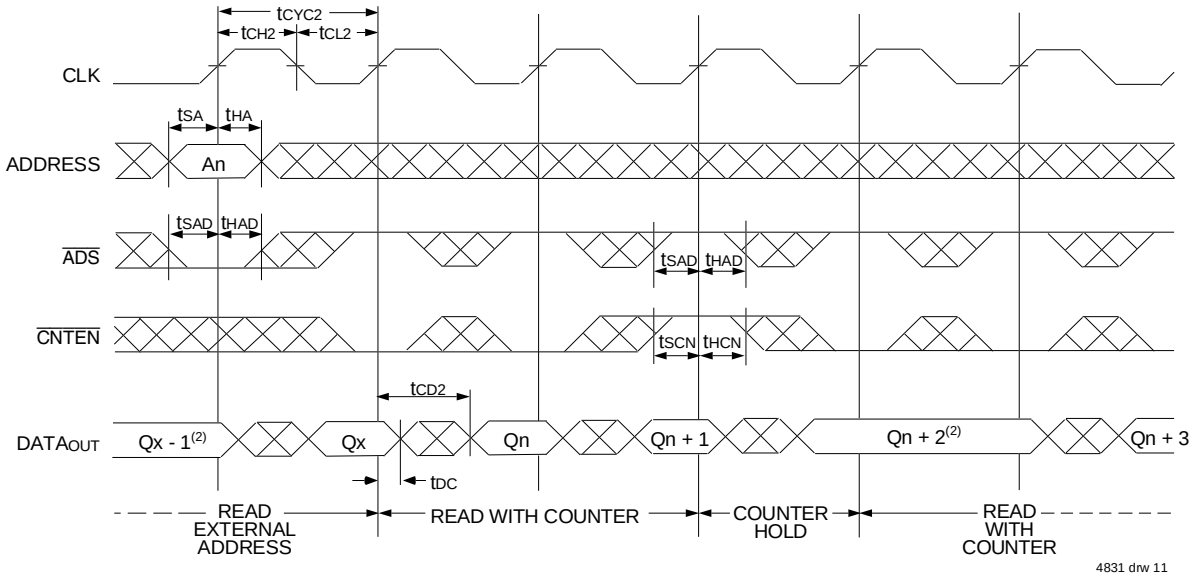
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)(2)



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

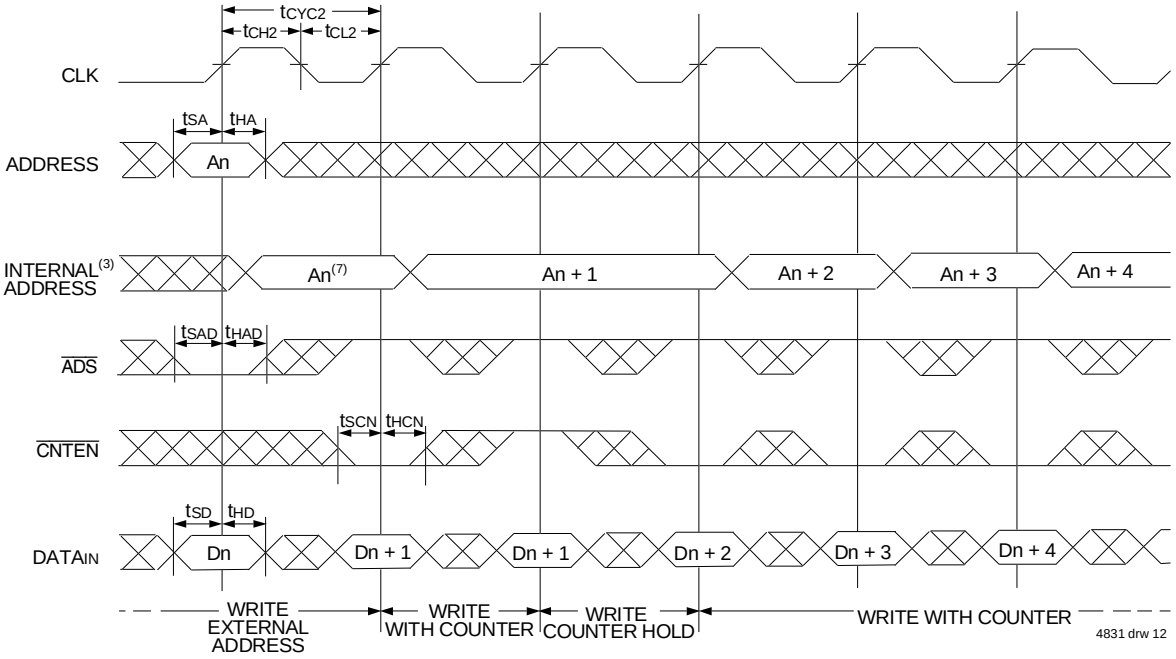
Timing Waveform of Pipelined Read with Address Counter Advance(1)



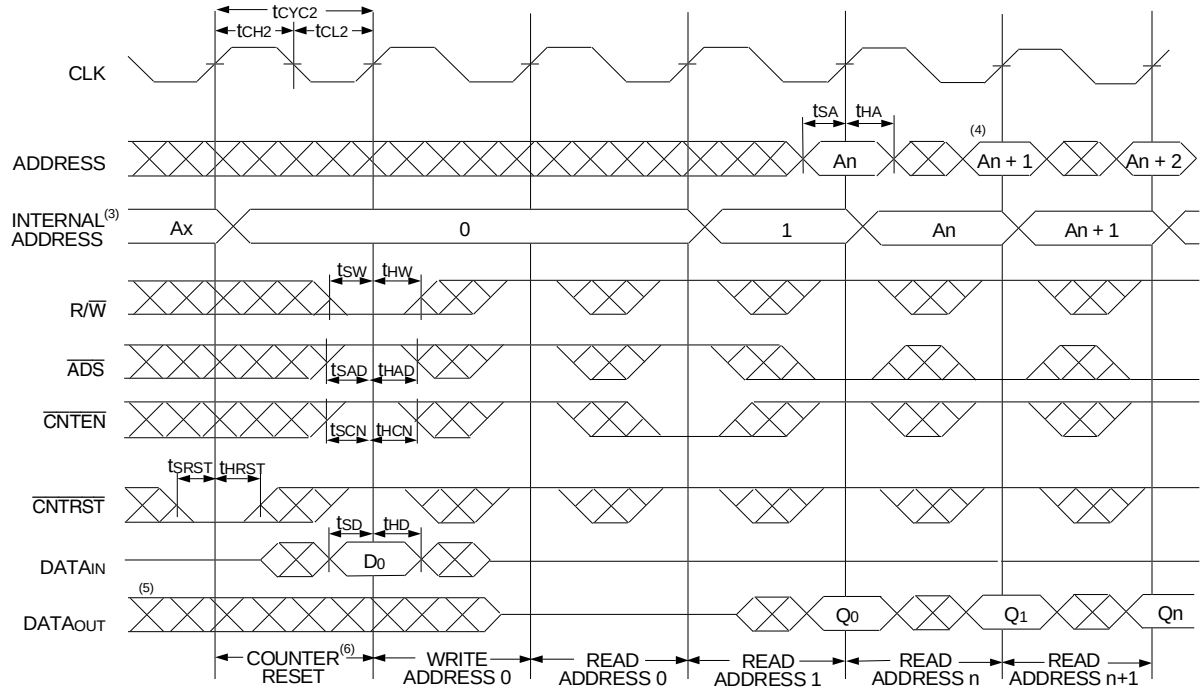
NOTES:

1. $\overline{CE_0}$, $\overline{OE}$, $\overline{BE_n}$ = V_{IL}; CE_1, R/$\overline{W}$, and $\overline{CNTRST}$ = V_{IH}.
2. If there is no address change via $\overline{ADS}$ = V_{IL} (loading a new address) or $\overline{CNTEN}$ = V_{IL} (advancing the address), i.e. $\overline{ADS}$ = V_{IH} and $\overline{CNTEN}$ = V_{IH}, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance(1)



Timing Waveform of Counter Reset(2)



NOTES:

1. $\overline{CE_0}$, $\overline{BE_n}$, and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{CNTRST}$ = V_{IH}.
2. $\overline{CE_0}$, $\overline{BE_n}$ = V_{IL}; CE_1 = V_{IH}.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle: ADDR 0 will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN}$ = V_{IL} advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1'Address is written to during this cycle.

Functional Description

The IDT70V3569 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE}_0$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V3569s for depth expansion configurations. Two cycles are required with $\overline{CE}_0$ LOW and CE_1 HIGH to re-activate the outputs.

Depth and Width Expansion

The IDT70V3569 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V3569 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 72-bits or wider.

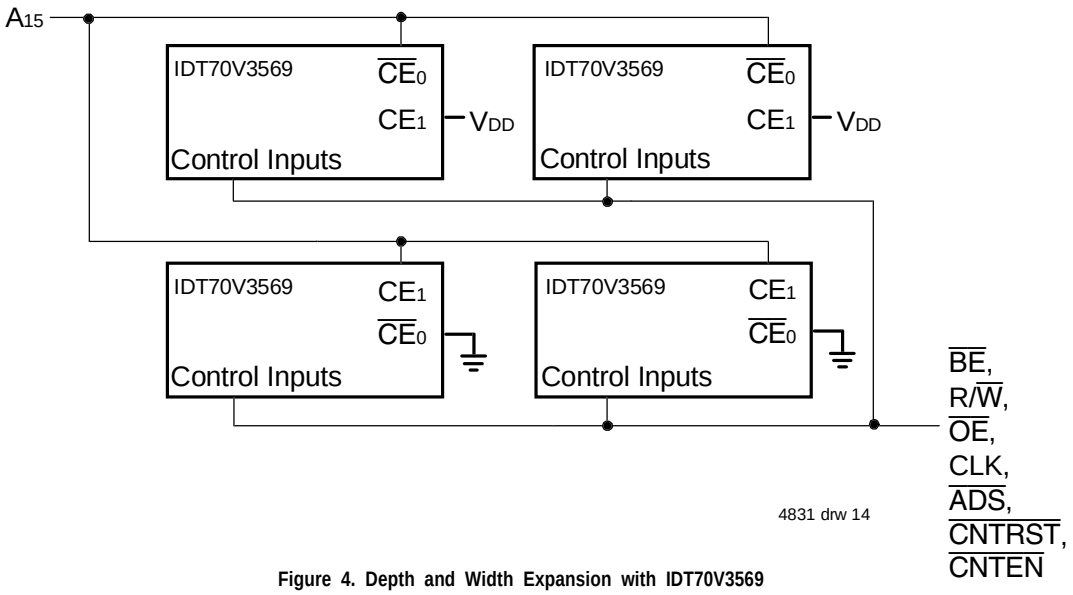
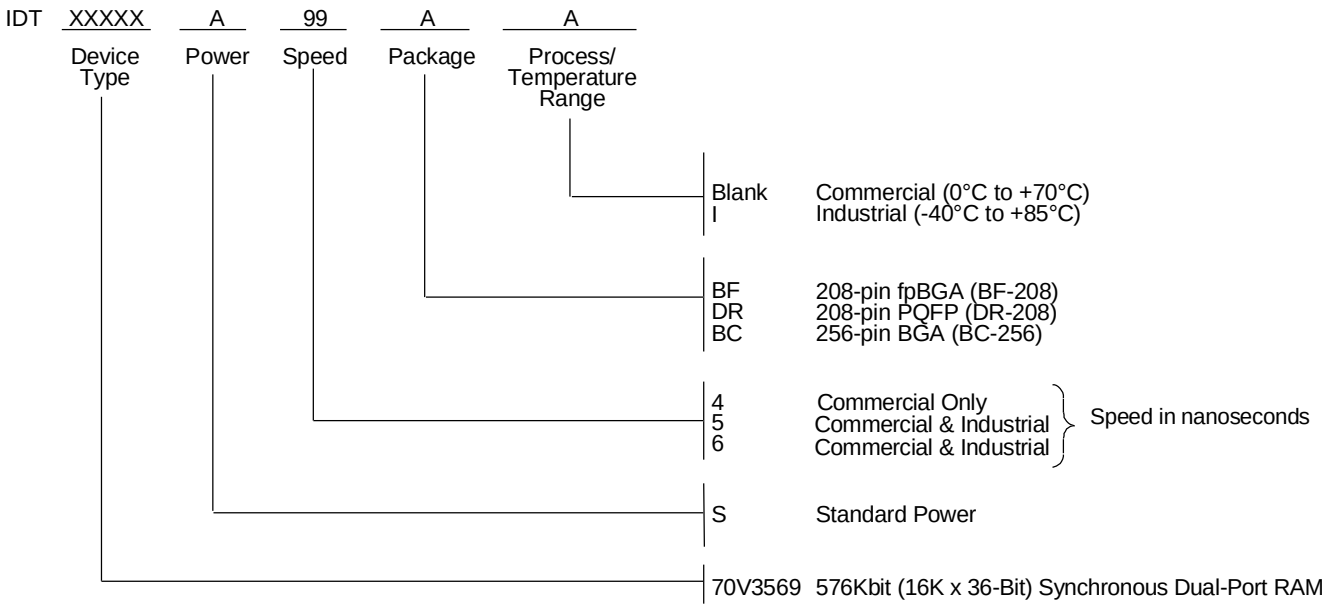


Figure 4. Depth and Width Expansion with IDT70V3569

Ordering Information



4831 drw 15A

Datasheet Document History

1/8/99:	Initial Public Release
3/12/99:	Added fpBGA package
4/28/99:	Fixed typo on page 10
6/8/99:	Changed drawing format
	Page 2 Changed package body dimensions
	Page 3 Fixed typo
6/15/99:	Page 5 Deleted note 6 for Table II
8/4/99:	Page 2 Fixed typographical error
	Page 6 Improved power number
10/14/99:	Upgraded speed to 133MHz, added 2.5V I/O capability
10/19/99:	Page 4 Corrected I/O numbers in Truth Table I
11/12/99:	Replaced IDT logo
4/10/00:	Added new BGA packages, added full 2.5V interface capability
1/12/01:	Page 6 Updated Truth Table II
	Increated storage temperature parameter
	Clarified T_A Parameter
	Page 8 DC Electrical parameters–changed wording from "open" to "disabled"
	Removed note 7 on DC Electrical Characteristics table
	Removed Preliminary status
4/10/01:	Added Industrial Temperature Ranges and removed related notes

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