



CYPRESS

CY62148B MoBL™

512K x 8 Static RAM

Features

- 4.5V–5.5V operation
- Low active power
 - Typical active current: 2.5 mA @ $f = 1$ MHz
 - Typical active current: 12.5 mA @ $f = f_{\max}$
- Low standby current
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with CE and OE features
- CMOS for optimum speed/power

Functional Description

The CY62148B is a high-performance CMOS static RAM organized as 512K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and three-state drivers. This device has

an automatic power-down feature that reduces power consumption by more than 99% when deselected.

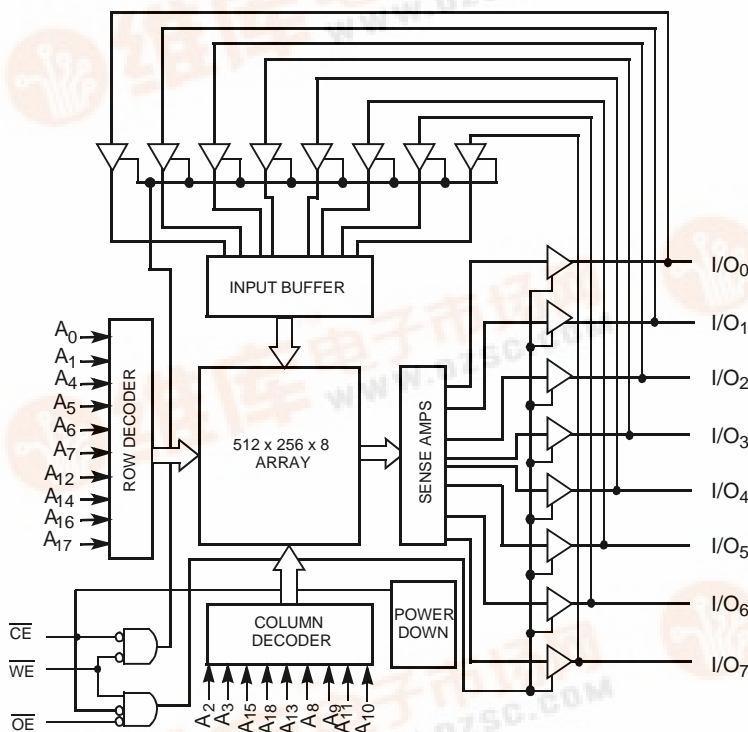
Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH for read. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY62148B is available in a standard 32-pin 450-mil-wide body width SOIC, 32-pin TSOP II, and 32-pin Reverse TSOP II packages.

Logic Block Diagram



Pin Configuration

Top View
SOIC
TSOP II

A_{17}	1	32	V_{CC}
A_{16}	2	31	A_{15}
A_{14}	3	30	A_{18}
A_{12}	4	29	\overline{WE}
A_7	5	28	A_{13}
A_6	6	27	A_8
A_5	7	26	A_9
A_4	8	25	A_{11}
A_3	9	24	\overline{OE}
A_2	10	23	A_{10}
A_1	11	22	\overline{CE}
A_0	12	21	I/O_7
I/O_0	13	20	I/O_6
I/O_1	14	19	I/O_5
I/O_2	15	18	I/O_4
GND	16	17	I/O_3

Top View
Reverse
TSOP II

GND	16	17	I/O_3
I/O_2	15	18	I/O_4
I/O_1	14	19	I/O_5
I/O_0	13	20	I/O_6
A_0	12	21	I/O_7
A_1	11	22	\overline{CE}
A_2	10	23	A_{10}
A_3	9	24	\overline{OE}
A_4	8	25	A_{11}
A_5	7	26	A_9
A_6	6	27	A_8
A_7	5	28	A_{13}
A_{12}	4	29	\overline{WE}
A_{14}	3	30	A_{18}
A_{16}	2	31	A_{15}
A_{17}	1	32	V_{CC}



Product Portfolio

Product	V _{CC} Range			Speed	Temp.	Power Dissipation			
						Operating, I _{CC}		Standby (I _{SB2})	
						f = f _{max}		Typ. ^[3]	Max.
	Min.	Typ.	Max.			Typ. ^[3]	Max.		
CY62148BLL	4.5 V	5.0V	5.5V	70 ns	Com'l	12.5 mA	20 mA	4 µA	20 µA
					Ind'l				

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –65°C to +150°C

Ambient Temperature with
Power Applied..... –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND –0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State^[1] –0.5V to V_{CC} +0.5V

DC Input Voltage^[1] –0.5V to V_{CC} +0.5V

Current into Outputs (LOW) 20 mA

Static Discharge Voltage.....2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V _{CC}
Commercial	0°C to +70°C	4.5V–5.5V
Industrial	–40°C to +85°C	

Notes:

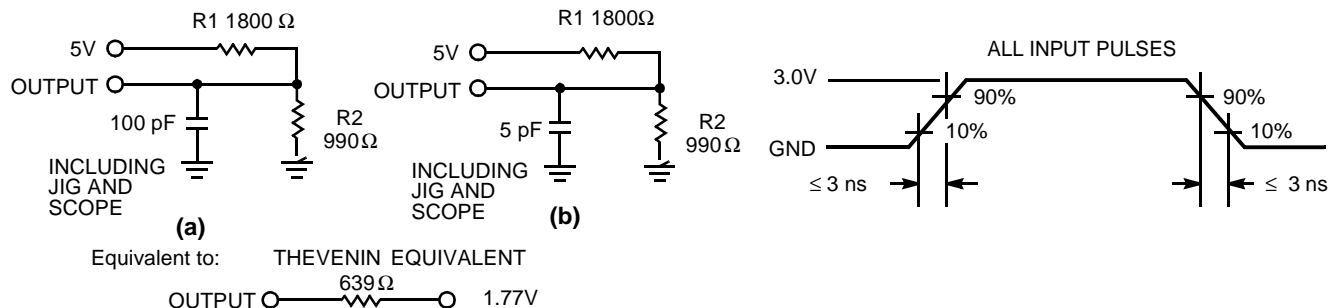
- V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
- T_A is the "Instant On" case temperature
- Typical values are measured at V_{CC} = 5V, T_A = 25°C, and are included for reference only and are not tested or guaranteed.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62148B-70			Unit
			Min.	Typ. ^[3]	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -1 mA	2.4			V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1 mA			0.4	V
V _{IH}	Input HIGH Voltage		2.2		V _{CC} +0.3	V
V _{IL}	Input LOW Voltage		-0.3		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}		12.5	20	mA
		f = 1 MHz		2.5		mA
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}			1.5	mA
I _{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0		4	20	μA

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	6	pF
C _{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms

Note:

- Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics^[5] Over the Operating Range

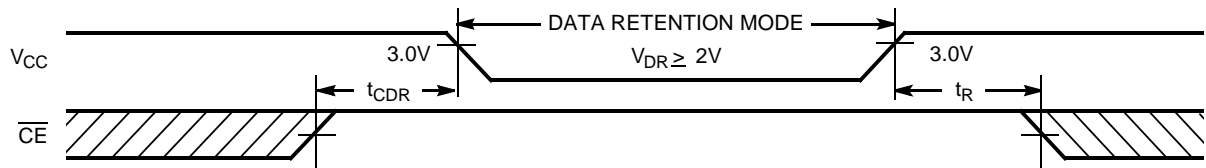
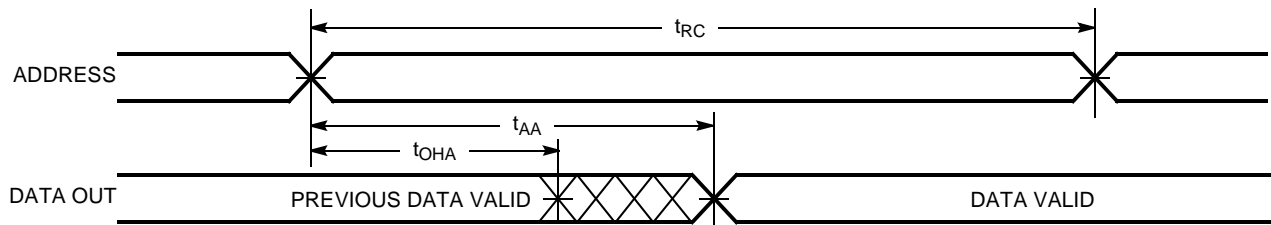
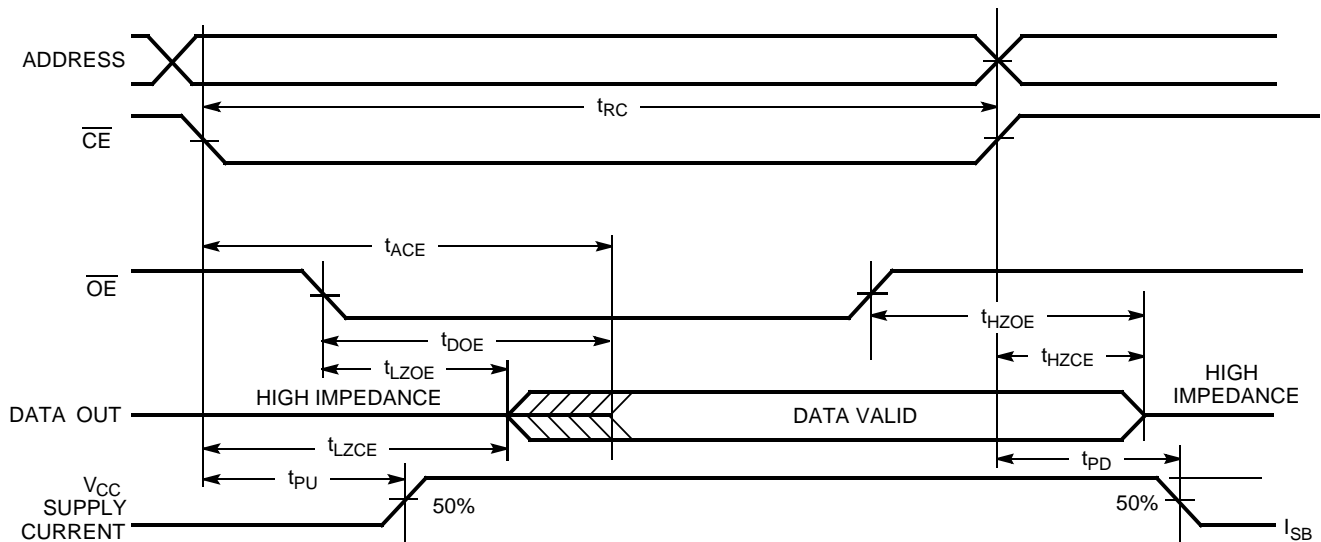
Parameter	Description	62148BLL-70		Unit
		Min.	Max.	
READ CYCLE				
t _{RC}	Read Cycle Time	70		ns
t _{AA}	Address to Data Valid		70	ns
t _{OHA}	Data Hold from Address Change	10		ns
t _{ACE}	\overline{CE} LOW to Data Valid		70	ns
t _{DOE}	\overline{OE} LOW to Data Valid		35	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[6]	5		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[6, 7]		25	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[6]	10		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]		25	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		70	ns
WRITE CYCLE ^[8]				
t _{WC}	Write Cycle Time	70		ns
t _{SCE}	\overline{CE} LOW to Write End	60		ns
t _{AW}	Address Set-Up to Write End	60		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Set-Up to Write Start	0		ns
t _{PWE}	\overline{WE} Pulse Width	55		ns
t _{SD}	Data Set-Up to Write End	30		ns
t _{HD}	Data Hold from Write End	0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[6]	5		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[6, 7]		25	ns

Notes:

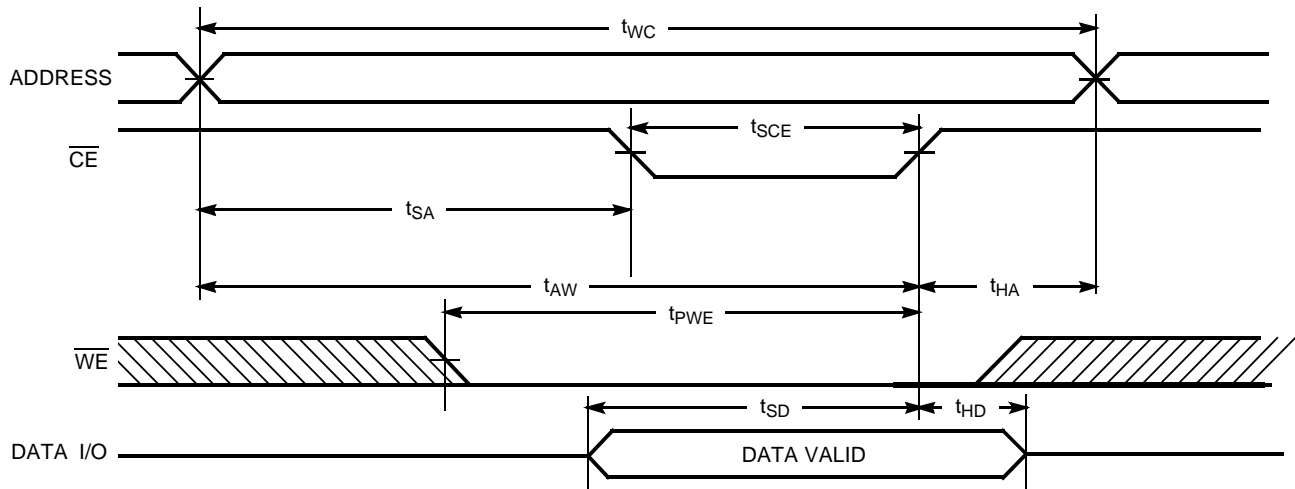
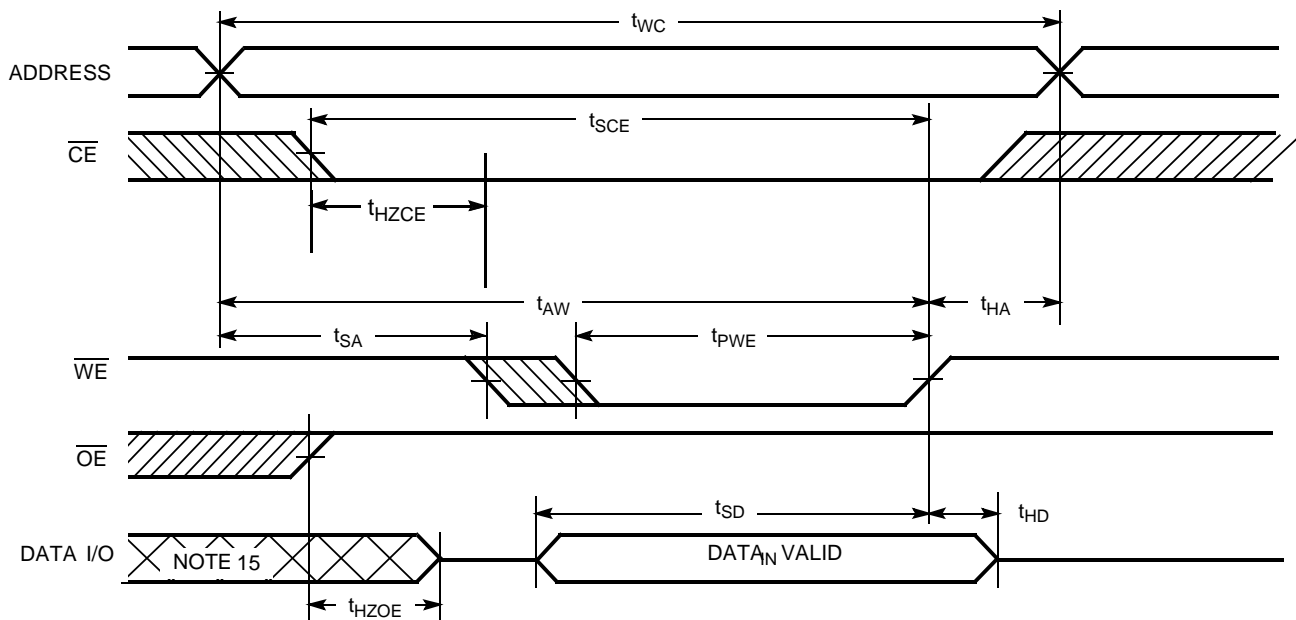
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics (Over the Operating Range)

Parameter	Description		Conditions	Min.	Typ. ^[3]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0			V
I_{CCDR}	Data Retention Current	Com'I	LL			20	μA
		Ind'I	LL			20	μA
$t_{CDR}^{[4]}$	Chip Deselect to Data Retention Time		No input may exceed $V_{CC} + 0.3V$ $V_{CC} = V_{DR} = 3.0V$ $CE > V_{CC} - 0.3V$	0			ns
$t_R^{[9]}$	Operation Recovery Time		$V_{IN} > V_{CC} - 0.3V$ or $V_{IN} < 0.3V$	t_{RC}			ns

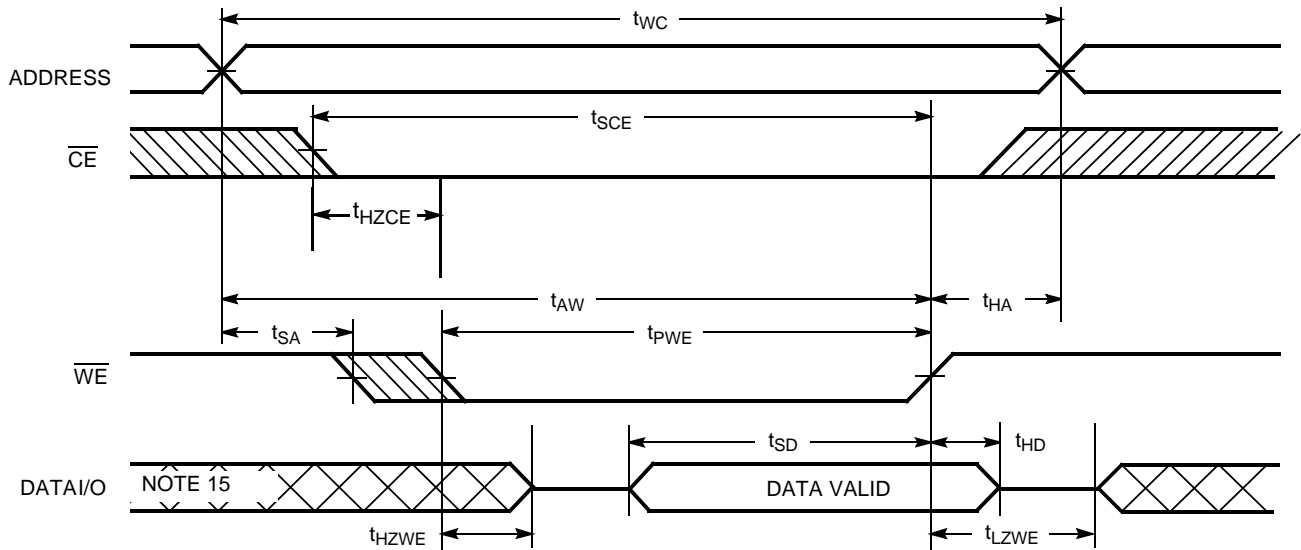
Data Retention Waveform

Switching Waveforms
Read Cycle No. 1^[10, 11]

Read Cycle No. 2 (\overline{OE} Controlled)^[11, 12]

Notes:

9. Full Device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ $\geq 100 \mu s$ or stable at $V_{CC(min)} \geq 100 \mu s$.
10. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
11. \overline{WE} is HIGH for read cycle.
12. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[13]

Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write)^[13, 14]

Notes:

13. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.
14. Data I/O is high-impedance if $\overline{\text{OE}} = V_{IH}$.
15. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No.3 (\overline{WE} Controlled, \overline{OE} LOW)^[13, 14]

Truth Table

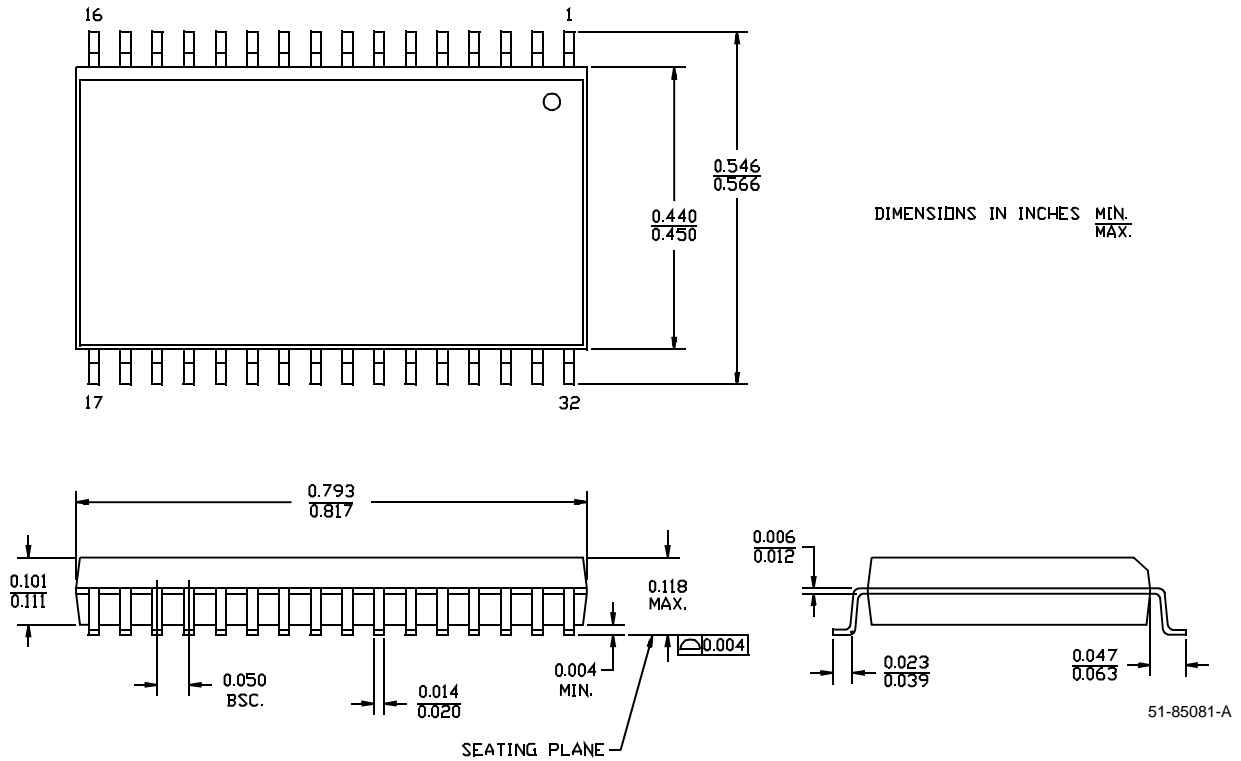
\overline{CE}	\overline{OE}	\overline{WE}	I/O ₀ – I/O ₇	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62148BLL-70SC	S34	32-Lead (450-Mil) Molded SOIC	Commercial
	CY62148BLL-70ZC	ZS32	32-Lead TSOP II	
	CY62148BLL-70ZRC	ZU32	32-Lead RTSOP II	
	CY62148BLL-70SI	S34	32-Lead (450-Mil) Molded SOIC	Industrial
	CY62148BLL-70ZI	ZS32	32-Lead TSOP II	
	CY62148BLL-70ZRI	ZU32	32-Lead RTSOP II	

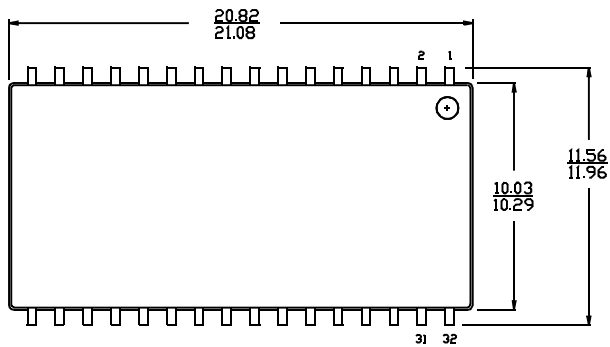
Package Diagrams

32-Lead (450 MIL) Molded SOIC S34

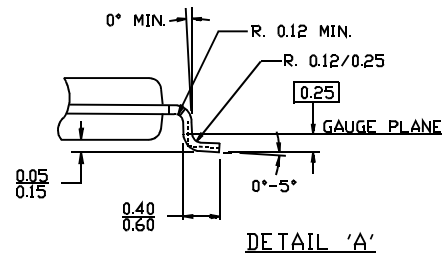
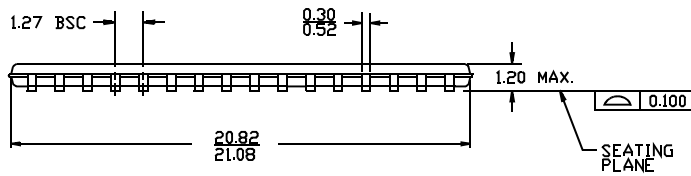
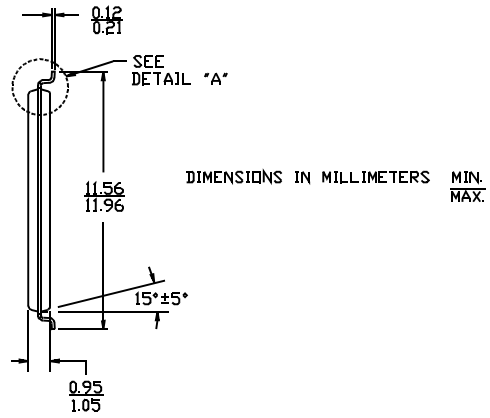


Package Diagrams (continued)

32-Lead TSOP II ZS32



TOP VIEW

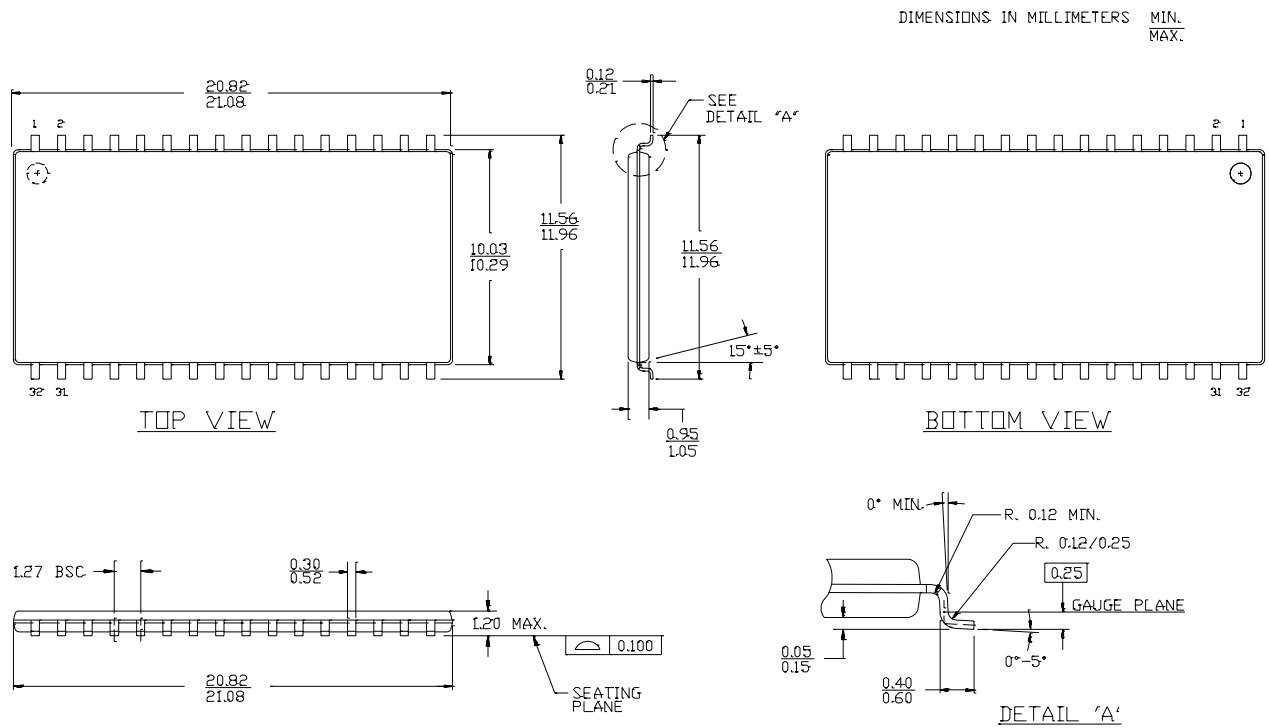


DETAIL 'A'

51-85095

Package Diagrams (continued)

32-Lead Reverse Thin Small Outline Package Type II ZU32



51-85138-**



Document Title: CY62148B 512K x 8 Static RAM Document Number: 38-05039				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106833	05/01/01	SZV	Change from Spec number 38-01104 to 38-05039
*A	106970	07/16/01	GAV	Modified annotations on Pin Configurations; $t_{SD} = 30$ ns
*B	109766	10/09/01	MGN	Remove 55-ns devices