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ECL Products	

100180

High Speed 8-Bit Adder

FEATURES

- Typical propagation delay: 2.35ns
- Typical supply current ($-I_{EE}$): 205mA

DESCRIPTION

The 100180 is a high-speed adder that can add two six-bit operands (A_n, B_n) and an Active-Low carry input (\bar{C}_{IN}).

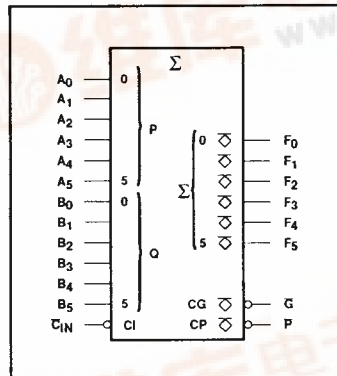
The sum is presented on the function outputs (F_n). When used in conjunction with the 100179, the carry generate and propagate outputs (\bar{G} and \bar{P}) allow more than one 100180 to add operands larger than 6-bits.

All unused inputs can be left open due to integrated pull-down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_5$	Operand A Inputs
$B_0 - B_5$	Operand B Inputs
\bar{C}_{IN}	Carry Input (Active-Low)
\bar{G}	Carry Generate Output (Active-Low)
\bar{P}	Carry Propagate Output (Active-Low)
$F_0 - F_5$	Function Outputs

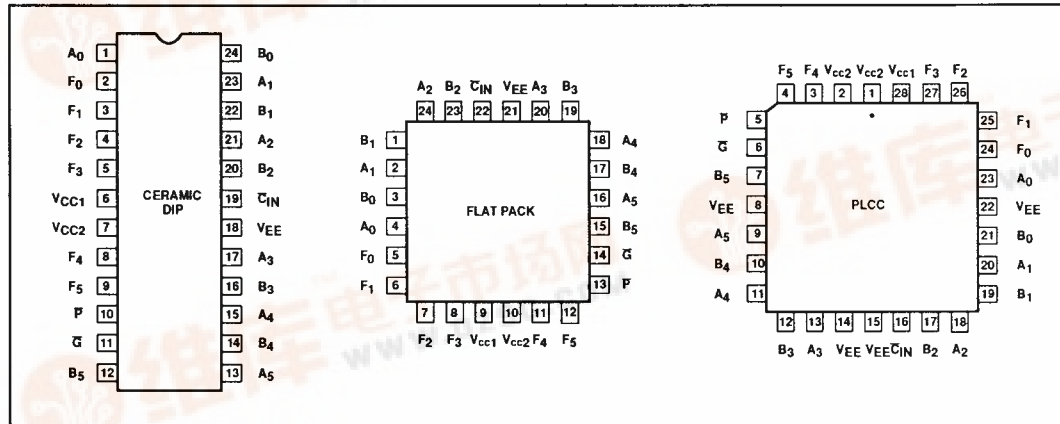
IEC/IEEE SYMBOL



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP (400 mils wide)	100180F
24-Pin Ceramic Flat Pack	100180Y
28-Pin PLCC	100180A

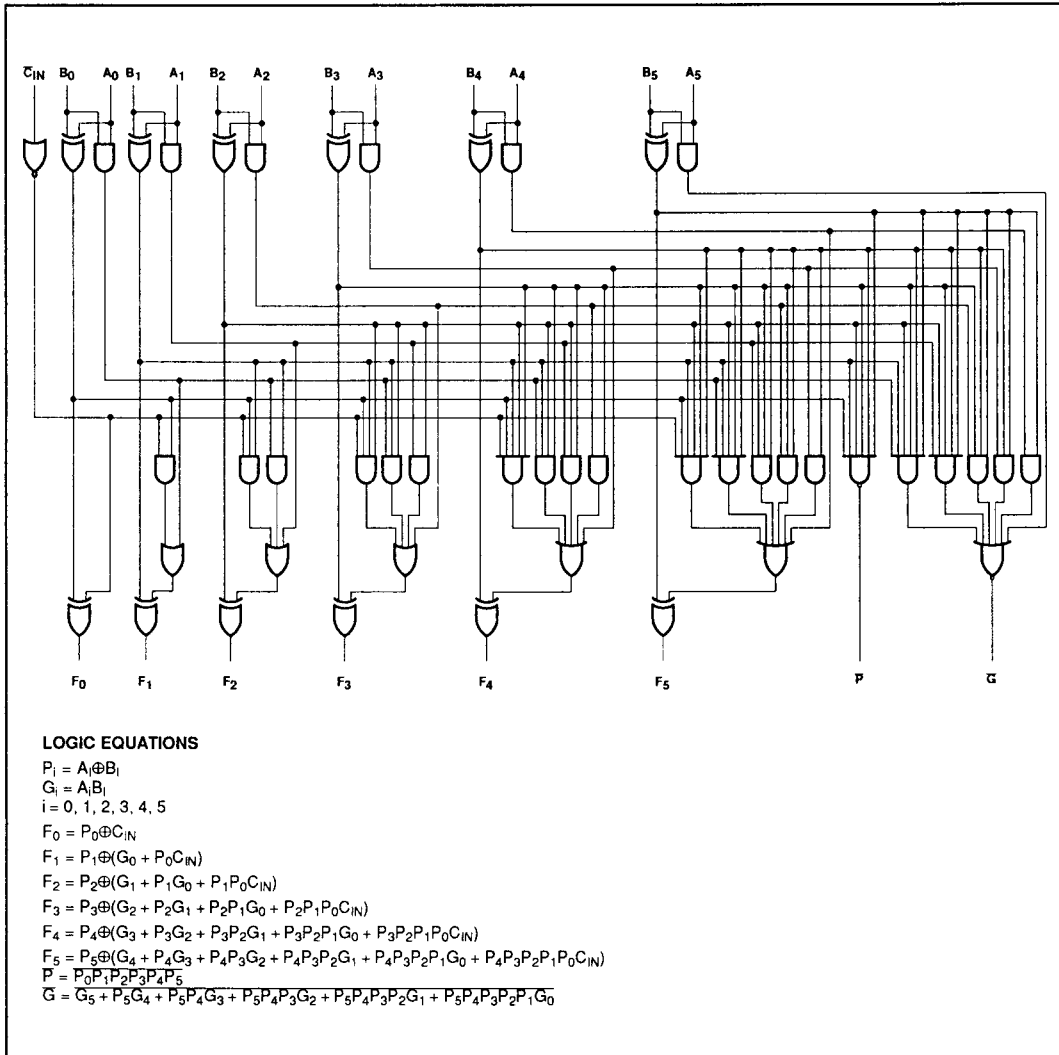
PIN CONFIGURATIONS



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LOGIC DIAGRAM



Adder**100180****ABSOLUTE MAXIMUM RATINGS** $V_{CC1} = V_{CC2} = \text{ground}$, $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	-7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	-55	mA
T_S	Storage temperature range	-65 to +150	$^\circ\text{C}$
T_J	Maximum junction temperature	+150	$^\circ\text{C}$

NOTE:

Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		-4.8	-4.5	-4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		-5.7			V
V_{IH}	High level input voltage	$V_{EE} = -4.2\text{V}$	-1150			mV
		$V_{EE} = -4.5\text{V}$	-1165		-880	
		$V_{EE} = -4.8\text{V}$	-1165			
V_{IL}	Low level input voltage	$V_{EE} = -4.2\text{V}$			-1475	mV
		$V_{EE} = -4.5\text{V}$	-1810		-1475	mV
		$V_{EE} = -4.8\text{V}$			-1490	mV
T_A	Operating ambient temperature range		0	+25	+85	$^\circ\text{C}$

NOTE:When operating at other than the specified V_{EE} voltages (-4.2V, -4.5V, -4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

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DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8\text{V}$ to -4.2V , $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise specified^{1,3,4}

SYMBOL	PARAMETER	TEST CONDITIONS ²			LIMITS			UNIT
					MIN.	TYP.	MAX.	
V_{OH}	High level output voltage	Outputs loaded with 50Ω to -2.0V $\pm 0.010\text{V}$	Inputs at V_{IHMAX} or V_{ILMIN} .	$V_{EE} = -4.2\text{V}$	-1020		-870	mV
				$V_{EE} = -4.5\text{V}$	-1025	-955	-880	mV
				$V_{EE} = -4.8\text{V}$	-1035		-880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN} .	$V_{EE} = -4.2\text{V}$	-1030			mV
				$V_{EE} = -4.5\text{V}$	-1035			mV
				$V_{EE} = -4.8\text{V}$	-1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN} .	$V_{EE} = -4.2\text{V}$			-1595	mV
				$V_{EE} = -4.5\text{V}$			-1610	mV
				$V_{EE} = -4.8\text{V}$			-1610	mV
V_{OL}	Low level output voltage	Inputs at V_{IHMAX} or V_{ILMIN} .	$V_{EE} = -4.2\text{V}$	-1810		-1605	mV	
			$V_{EE} = -4.5\text{V}$	-1810	-1705	-1620	mV	
			$V_{EE} = -4.8\text{V}$	-1830		-1620	mV	
I_{IH}	High level input current	One input under test at V_{IHMAX} . Other inputs at V_{ILMIN} .					220	μA
I_{IL}	Low level input current	One input under test at V_{ILMIN} . Other inputs at V_{IHMAX} .			0.5			μA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX} .			135	205	290	mA

NOTES:

- The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
- Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
- The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
- The device can function down to $V_{EE} = -5.7\text{V}$, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8\text{V}$ to -4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	1.10	4.70	1.10	4.60	1.10	4.70	ns
			1.10	4.70	1.10	4.60	1.10	4.70	ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to P		1.00	3.00	1.00	3.00	1.00	3.30	ns
			1.00	3.00	1.00	3.00	1.00	3.30	ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to G		1.10	3.90	1.20	3.80	1.20	3.90	ns
			1.10	3.90	1.20	3.80	1.20	3.90	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to F_n		0.90	4.00	0.90	3.90	0.90	4.00	ns
			0.90	4.00	0.90	3.90	0.90	4.00	ns
t_{TLH} t_{THL}	Transition time F_n, P, G		0.45	2.30	0.45	2.20	0.45	2.30	ns
		0.45	2.30	0.45	2.20	0.45	2.30	ns	

NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

Adder**100180****AC ELECTRICAL CHARACTERISTICS**Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	1.10 1.10	4.70 4.70	1.10 1.10	4.60 4.60	1.10 1.10	4.70 4.70	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to P		1.00 1.00	3.00 3.00	1.00 1.00	3.00 3.00	1.00 1.00	3.30 3.30	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to G		1.10 1.10	3.90 3.90	1.20 1.20	3.80 3.80	1.20 1.20	3.90 3.90	ns ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to F_n		0.90 0.90	4.00 4.00	0.90 0.90	3.90 3.90	0.90 0.90	4.00 4.00	ns ns
t_{TLH} t_{THL}	Transition time F_n, P, G		0.45 0.45	2.30 2.30	0.45 0.45	2.20 2.20	0.45 0.45	2.30 2.30	ns ns

NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICSFlat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	1.10 1.10	4.50 4.50	1.10 1.10	4.40 4.40	1.10 1.10	4.50 4.50	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to P		1.00 1.00	2.80 2.80	1.00 1.00	2.80 2.80	1.00 1.00	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to G		1.10 1.10	3.70 3.70	1.20 1.20	3.60 3.60	1.20 1.20	3.70 3.70	ns ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to F_n		0.90 0.90	3.80 3.80	0.90 0.90	3.70 3.70	0.90 0.90	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time F_n, P, G		0.45 0.45	2.30 2.30	0.45 0.45	2.20 2.20	0.45 0.45	2.30 2.30	ns ns

NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICSFlat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	1.10 1.10	4.50 4.50	1.10 1.10	4.40 4.40	1.10 1.10	4.50 4.50	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to P		1.00 1.00	2.80 2.80	1.00 1.00	2.80 2.80	1.00 1.00	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to G		1.10 1.10	3.70 3.70	1.20 1.20	3.60 3.60	1.20 1.20	3.70 3.70	ns ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to F_n		0.90 0.90	3.80 3.80	0.90 0.90	3.70 3.70	0.90 0.90	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time F_n, P, G		0.45 0.45	2.30 2.30	0.45 0.45	2.20 2.20	0.45 0.45	2.30 2.30	ns ns

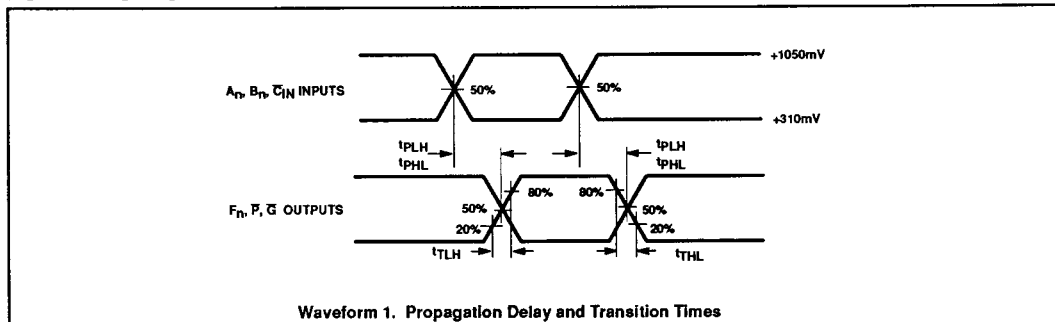
NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

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AC WAVEFORMS



NOTE:

All power and signal voltages shifted up 2.0V for AC bench test purposes.