

FAIRCHILD
SEMICONDUCTOR™

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100304 Low Power Quint AND/NAND Gate

General Description

The 100304 is monolithic quint AND/NAND gate. The Function output is the wire-NOR of all five AND gate outputs. All inputs have 50 kΩ pull-down resistors.

Features

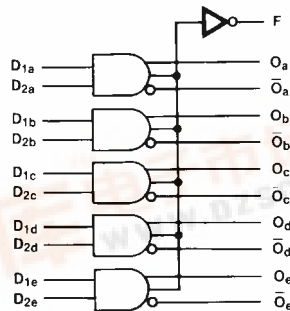
- Low Power Operation
- 2000V ESD protection
- Pin/function compatible with 100104
- Voltage compensated operating range = -4.2V to -5.7V
- Available to industrial grade temperature range (PLCC package only)

Ordering Code:

Order Number	Package Number	Package Description
100304PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
100304QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100304QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (-40°C to +85°C)

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



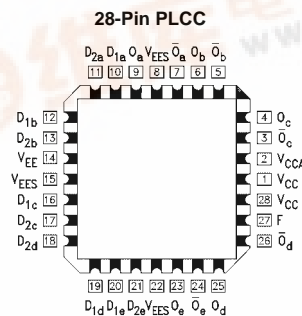
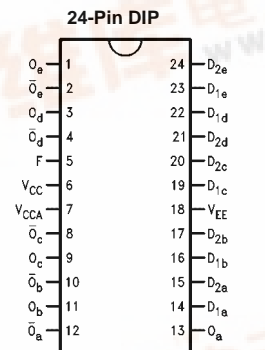
Pin Descriptions

Pin Names	Description
D _{1a} -D _{1e}	Data Inputs
F	Function Output
O _a -O _e	Data Outputs
\bar{O}_a - \bar{O}_e	Complementary Data Outputs

Logic Equation

$$F = (\bar{D}_{1a} \cdot \bar{D}_{2a}) + (\bar{D}_{1b} \cdot \bar{D}_{2b}) + (\bar{D}_{1c} \cdot \bar{D}_{2c}) + (\bar{D}_{1d} \cdot \bar{D}_{2d}) + (\bar{D}_{1e} \cdot \bar{D}_{2e})$$

Connection Diagrams



100304 Low Power Quint AND/NAND Gate



Absolute Maximum Ratings(Note 1)

Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
V_{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	-40°C to +85°C
Supply Voltage (V_{EE})	-5.7V to -4.2V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version**DC Electrical Characteristics** (Note 3)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH} (Max)$ Loading with 50Ω to -2.0V
V_{OL}	Output LOW Voltage	-1830	-1705	-1620	mV	$V_{IN} = V_{IL} (Min)$
V_{OHC}	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH}(Min)$ Loading with 50Ω to -2.0V
V_{OLC}	Output LOW Voltage			-1610	mV	or $V_{IL} (Max)$
V_{IH}	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs
I_{IL}	Input LOW Current	0.50			μA	$V_{IN} = V_{IL} (Min)$
I_{IH}	Input High Current $D_{2a}-D_{2e}$ $D_{1a}-D_{1e}$			250 350	μA	$V_{IN} = V_{IH}(Max)$
I_{EE}	Power Supply Current	-69	-43	-30	mA	Inputs open

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay $D_{na}-D_{ne}$ to O, \bar{O}	0.40	1.75	0.40	1.65	0.40	1.75	ns	Figures 1, 2
t_{PHL}	Propagation Delay Data to F	1.00	2.60	1.00	2.60	1.15	3.20	ns	
t_{TLH}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	
t_{THL}									

PLCC AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay $D_{na}-D_{ne}$ to O, \bar{O}	0.40	1.55	0.40	1.45	0.40	1.55	ns	Figures 1, 2
t_{PHL}	Propagation Delay Data to F	1.00	2.40	1.00	2.40	1.15	3.00	ns	
t_{TLH}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.15	0.35	1.10	ns	
t_{THL}									

Industrial Version

PLCC DC Electrical Characteristics (Note 4)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -40^{\circ}C$ to $+85^{\circ}C$

Symbol	Parameter	$T_C = -40^{\circ}C$		$T_C = 0^{\circ}C$ to $+85^{\circ}C$		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$	Loading with 50Ω to -2.0V
V_{OL}	Output LOW Voltage	-1830	-1575	-1830	-1620			
V_{OHC}	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with 50Ω to -2.0V
V_{OLC}	Output LOW Voltage		-1565		-1610			
V_{IH}	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1830	-1480	-1830	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	$V_{IN} = V_{IL} (Min)$	
I_{IH}	Input HIGH Current		250		250	μA	$V_{IN} = V_{IH} (Max)$	
	$D_{2a}-D_{2e}$		350		350			
	$D_{1a}-D_{1e}$							
I_{EE}	Power Supply Current	-69	-30	-69	-30	mA	Inputs OPEN	

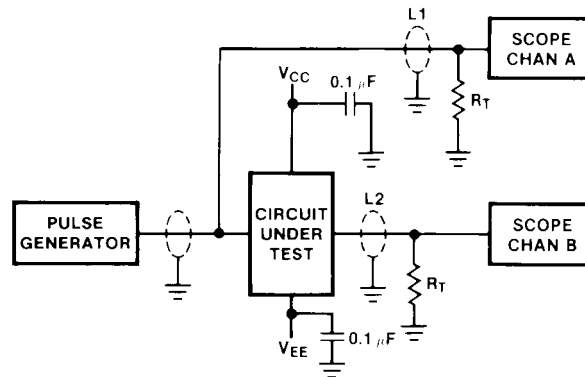
Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PLCC AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 40^{\circ}C$		$T_C = +25^{\circ}C$		$T_C = +85^{\circ}C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	0.35	1.55	0.40	1.45	0.40	1.55	ns	Figures 1, 2
t_{PHL}	$D_{na}-D_{ne}$ to O, \bar{O}								
t_{PLH}	Propagation Delay	1.00	2.40	1.00	2.40	1.15	3.00	ns	
t_{PHL}	Data to F								
t_{TLH}	Transition Time	0.35	1.10	0.35	1.15	0.35	1.10	ns	
t_{THL}	20% to 80%, 80% to 20%								

Test Circuitry



Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

L1 and L2 = equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms

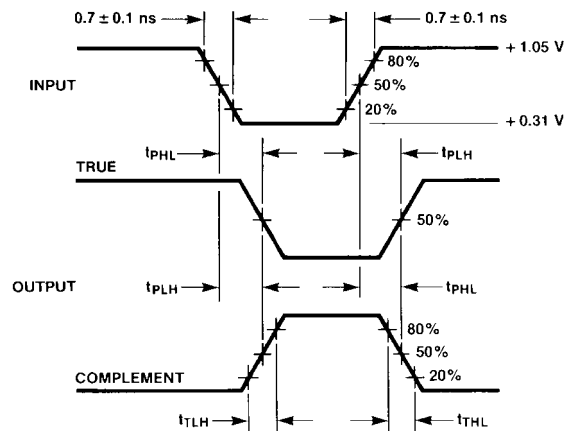
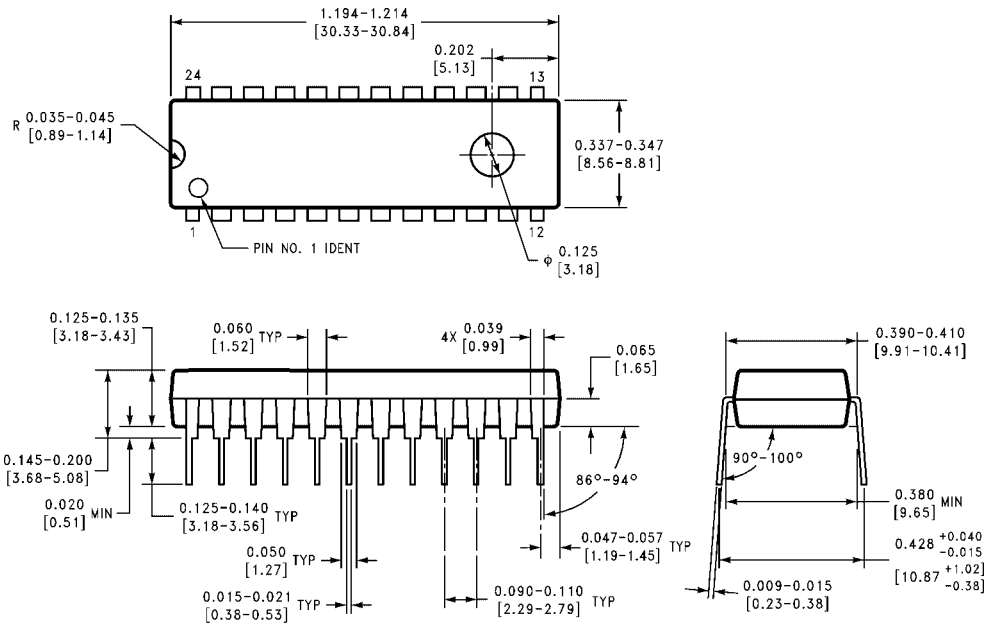


FIGURE 2. Propagation Delay and Transition Times

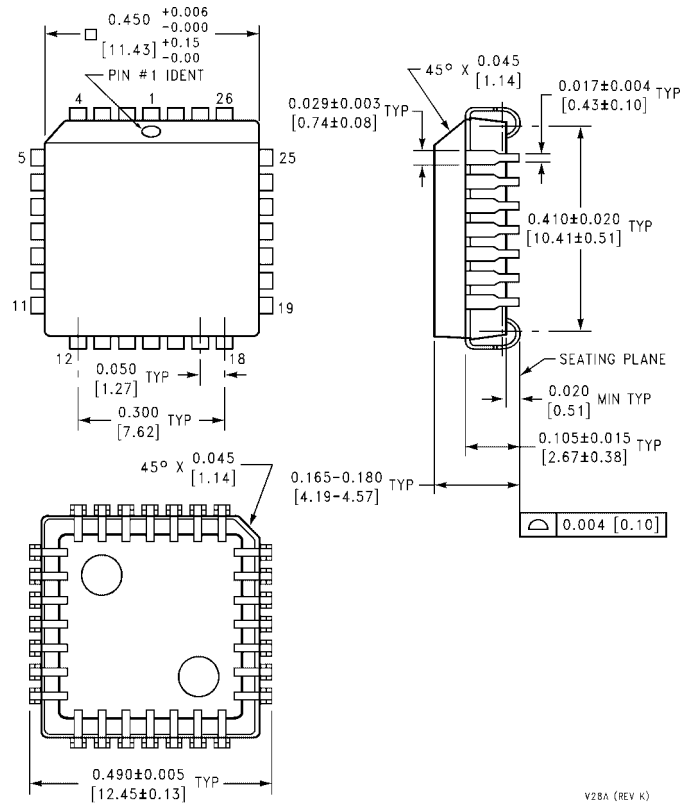
Physical Dimensions inches (millimeters) unless otherwise noted



N24E (REV A)

**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
Package Number N24E**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
Package Number V28A

V28A (REV K)

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