National Semiconductor

August 1998

# 100328
# Low Power Octal ECL/TTL Bi-Directional Translator with Latch

## General Description

The 100328 is an octal latched bi-directional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of this translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. A HIGH on the latch enable input (LE) latches the data at both inputs even though only one output is enabled at the time. A LOW on LE makes the 100328 transparent.

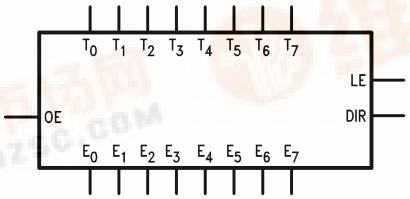
The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

The 100328 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have 50 kΩ pull-down resistors.

## Features

- Identical performance to the 100128 at 50% of the supply current
- Bi-directional translation
- 2000V ESD protection
- Latched outputs
- FAST TTL outputs
- TRI-STATE® outputs
- Voltage compensated operating range = −4.2V to −5.7V
- Available to MIL-STD-883

## Logic Symbol




DS100295-1

| Pin Names | Description |
|---|---|
| $E_0$–$E_7$ | ECL Data I/O |
| $T_0$–$T_7$ | TTL Data I/O |
| OE | Output Enable Input |
| LE | Latch Enable Input |
| DIR | Direction Control Input |

All pins function at 100K ECL levels except for $T_0$–$T_7$.

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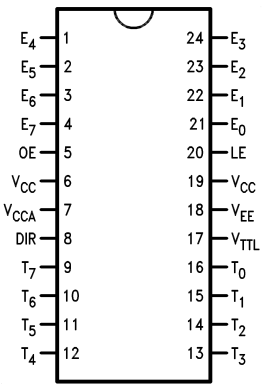
FAST® is a registered trademark of Fairchild Semiconductor.

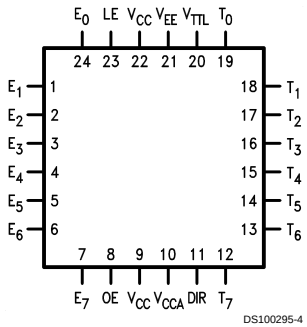
## Connection Diagrams

**24-Pin DIP**




DS100295-2

**24-Pin Quad Cerpak**

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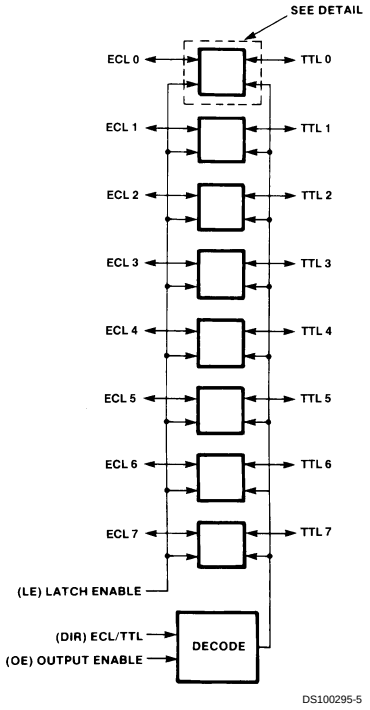
## Functional Diagram

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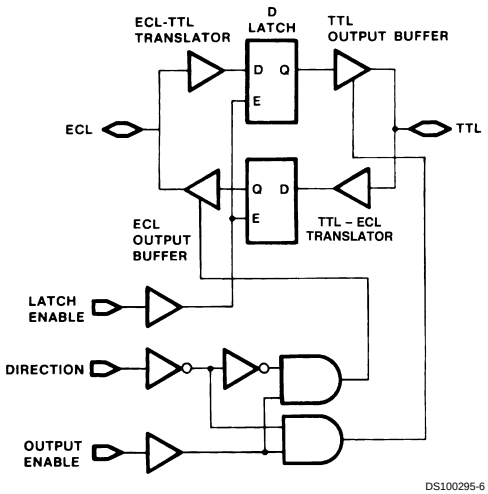
**Note:** LE, DIR, and OE use ECL logic levels

## Detail

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## Truth Table

| OE | DIR | LE | ECL Port | TTL Port | Notes |
|---|---|---|---|---|---|
| L | X | L | LOW (Cut-Off) | Z | |
| L | L | H | Input | Z | (Notes 1, 3) |
| L | H | H | LOW (Cut-Off) | Input | (Notes 2, 3) |
| H | L | L | L | L | (Notes 1, 4) |
| H | L | L | H | H | (Notes 1, 4) |
| H | L | H | X | Latched | (Notes 1, 3) |
| H | H | L | L | L | (Notes 2, 4) |
| H | H | L | H | H | (Notes 2, 4) |
| H | H | H | Latched | X | (Notes 2, 4) |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

**Note 1:** ECL input to TTL output mode.

**Note 2:** TTL input to ECL output mode.

**Note 3:** Retains data present before LE set HIGH.

**Note 4:** Latch is transparent.

## Absolute Maximum Ratings (Note 5)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Storage Temperature ($T_{STG}$) | −65˚C to +150˚C |
| Maximum Junction Temperature ($T_J$) | |
| Ceramic | +175˚C |
| $V_{EE}$ Pin Potential to Ground Pin | −7.0V to +0.5V |
| $V_{TTL}$ Pin Potential to Ground Pin | −0.5V to +6.0V |
| ECL Input Voltage (DC) | $V_{EE}$ to +0.5V |
| ECL Output Current (DC Output HIGH) | −50 mA |
| TTL Input Voltage (Note 7) | −0.5V to +6.0V |
| TTL Input Current (Note 7) | −30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State TRI-STATE Output | −0.5V to +5.5V |
| Current Applied to TTL Output in LOW State (Max) | Twice the Rated $I_{OL}$ (mA) |
| ESD (Note 6) | ≥2000V |

## Recommended Operating Conditions

| | |
|---|---|
| Case Temperature ($T_C$) | |
| Military | −55˚C to +125˚C |
| ECL Supply Voltage ($V_{EE}$) | −5.7V to −4.2V |
| TTL Supply Voltage ($V_{TTL}$) | +4.5V to +5.5V |

**Note 5:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 6:** ESD testing conforms to MIL-STD-883, Method 3015.

**Note 7:** Either voltage limit or current limit is sufficient to protect inputs.

## Military Version
## TTL-to-ECL DC Electrical Characteristics

$V_{EE}$ = −4.2V to −5.7V, $V_{CC}$ = $V_{CCA}$ = GND, $T_C$ = −55˚C to +125˚C, $V_{TTL}$ = +4.5V to +5.5V

| Symbol | Parameter | Min | Max | Units | $T_C$ | Conditions | | Notes |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1025 | −870 | mV | 0˚C to +125˚C | $V_{IN}$ = $V_{IH}$ (Max) or $V_{IL}$ (Min) | Loading with 50Ω to −2.0V | (Notes 8, 9, 10) |
| | | −1085 | −870 | mV | −55˚C | | | |
| $V_{OL}$ | Output LOW Voltage | −1830 | −1620 | mV | 0˚C to +125˚C | | | |
| | | −1830 | −1555 | mV | −55˚C | | | |
| | Cutoff Voltage | | −1950 | mV | 0˚C to +125˚C | OE or DIR Low | | |
| | | | −1850 | mV | −55˚C | | | |
| $V_{OHC}$ | Output HIGH Voltage | −1035 | | mV | 0˚C to +125˚C | $V_{IN}$ = $V_{IH}$ (Min) or $V_{IL}$ (Max) | Loading with 50Ω0 to −2.0V | (Notes 8, 9, 10) |
| | | −1085 | | mV | −55˚C | | | |
| $V_{OLC}$ | Output LOW Voltage | | −1610 | mV | 0˚C to +125˚C | | | |
| | | | −1555 | mV | −55˚C | | | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | V | −55˚C to +125˚C | Over $V_{TTL}$, $V_{EE}$, $T_C$ Range | | (Notes 8, 9, 10, 11) |
| $V_{IL}$ | Input LOW Voltage | | 0.8 | V | −55˚C to +125˚C | Over $V_{TTL}$, $V_{EE}$, $T_C$ Range | | (Notes 8, 9, 10, 11) |
| $I_{IH}$ | Input HIGH Current | | 70 | µA | −55˚C to 125˚C | $V_{IN}$ = +2.7V | | (Notes 8, 9, 10) |
| | Breakdown Test | | 1.0 | mA | −55˚C to +125˚C | $V_{IN}$ = +5.5V | | |
| $I_{IL}$ | Input LOW Current | −1.0 | | mA | −55˚C to +125˚C | $V_{IN}$ = +0.5V | | (Notes 8, 9, 10) |
| $V_{FCD}$ | Input Clamp Diode Voltage | −1.2 | | V | −55˚C to +125˚ C | $I_{IN}$ = −18 mA | | (Notes 8, 9, 10) |
| $I_{EE}$ | $V_{EE}$ Supply Current | | | | −55˚C to +125˚C | LE Low, OE and DIR High Inputs Open | | (Notes 8, 9, 10) |
| | | −165 | −73 | mA | | $V_{EE}$ = −4.2V to −4.8V | | |
| | | −175 | −73 | | | $V_{EE}$ = −4.2V to −5.7V | | |

## Military Version
## ECL-to-TTL DC Electrical Characteristics

$V_{EE}$ = −4.2V to −5.7V, $V_{CC}$ = $V_{CCA}$ = GND, $T_C$ = −55˚C to +125˚C, $C_L$ = 50 pF, $V_{TTL}$ = +4.5V to + 5.5V

| Symbol | Parameter | Min | Max | Units | $T_C$ | Conditions | Notes |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 2.5<br>2.4 | | mV | 0˚C to +125˚C<br>−55˚C | $I_{OH}$ = −1 mA, $V_{TTL}$ = 4.50V | (Notes 8, 9, 10) |
| $V_{OL}$ | Output LOW Voltage | | 0.5 | mV | −55˚C<br>+125˚C | $I_{OL}$ = 24 mA, $V_{TTL}$ = 4.50V | |
| $V_{IH}$ | Input HIGH Voltage | −1165 | −870 | mV | −55˚C<br>+125˚C | Guaranteed HIGH Signal for All Inputs | (Notes 8, 9, 10, 11) |
| $V_{IL}$ | Input LOW Voltage | −1830 | −1475 | mV | −55˚C to<br>+125˚C | Guaranteed LOW Signal for All Inputs | (Notes 8, 9, 10, 11) |
| $I_{IH}$ | Input HIGH Current | | 350<br>500 | µA | 0˚C to<br>+125˚C | $V_{EE}$ = −5.7V<br>$V_{IN}$ = $V_{IH}$ (Max) | (Notes 8, 9, 10) |
| $I_{IL}$ | Input LOW Current | 0.50 | | µA | −55˚C to<br>+125˚C | $V_{EE}$ = −4.2V<br>$V_{IN}$ = $V_{IL}$ (Min) | (Notes 8, 9, 10) |
| $I_{OZHT}$ | TRI-STATE Current Output High | | 70 | µA | −55˚C to<br>+125˚C | $V_{OUT}$ = +2.7V | (Notes 8, 9, 10) |
| $I_{OZLT}$ | TRI-STATE Current Output Low | −1.0 | | mA | −55˚C to<br>+125˚C | $V_{OUT}$ = +0.5V | (Notes 8, 9, 10) |
| $I_{OS}$ | Output Short-Circuit CURRENT | −150 | −60 | mA | −55˚C to<br>+125˚C | $V_{OUT}$ = 0.0V, $V_{TTL}$ = +5.5V | (Notes 8, 9, 10) |
| $I_{TTL}$ | $V_{TTL}$ Supply Current | | 75<br>50<br>70 | mA<br>mA<br>mA | −55˚C to<br>+125˚C | TTL Outputs Low<br>TTL Output High<br>TTL Output in TRI-STATE | (Notes 8, 9, 10) |

**Note 8:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 9:** Screen tested 100% on each device at −55˚C, +25˚C, and +125˚C, Subgroups, 1, 2 3, 7, and 8.

**Note 10:** Sample tested (Method 5005, Table I) on each manufactured lot at −55˚C, +25˚C, and +125˚C, Subgroups A1, 2, 3, 7, and 8.

**Note 11:** Guaranteed by applying specified input condition and testing $V_{OH}$/$V_{OL}$.

## Military Version
## TTL-to-ECL AC Electrical Characteristics

$V_{EE}$ = −4.2V to −5.7V, $V_{TTL}$ = +4.5V to +5.5V, $V_{CC}$ = $V_{CCA}$ = GND

| Symbol | Parameter | $T_C$ = −55˚C | | $T_C$ = 25˚C | | $T_C$ = +125˚C | | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| $t_{PLH}$<br>$t_{PHL}$ | $T_N$ to $E_n$<br>(Transparent) | 0.8 | 3.4 | 1.1 | 3.6 | 0.8 | 3.7 | ns<br>ns | *Figures 1, 2* | (Notes 12, 13, 14) |
| $t_{PLH}$<br>$t_{PHL}$ | LE to $E_n$ | 1.2 | 3.8 | 1.4 | 3.7 | 1.1 | 3.8 | ns<br>ns | *Figures 1, 2* | |
| $t_{PZH}$ | OE to $E_n$<br>(Cutoff to HIGH) | 0.8 | 3.6 | 1.5 | 4.0 | 2.0 | 5.2 | ns | *Figures 1, 2* | (Notes 12, 13, 14) |
| $t_{PHZ}$ | OE to $E_n$<br>(HIGH to Cutoff) | 1.5 | 4.6 | 1.6 | 4.2 | 1.6 | 4.3 | ns | *Figures 1, 2* | |
| $t_{PHZ}$ | DIR to $E_n$<br>(HIGH to Cutoff) | 1.6 | 4.7 | 1.6 | 4.3 | 1.7 | 4.3 | ns | *Figures 1, 2* | |
| $t_{set}$ | $T_n$ to LE | 2.5 | | 2.0 | | 2.5 | | ns | *Figures 1, 2* | (Note 15) |
| $t_{hold}$ | $T_n$ to LE | 2.5 | | 2.0 | | 2.5 | | ns | *Figures 1, 2* | |
| $t_{pw}$(H) | Pulse Width LE | 2.5 | | 2.0 | | 2.5 | | ns | *Figures 1, 2* | (Note 15) |
| $t_{TLH}$<br>$t_{THL}$ | Transition Time<br>20% to 80%, 80% to 20% | 0.4 | 2.3 | 0.5 | 2.1 | 0.4 | 2.4 | ns | *Figures 1, 2* | (Note 15) |

## Military Version
## ECL-to-TTL AC Electrical Characteristics

$V_{EE}$ = −4.2V to −5.7V, $V_{TTL}$ = +4.5V to +5.5V, $V_{CC}$ = $V_{CCA}$ = GND, $C_L$ = 50 pF

| Symbol | Parameter | $T_C$ = −55°C | | $T_C$ = 25°C | | $T_C$ = +125°C | | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| $t_{PLH}$ | $E_n$ to $T_n$ | 2.1 | 6.0 | 2.0 | 5.6 | 2.2 | 6.3 | ns | *Figures 1, 2* | (Notes 12, 13, 14) |
| $t_{PHL}$ | (Transparent) | | | | | | | | | |
| $t_{PLH}$ | LE to $T_n$ | 3.1 | 7.0 | 3.1 | 6.5 | 3.3 | 7.5 | ns | *Figures 3, 4* | |
| $t_{PHL}$ | | | | | | | | | | |
| $t_{PZH}$ | OE to $T_n$ | 3.2 | 8.0 | 3.7 | 8.0 | 4.0 | 9.2 | ns | *Figures 3, 4* | (Notes 12, 13, 14) |
| $t_{PZL}$ | (Enable Time) | 3.6 | 8.0 | 4.0 | 8.5 | 4.3 | 9.6 | | | |
| $t_{PHZ}$ | OE to $T_n$ | 3.2 | 8.5 | 3.3 | 8.0 | 3.5 | 8.4 | ns | *Figures 3, 5* | |
| $t_{PLZ}$ | (Disable Time) | 3.0 | 8.0 | 3.4 | 7.5 | 4.1 | 10.0 | | | |
| $t_{PHZ}$ | DIR to $T_n$ | 2.6 | 7.0 | 2.6 | 7.0 | 2.9 | 8.0 | ns | *Figures 3, 6* | |
| $t_{PLZ}$ | (Disable Time) | 2.7 | 7.0 | 3.1 | 7.0 | 4.0 | 10.0 | | | |
| $t_{set}$ | $E_n$ to LE | 2.5 | | 2.0 | | 2.5 | | ns | *Figures 3, 4* | (Note 15) |
| $t_{hold}$ | $E_n$ to LE | 3.0 | | 2.5 | | 3.0 | | ns | *Figures 3, 4* | |
| $t_{pw}$(H) | Pulse Width LE | 2.5 | | 2.0 | | 5.0 | | ns | *Figures 3, 4* | (Note 15) |

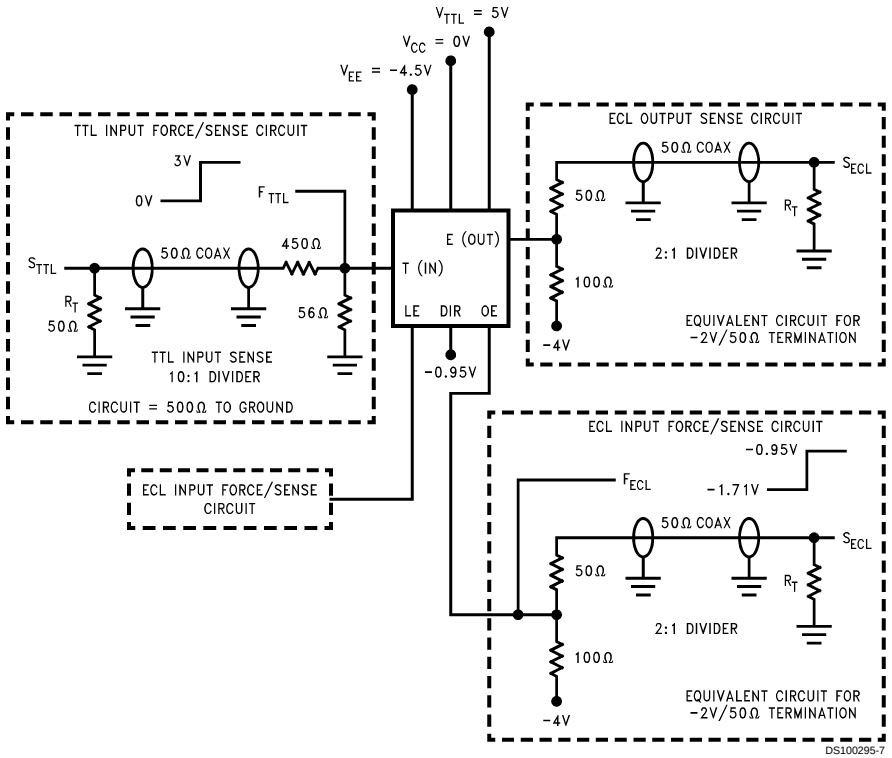
**Note 12:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 13:** Screen tested 100% on each device at +25°C, temperature only, Subgroup A9.

**Note 14:** Sample tested (Method 5005, Table I) on each mfg. lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

**Note 15:** Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

## Test Circuitry (TTL-to-ECL)




**Note 16:** $R_t$ =50Ω termination. When an input or output is being monitored by a scope, $R_t$ is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as $R_t$.

**Note 17:** TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

**Note 18:** $V_{TTL}$ is decoupled to ground with 0.1 µF to ground, $V_{EE}$ is decoupled to ground with 0.01 µF and $V_{CC}$ is connected to ground.

**Note 19:** For ECL input pins, the equivelent force/sense circuitry is optional.

**FIGURE 1. TTL-to-ECL AC Test Circuit**

## Switching Waveforms (TTL-to-ECL)

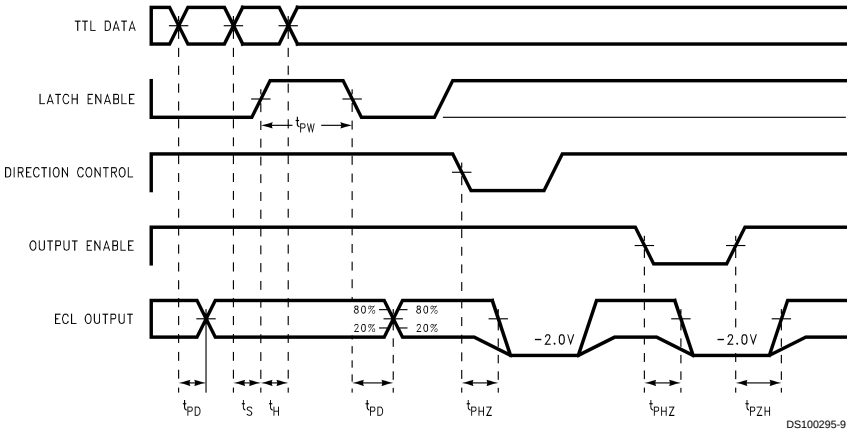
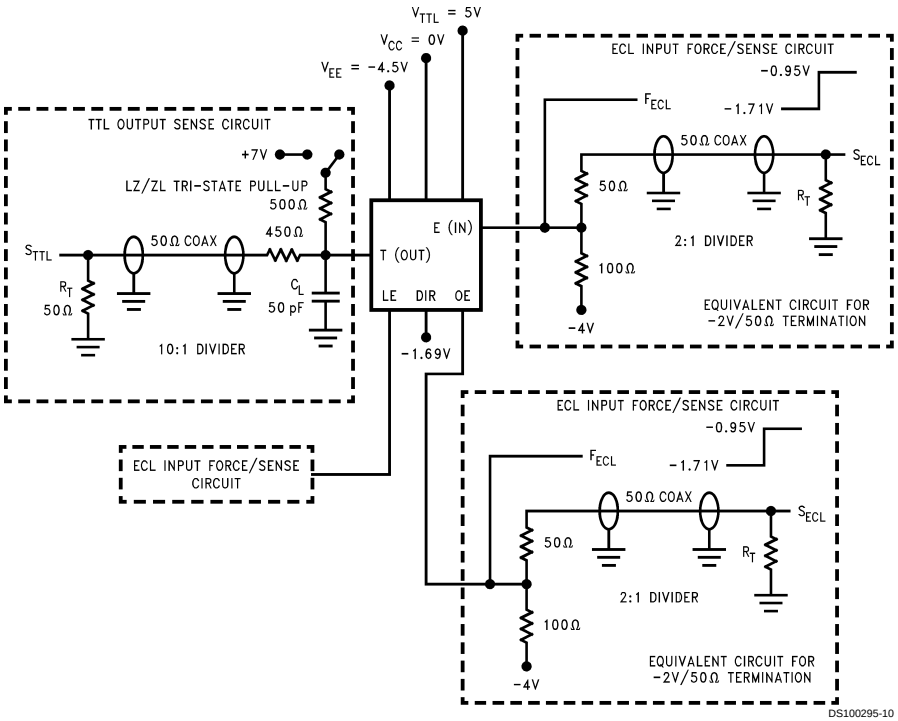



**FIGURE 2. TTL to ECL Transition — Propagation Delay and Transition Times**

## Test Circuitry (ECL-to-TTL)




**Note 20:** $R_t$ =50Ω termination. When an input or output is being monitored by a scope, $R_t$ is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as $R_t$.

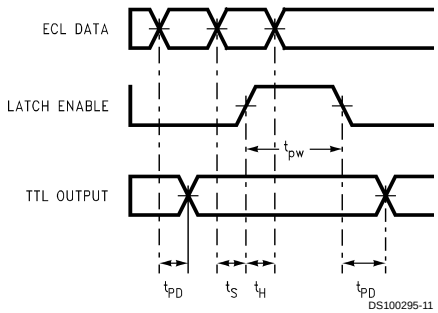
**Note 21:** The TTL TRI-STATE pull up switch is connected to +7V only for ZL and LZ tests.

**Note 22:** TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

**Note 23:** $V_{TTL}$ is decoupled to ground with 0.1 µF, $V_{EE}$ is decoupled to ground with 0.01 µF and $V_{CC}$ is connected to ground.

**FIGURE 3. ECL-to-TTL AC Test Circuit**

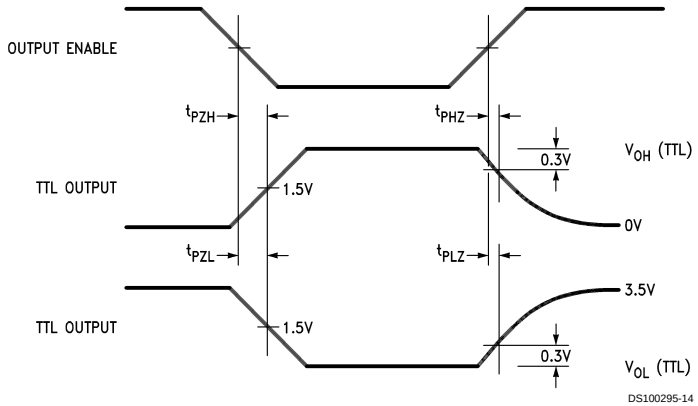
## Switching Waveforms (ECL-to-TTL)




**Note 24:** DIR is LOW, and OE is HIGH

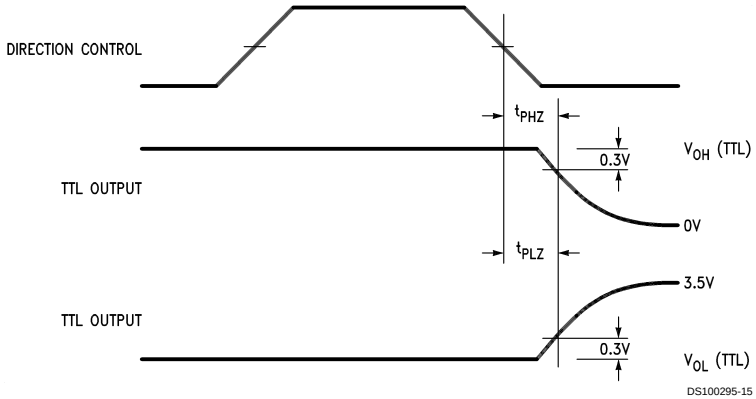
**FIGURE 4. ECL-to-TTL Transition — Propagation Delay and Transition Times**

## Switching Waveforms (ECL-to-TTL) (Continued)




**Note 25:** DIR is LOW, LE is HIGH

**FIGURE 5. ECL-to-TTL Transition, OE to TTL Output, Enable and Disable Times**




**Note 26:** OE is HIGH, LE is HIGH

**FIGURE 6. ECL-to-TTL Transition, DIR to TTL Output, Disable Time**

## Applications

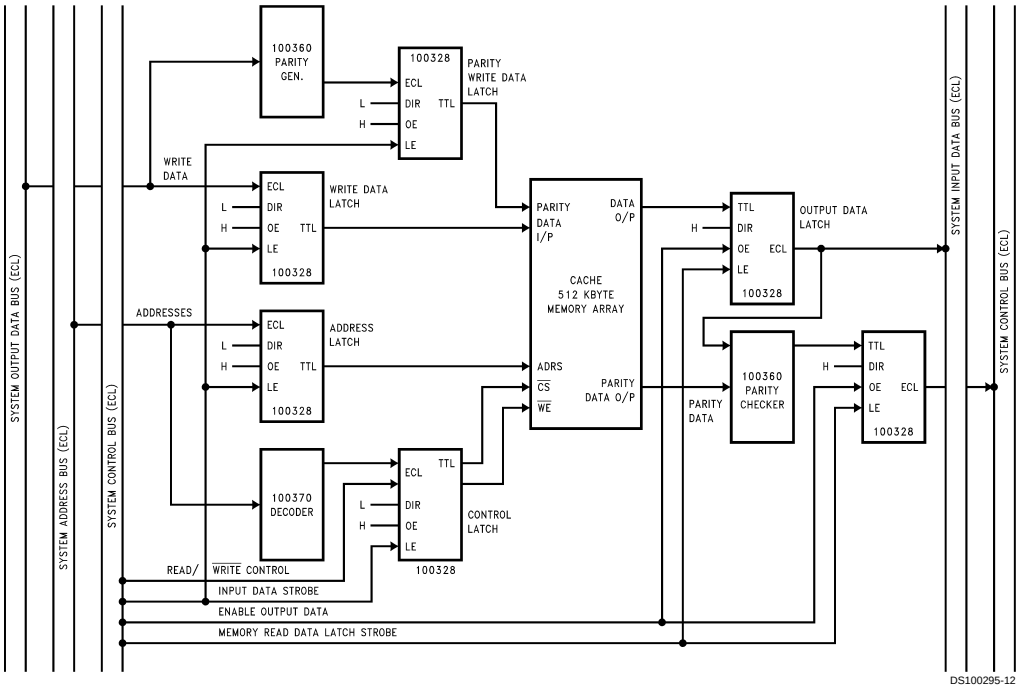



**FIGURE 7. Applications Diagram — MOS/TTL SRAM Interface Using 100328 ECL–TTL Latched Translator**

## Ordering Information

The device number is used to form part of a simplified purchasing code where A package type and temperature range are defined as follows:

100328 D C QB

Device Type (Basic)

Package Code
- D = Ceramic DIP
- F = Quad Cerpak
- P = Plastic DIP
- Q = Plastic Leaded Chip Carrier (PCC)
- S = Small Outline (SOIC)

Special Variation
- QB = Military grade device with environmental and burn-in processing

Temperature Range
- C = Commercial (0°C to +85°C)
- I = Industrial (−40°C to +85°C) (PCC Only)
- M = Military (−55°C to +125°C)

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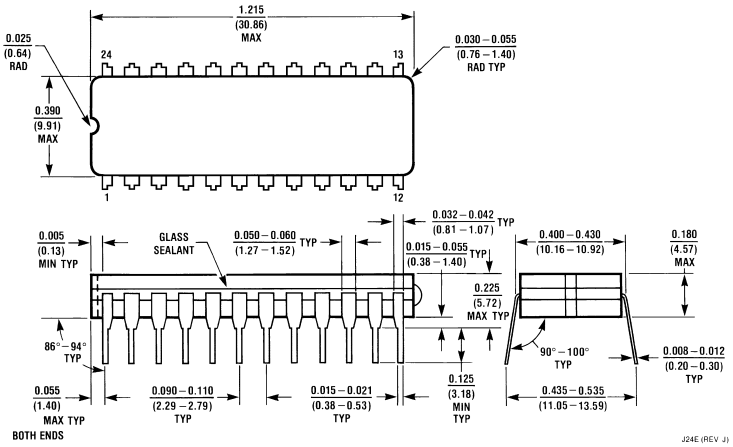
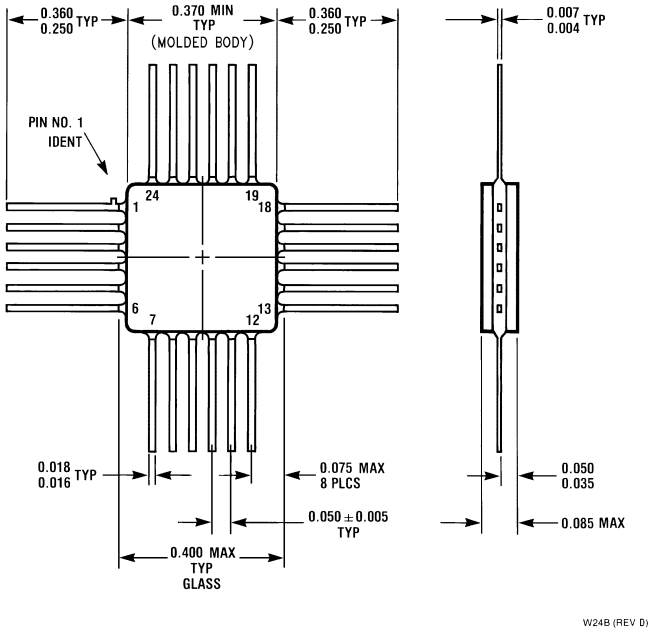
## Physical Dimensions inches (millimeters) unless otherwise noted




**24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)**
**NS Package Number J24E**




**24-Lead Quad Cerpak (F)**
**NS Package Number W24B**

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