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National Semiconductor

Not Intended For New Designs
August 1992

11C90/11C91
650 MHz Prescalers

General Description

The 11C90 and 11C91 are high-speed prescalers designed specifically for communication and instrumentation applications. All discussions and examples in this data sheet are applicable to the 11C91 as well as the 11C90.

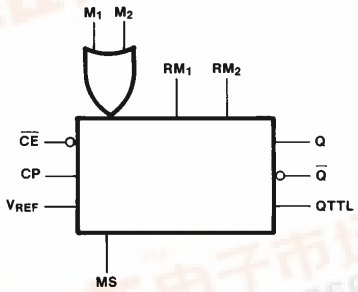
The 11C90 will divide by 10 or 11 and the 11C91 by 5 or 6, both over a frequency range from DC to typically 650 MHz. The division ratio is controlled by the Mode Control. The divide-by-10 or -11 capability allows the use of pulse swallowing techniques to control high-speed counting modulos by lower-speed circuits. The 11C90 may be used with either ECL or TTL power supplies.

In addition to the ECL outputs Q and $\overline{Q}$, the 11C90 contains an ECL-to-TTL converter and a TTL output. The TTL output operates from the same V_{CC} and V_{EE} levels as the counter, but a separate pin is used for the TTL circuit V_{EE}. This minimizes noise coupling when the TTL output switches and also allows power consumption to be reduced by leaving the separate V_{EE} pin open if the TTL output is not used.

To facilitate capacitive coupling of the clock signal, a 400Ω resistor (V_{REF}) is connected internally to the V_{BB} reference. Connecting this resistor to the Clock Pulse input (CP) automatically centers the input about the switching threshold. Maximum frequency operation is achieved with a 50% duty cycle.

Each of the Mode Control inputs is connected to an internal 2 kΩ resistor with the other end uncommitted (RM_1 and RM_2). An M input can be driven from a TTL circuit operating from the same V_{CC} by connecting the free end of the associated 2 kΩ resistor to V_{CCA}. When an M input is driven from the ECL circuit, the 2 kΩ resistor can be left open or, if required, can be connected to V_{EE} to act as a pull-down resistor.

Logic Symbol



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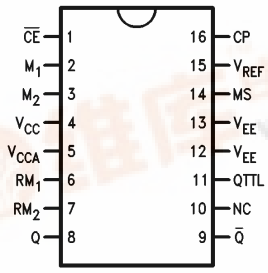
Pin Names	Description
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input
M_n	Count Modulus Control Input
MS	Asynchronous Master Set Input
Q, $\overline{Q}$	ECL Outputs
QTTL	TTL Output
RM_n	2 kΩ Resistor to M_n
V_{REF}	400Ω Resistor to V_{BB}

Connection Diagram

16-Pin DIP



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Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage Range	−7.0V to GND
Input Voltage (DC)	V_{EE} to GND
Output Current (DC Output HIGH)	−50 mA
Operating Range	−5.7V to −4.7V
Lead Temperature (Soldering, 10 sec.)	300°C

Recommended Operating Conditions

	Min	Typ	Max
Ambient Temperature (T_A)			
Commercial	0°C		+75°C
Military	−55°C		+125°C
Supply Voltage (V_{EE})			
Commercial	−5.7V	−5.2V	−4.7V
Military	−5.7V	−5.2V	−4.7V

TTL Input/Output Operation

DC Electrical Characteristics

Over Operating Temperature and Voltage Range unless otherwise noted, Pins 12 and 13 = GND

Symbol	Parameter	Min	Typ (Note 3)	Max	Units	Conditions
V_{IH}	Input HIGH Voltage M_1 and M_2 Inputs		4.1		V	Guaranteed Input HIGH Threshold Voltage (Note 4), $V_{CC} = V_{CCA} = 5.0V$
V_{IL}	Input LOW Voltage M_1 and M_2 Inputs		3.3		V	Guaranteed Input LOW Threshold Voltage (Note 4), $V_{CC} = V_{CCA} = 5.0V$
V_{OH}	Output HIGH Voltage QTTL Output	2.3	3.3		V	$V_{CC} = V_{CCA} =$ Min, $I_{OH} = -640\ \mu A$
V_{OL}	Output LOW Voltage QTTL Output		0.2	0.5	V	$V_{CC} = V_{CCA} =$ Min, $I_{OL} = 20.0$ mA
I_{IL}	Input LOW Current M_1 and M_2 Inputs		−2.3	−5.0	mA	$V_{CC} = V_{CCA} =$ Max, $V_{IN} = 0.4V$, Pins 6, 7 = V_{CC}
I_{SC}	Output Short Circuit Current	−20	−35	−80	mA	$V_{CC} = V_{CCA} =$ Max, $V_{OUT} = 0.0V$, Pin 14 = V_{CC}

AC Electrical Characteristics

$V_{CC} = V_{CCA} = 5.0V$ Nominal, V_{EE} = GND, $T_A = +25°C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{PLH} t_{PHL}	Propagation Delay, (50% to 50%) CP to QTTL	6	10	14	ns	See *Figure 1*
t_{PLH}	Propagation Delay, (50% to 50%) MS to QTTL		12	17	ns	
t_s	Mode Control Setup Time	4	2		ns	
t_h	Mode Control Hold Time	0	−2		ns	
t_{TLH}	Output Rise Time (20% to 80%)		10		ns	
t_{THL}	Output Fall Time (80% to 20%)		2		ns	
f_{MAX}	Count Frequency	550 600	650 650		MHz	−55°C to +125°C 0°C to +75°C Clock Input AC Coupled 350 mV Peak-to-Peak Sinewave (Note 5)

ECL Operation—Commercial Version

DC Electrical Characteristics

$V_{CC} = V_{CCA} = GND$, $V_{EE} = -5.2V$

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions
V_{OH}	Output HIGH Voltage Q and $\overline{Q}$	−1060 −1025 −980	−995 −960 −910	−905 −880 −805	mV	0°C +25°C +75°C	Load = 50Ω to −2V
V_{OL}	Output LOW Voltage Q and $\overline{Q}$	−1820	−1705	−1620	mV	0°C to +75°C	
V_{IH}	Input HIGH Voltage	−1135 −1095 −1035		−840 −810 −720	mV	0°C +25°C +75°C	Guaranteed Input HIGH Signal (Note 6)
V_{IL}	Input LOW Voltage	−1870 −1850 −1830		−1500 −1485 −1460	mV	0°C +25°C +75°C	Guaranteed Input LOW Signal
I_{IH}	Input HIGH Current CP Input (Note 1) MS Input M_1 and M_2 Input			 400 400 250	 μA	 +25°C +25°C +25°C	$V_{IN} = V_{IHA}$
I_{IL}	Input LOW Current	0.5			μA	+25°C	$V_{IN} = V_{ILB}$
I_{EE}	Power Supply Current	−110 −119	−75		mA	0°C to +75°C	Pins 6, 7, 13 not connected
V_{EE}	Operating Supply Voltage Range	−5.7	−5.2	−4.7	V	0°C to +75°C	
V_{REF}	Reference Voltage	−1550		−1150	mV	+25°C	$V_{RM_1} = V_{RM_2} = -5.2V$ $I_N = -10.0\ \mu A$

AC Electrical Characteristics

T_A = 0°C to +75°C, $V_{CC} = V_{CCA} = GND$, $V_{EE} = -5.2V$

Symbol	Parameter	0°C Typ	+25°C			+75°C Typ	Units	Conditions
			Min	Typ	Max			
t_{PLH} t_{PHL}	Propagation Delay, (50% to 50%) CP to Q	1.8	1.3	2.0	3.0	2.5	ns	Output: R_L = 50Ω to −2.0V Input: $t_{ri} = t_{fi}$ = 2.0 ±0.1 ns (20% to 80%) See *Figure 1*
t_{PLH}	Propagation Delay, (50% to 50%) MS to Q	3.7		4.0	6.0	4.5	ns	
t_s	Setup Time, M to CP	2.0	4.0	2.0		2.0	ns	
t_h	Hold Time, M to CP	−2.0	0.0	−2.0		−2.0	ns	
t_{TLH}	Output Rise Time (20% to 80%)	1.0		1.0	2.0	1.0	ns	
t_{THL}	Output Fall Time (80% to 20%)	1.0		1.0	2.0	1.0	ns	
f_{MAX}	Maximum Clock Frequency	650	600	650		625	MHz	AC Coupled Input 350 mV Peak-to-Peak. f_{MAX} is Guaranteed to be 575 MHz Min at 0°C to +75°C.

ECL Operation—Military Version

DC Electrical Characteristics

$V_{CC} = V_{CCA} = GND$, $V_{EE} = -5.2V$

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions
V_{OH}	Output HIGH Voltage Q and $\overline{Q}$	−1100 −980 −910	−1030 −910 −820	−900 −820 −670	mV	−55°C +25°C +125°C	Load = 100Ω to −2V
V_{OL}	Output LOW Voltage Q and $\overline{Q}$	−1820	−1705	−1620	mV	−55°C to +125°C	
V_{IH}	Input HIGH Voltage	−1190 −1095 −975		−905 −810 −690	mV	−55°C +25°C +125°C	Guaranteed Input HIGH Signal (Note 6)
V_{IL}	Input LOW Voltage	−1890 −1850 −1800		−1525 −1485 −1435	mV	−55°C +25°C +125°C	Guaranteed Input LOW Signal
I_{IH}	Input HIGH Current CP Input (Note 1) MS Input M_1 and M_2 Input			 400 400 250	 μA	 +25°C +25°C +25°C	$V_{IN} = V_{IHA}$
I_{IL}	Input LOW Current	0.5			μA	+25°C	$V_{IN} = V_{ILB}$
I_{EE}	Power Supply Current	−110	−75		mA	+25°C	Pins 6, 7, 13 not connected
			−119		mA	−55°C to +125°C	
V_{EE}	Operating Supply Voltage Range	−5.7	−5.2	−4.7	V	−55°C to +125°C	
V_{REF}	Reference Voltage	−1550		−1150	mV	+25°C	$V_{RM_1} = V_{RM_2} = -5.2V$ $I_N = -10.0\ \mu A$

AC Electrical Characteristics

$T_A = -55°C$ to $+125°C$, $V_{CC} = V_{CCA} = GND$, $V_{EE} = -5.2V$

Symbol	Parameter	−55°C Typ	+25°C			+125°C Typ	Units	Conditions
			Min	Typ	Max			
t_{PLH} t_{PHL}	Propagation Delay, (50% to 50%) CP to Q	1.5	1.3	2.0	3.0	3.0	ns	Output: $R_L = 50\Omega$ to −2.0V Input: $t_{ri} = t_{fi} = 2.0 \pm 0.1$ ns (20% to 80%) See *Figure 1*
t_{PLH}	Propagation Delay, (50% to 50%) MS to Q	3.5		4.0	6.0	5.0	ns	
t_s	Setup Time, M to CP	2.0	4.0	2.0		2.0	ns	
t_h	Hold Time, M to CP	−2.0	0.0	−2.0		−2.0	ns	
t_{TLH}	Output Rise Time (20% to 80%)	1.0		1.0	2.0	1.0	ns	
t_{THL}	Output Fall Time (80% to 20%)	1.0		1.0	2.0	1.0	ns	
f_{MAX}	Maximum Clock Frequency	700	600	650		600	MHz	AC Coupled Input 350 mV Peak-to-Peak. f_{MAX} is Guaranteed to be 550 MHz Min at −55°C to +125°C.

Note 1: Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

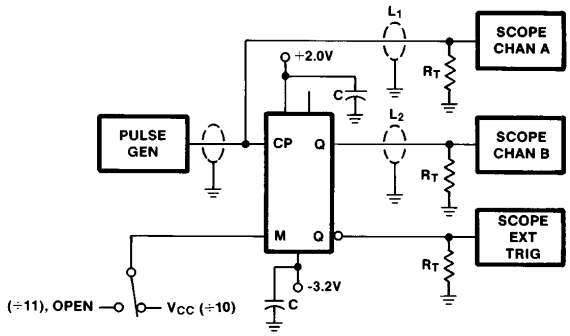
Note 2: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 3: Typical limits are at $V_{CC} = 5.0V$ and $T_A = +25°C$.

Note 4: The M_1 and M_2 threshold specifications are normally referenced to the V_{CC} potential, as shown in the ECL operation tables. Using V_{EE} (GND) as the reference, as in normal TTL practice, effectively makes the threshold vary directly with V_{CC}. Threshold is typically 1.3V below V_{CC} (e.g., +3.7V at $V_{CC} = +5V$). A signal swing about threshold of ±0.4V is adequate, which gives the state V_{IH} and V_{IL} values. The internal 2 kΩ resistors are intended to pull TTL outputs up to the required V_{IH} range, as discussed in the Functional Description and shown in *Figure 5*.

Note 5: TTL Output Signal swing is guaranteed at f_{MAX} over temperature range.

Note 6: M_1 or M_2 can be tied to V_{CC} for fixed divide-by-ten operation.



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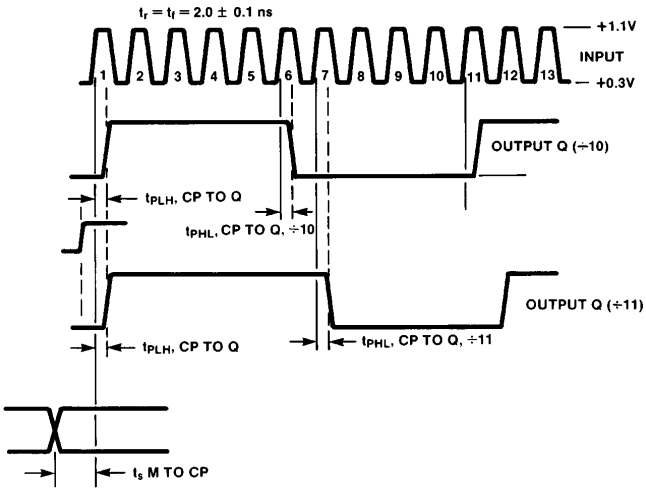

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Conditions:

V_{CC} = +2.0V
V_{EE} = −3.2V
R_T = 50Ω (scope input impedance)
C_L = Jig and stray capacitance < 5.0 pF
I_1 = L_2 = equal 50Ω impedance lines
C = 0.1 pF

Note 7: Use high impedance to test QTTL.
Connect pin 13 to V_{EE}.

Note 8: For High frequency test use AC coupled input as in *Figure 3*.
Adjust input amplitude to 350 mV peak-to-peak.

FIGURE 1. AC Test Circuit

Functional Description

The 11C90 contains four ECL Flip-Flops, an ECL to TTL converter and a Schottky TTL output buffer with an active pull-up. Three of the Flip-Flops operate as a synchronous shift counter driving the fourth Flip-Flop operating as an asynchronous toggle. The internal feedback logic is such that the TTL output and the Q ECL output are HIGH for six clock periods and LOW for five clock periods. The Mode Control (M) inputs can modify the feedback to make the output HIGH for five clock periods and LOW for five clock periods, as indicated in the Count Sequence Table.

The feedback logic is such that the instant the output goes HIGH, the circuit is already committed as to whether the output period will be 10 or 11 clock periods long. This means that subsequent changes in an M input signal, including decoding spikes, will have no effect on the current output period. The only timing restriction for an M input signal is that it be in the desired state at least a setup time before the clock that follows the HHLL state shown in the table. The allowable propagation delay through external logic to an M input is maximized by designing it to use the positive transition of the 11C90 output as its active edge. This gives an allowable delay of ten clock periods, minus the CP to Q delay of the 11C90 and the M to CP setup time. If the external logic uses the negative output transition as its active edge, the allowable delay is reduced to five clock periods minus the previously mentioned delay and setup time.

Capacitively coupled triggering is simplified by the 400Ω resistor which connects pin 15 to the internal V_{BB} reference. By connecting this to the CP input, as shown in *Figure 3*, the clock is automatically centered about the input threshold. A clock duty cycle of 50% provides the fastest operation, since the Flip-Flops are Master-Slave types with offset clock thresholds between master and slave. This feature ensures that the circuit will operate with clock waveforms having very slow rise and fall times, and thus, there is no maximum frequency restriction. Recommended minimum and maximum clock amplitude as a function of a frequency and temperature are shown in the graph labeled *Figure 2*. When the CP or any other input is driven from another ECL circuit, normal ECL termination methods are recommended. One method is indicated in *Figure 4*. Other ECL termination methods are discussed in the F100K ECL Design Guide (Section 5 of Databook).

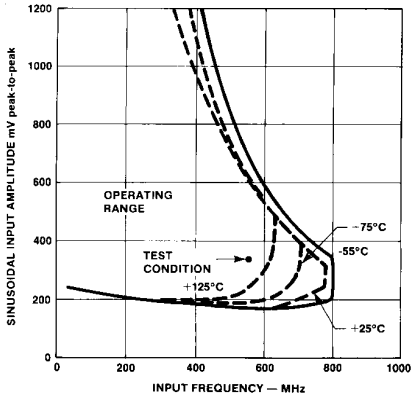

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FIGURE 2. AC Coupled Triggering Characteristics

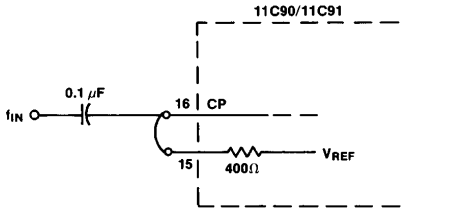

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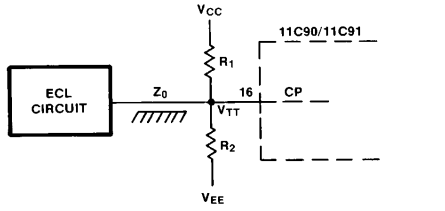
FIGURE 3. Capacitively Coupled Clocking



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$Z_O\Omega$	50	75	100
$R_1\Omega$	80.6	121	162
$R_2\Omega$	130	196	261

$V_{EE} = -5.2V$, $V_{CC} = 0V$, $V_{TT} = -2.0V$

FIGURE 4. Clocking by ECL Source via Terminated Line

When an M input is to be driven from a TTL output operating from the same V_{CC} and ground (V_{EE}), the internal 2 kΩ resistor can be used to pull the TTL output up as shown in *Figure 5*. Some types of TTL outputs will only pull up to within two diode drops of V_{CC}, which is not high enough for 11C90 inputs. The resistor will pull the signal up through the threshold region, although this final rise may be somewhat slow, depending on wiring capacitance. A resistor network that gives faster rise and also lower impedance is shown in *Figure 6*.

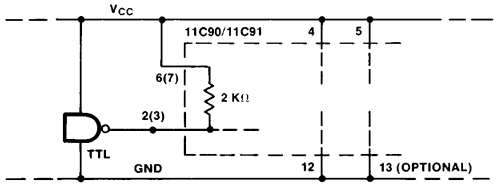

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FIGURE 5. Using Internal Pull-Up with TTL Source

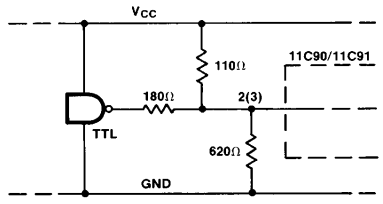

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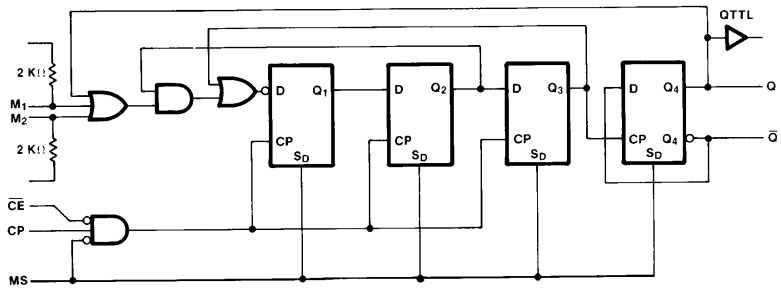
FIGURE 6. Faster Low Impedance TTL to ECL Interface

Functional Description (Continued)

The ECL outputs have no pull-down resistors and can drive series or parallel terminated transmission lines. For short interconnections that do not require impedance matching, a 270Ω to 510Ω resistor to V_{EE} can be used to establish the V_{OL} level. Both V_{CC} pins must always be used and should be connected together as close to the package as possible. Pin 12 must always be connected to the V_{EE} side of the supply, while pin 13 is required only if the TTL output is used. Low impedance V_{CC} and V_{EE} distribution and RF bypass capacitors are recommended to prevent crosstalk.

Logic Diagram 11C90



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Note: This diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than shown.

Count Sequence Table 11C90

	Q_1	Q_2	Q_3	Q_4(QTTL)	
	H	H	H	H	÷11
÷10	L	H	H	H	
	L	L	H	H	
	L	L	L	H	
	H	L	L	H	
	H	H	L	H	
	L	H	H	L	
	L	L	H	L	
	L	L	L	L	
	H	L	L	L	
	H	H	L	L	

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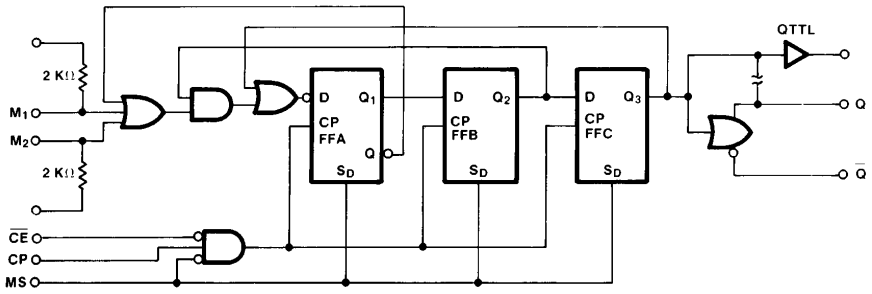
Note: A HIGH on MS forces all Qs HIGH.

Operating Mode Table 11C90

Inputs				Output Response
MS	$\overline{CE}$	M_1	M_2	
H	X	X	X	Set HIGH
L	H	X	X	Hold
L	L	L	L	÷11
L	L	H	X	÷10
L	L	X	H	÷10

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Logic Diagram 11C91



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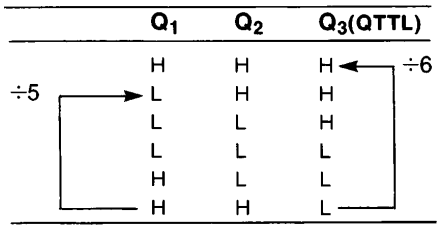
Count Sequence Table 11C91



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Note: A HIGH on MS forces all Qs HIGH.

Operating Mode Table 11C91

Inputs				Output Response
MS	$\overline{CE}$	M_1	M_2	
H	X	X	X	Set HIGH
L	H	X	X	Hold
L	L	L	L	÷6
L	L	X	H	÷5
L	L	H	X	÷5

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

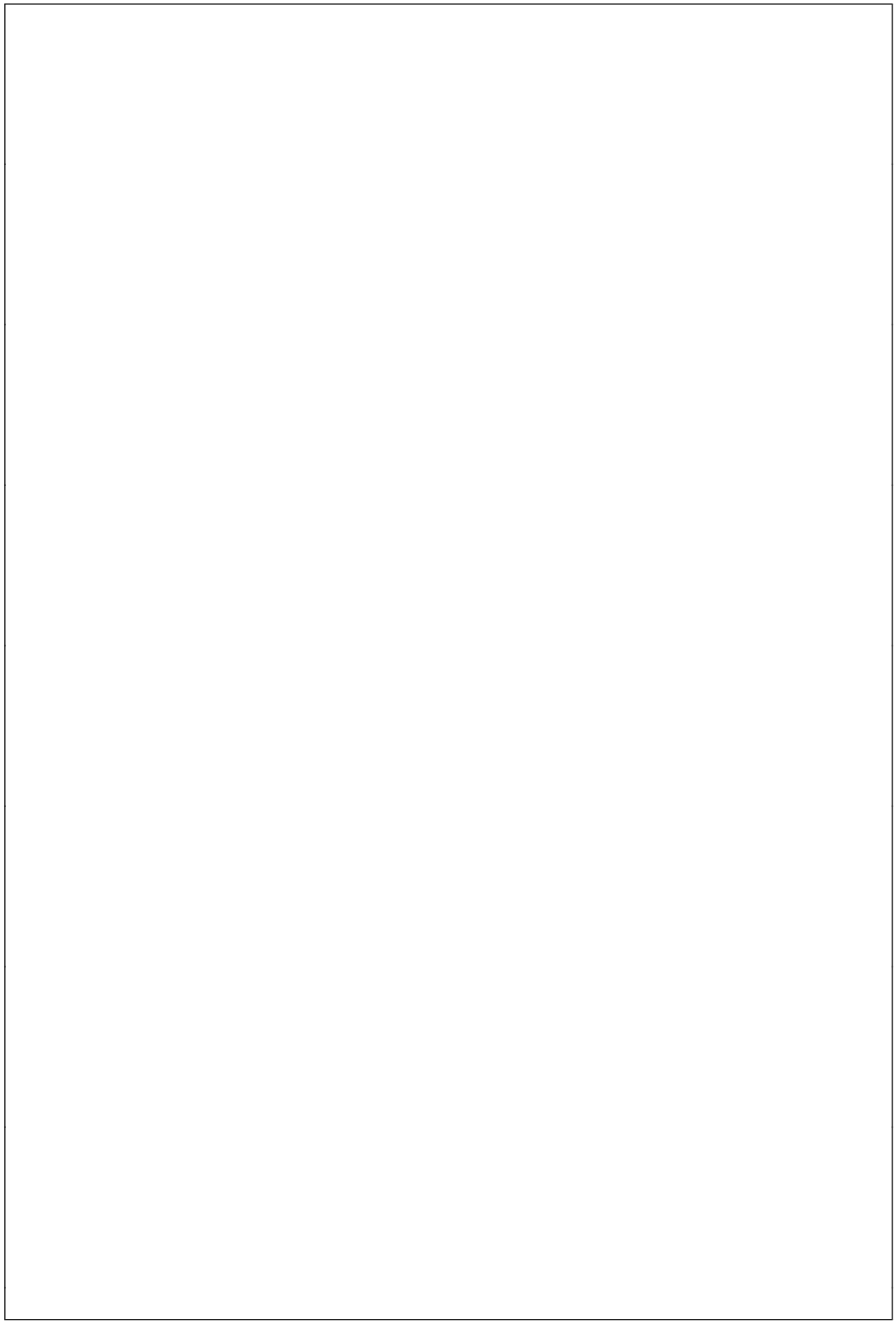
11C90/91 D C QR

Device Number (basic)

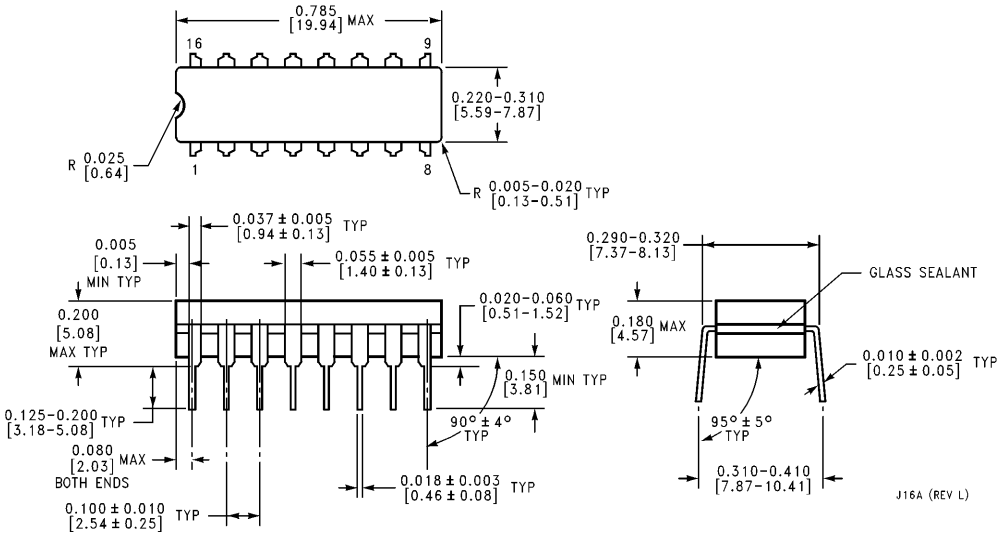
Package Code
D = Ceramic Dual In-Line

Special Variations
QR = Commercial grade device with burn-in

Temperature Range
C = Commercial (0°C to +85°C)



Physical Dimensions inches (millimeters)



16 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

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