THAT Corporation

InGenius® High-CMRR Balanced Input Line Receiver

THAT 1200, 1203, 1206

FEATURES

- High common-mode rejection (typical 90 dB at 60 Hz) maintained under real-world conditions
- Excellent solution for hum and groundloop suppression
- Transformer-like noise rejection in an 8-pin IC, at fraction of transformer cost and size

APPLICATIONS

- Balanced input stages
- Summing amplifiers
- Transformer front-end replacements
- ADC front-ends

Description

The THAT 1200 series of *InGenius* balanced line receivers are designed to overcome a serious limitation of conventional balanced input stages — notoriously poor common mode rejection in real world applications. While conventional input stages may exhibit good rejection characteristics in the lab and on paper, they perform poorly when fed from even slightly unbalanced source impedances — a common situation in almost any pro sound environment.

Developed by Bill Whitlock of Jensen Transformers, the patented *InGenius* input stage uses a unique bootstrap circuit to raise its common-mode input impedance into the megohm range, but without the noise penalty that comes from high-valued resistors. InGenius line receivers maintain their high CMRR over a wide range of source impedance imbalances — even when fed from single-ended sources.

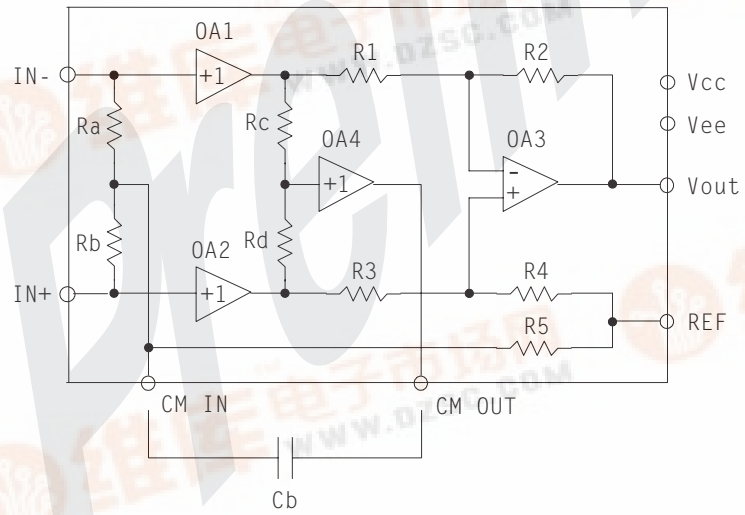


Figure 1. THAT1200-series equivalent circuit diagram

Pin Name	DIP Pin	SO Pin
Ref	1	3
In-	2	4
In+	3	5
Vee	4	6
CM In	5	11
Vout	6	12
Vcc	7	13
CM Out	8	14

Table 1. 1200-series pin assignments

Gain	Plastic DIP	Plastic SO
0 dB	1200P	1200S
-3 dB	1203P	1203S
-6 dB	1206P	1206S

Table 2. Ordering information

SPECIFICATIONS[1]

Absolute Maximum Ratings (T_A = 25°C)

Positive Supply Voltage (V_{CC})	+18 V	Power Dissipation (P_D) (T_A = 75°C)	TBD mW
Negative Supply Voltage (V_{EE})	-18 V	Operating Temperature Range (T_{OP})	0 to +70°C
Positive Input Voltage (V_{IN+})	+18 V	Storage Temperature Range (T_{ST})	-40 to +125°C
Negative Input Voltage (V_{IN-})	-18 V	Junction Temperature (T_J)	150°C
Output Short-Circuit Duration (t_{SH})	Continuous	Lead Temperature (Soldering 60 seconds)	TBD °C

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Positive Supply Voltage	V_{CC}		+3		+18	V
Negative Supply Voltage	V_{EE}		-3		-18	V

Electrical Characteristics[2]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current	I_{CC}	No signal	—	4.7	8.0	mA
Input Bias Current	I_B	No signal; Either input connected to GND	—	700	1,400	nA
Input Offset Current	I_{B-OFF}	No signal	—	—	±140	nA
Input Offset Voltage	V_{OFF}	No signal	—	—	10	mV
Input Voltage Range	V_{IN-CM}	Common mode	±12.5	±13.0	—	V
	$V_{IN-DIFF}$	Differential (equal and opposite swing)				
		THAT 1200	21.0	21.5	—	dBu
		THAT 1203	24.0	24.5	—	dBu
		THAT 1206	24.0	24.5	—	dBu
Input Impedance	$Z_{IN-DIFF}$	Differential		48.0		kΩ
	Z_{IN-CM}	Common mode		with bootstrap		
		60 Hz		10.0		MΩ
		20 kHz		3.2		MΩ
				no bootstrap		
		60 Hz		36.0		kΩ
		20 kHz		36.0		kΩ

1. All specifications are subject to change without notice.
2. Unless otherwise noted, T_A=25°C, V_{CC} = +15V, V_{EE} = -15V
3. 0 dBu = 0.775Vrms.

Electrical Characteristics (Cont'd)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Common Mode Rejection	CMR_1	Matched source impedances; V_{CM} = ±10V				
		DC	70	90	—	dB
		60 Hz	70	90	—	dB
		20 kHz	—	85	—	dB
Common Mode Rejection	CMR_2	600Ω unmatched source impedances[4]; V_{CM} = ±10V				
		60 Hz	—	70	—	dB
		20 kHz	—	65	—	dB
Power Supply Rejection[5]	PSR	At 60 Hz, with V_{CC} = -V_{EE}				
		THAT1200	—	82	—	dB
		THAT1203	—	80	—	dB
		THAT1206	—	80	—	dB
Power Supply Rejection[6]	PSR_{CM}	At CM output, at 60 Hz	—	63	—	dB
Total Harmonic Distortion	THD	$V_{IN-DIFF}$ = 10 dBV; BW = 20 kHz; f = 1 kHz				
		RL =2 kΩ	—	0.0005	—	%
Output Noise	$e_{n(OUT)}$	BW = 20 kHz				
		THAT1200	—	-106	—	dBu
		THAT1203	—	-105	—	dBu
		THAT1206	—	-107	—	dBu
Output Noise	$e_{nCM(OUT)}$	At CM output	—	-106	—	dBu
Slew Rate	SR	R_L = 10 kΩ; C_L = 300 pF	7*	12	—	V/µs
Slew Rate	SR_{CM}	With CM input signal R_{Lcm} = 10 kΩ; C_{Lcm} = 50 pF	12.5*	21	—	V/µs
Small Signal Bandwidth	BW_{-3dB}	R_L = 10 kΩ; C_L = 10 pF				
		THAT1200	—	22	—	MHz
		THAT1203	—	27	—	MHz
		THAT1206	—	34	—	MHz
		R_L = 2 kΩ; C_L = 300 pF				
		THAT1200	—	17	—	MHz
		THAT1203	—	18	—	MHz
		THAT1206	—	20	—	MHz
Small Signal Bandwidth	BW_{CM-3dB}	At CM output; R_{Lcm} = 10 kΩ				
		C_{Lcm} = 10 pF	—	20	—	MHz
		C_{Lcm} = 50 pF	—	18	—	MHz
Output Gain Error	$G_{ER(OUT)}$	f = 1 kHz; R_L = 2 kΩ	—	0	±0.05	dB
Output Voltage Swing	V_O	At max differential input				
		THAT1200	21	21.5	—	dBu
		THAT1203	21	21.5	—	dBu
		THAT1206	18	18.5	—	dBu

4. See test circuit in Figure 2.
5. Defined with respect to the differential gain.
6. Defined with respect to the common mode gain between any input and common mode output.

* Guaranteed by design

Electrical Characteristics (Cont'd)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Short Circuit Current	I_{SC}	$R_L = R_{Lcm} = 0\ \Omega$	—	±25	—	mA
	I_{CMSC}	At CM output	—	±10	—	mA
Minimum Resistive Load	R_{Lmin}		2	—	—	kΩ
	R_{LCMmin}	At CM output	10	—	—	kΩ
Maximum Capacitive Load	C_{Lmax}		—	—	300	pF
	C_{LCMmax}	At CM output	—	—	50	pF

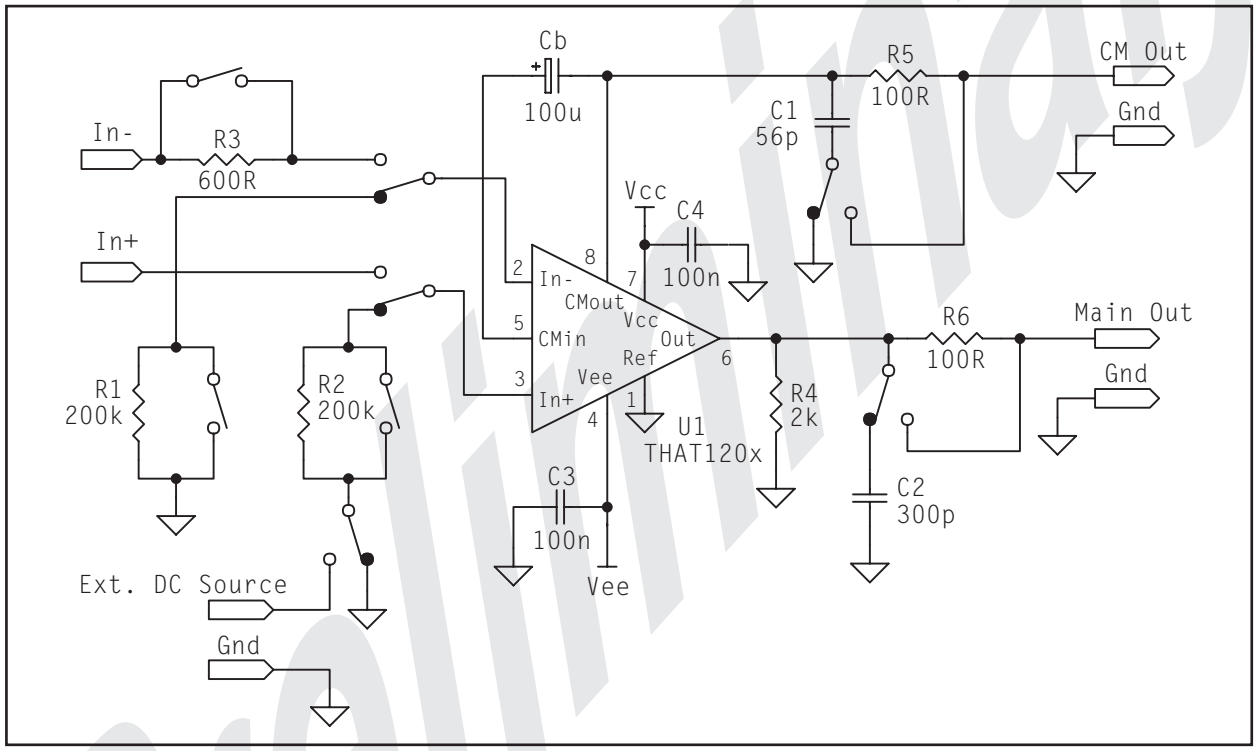


Figure 2. THAT1200-series test circuit

Applications

RFI Protection

Figure 3 shows the THAT 1200 configured with robust RFI input protection. In applications where RFI rejection is of less concern, the circuit shown Figure 4 provides a less aggressive approach.

Bootstrap coupling capacitor

Referring to Figure 3, electrolytic capacitor Cb provides the feedback path for the boostrap circuit. The capacitor value is chosen to be high enough to present a sufficiently small impedance to signals at the low end of the audio spectrum. Its voltage rating is dependent on the topology of the surrounding circuitry, as described in the following paragraphs.

AC signals presented to the input stage cause the two ends of capacitor Cb to swing in tandem so that virtually no voltage appears across the capacitor. Consequently, capacitors with small DC working voltages may be used when the previous stage is AC coupled to the input of the THAT 1200.

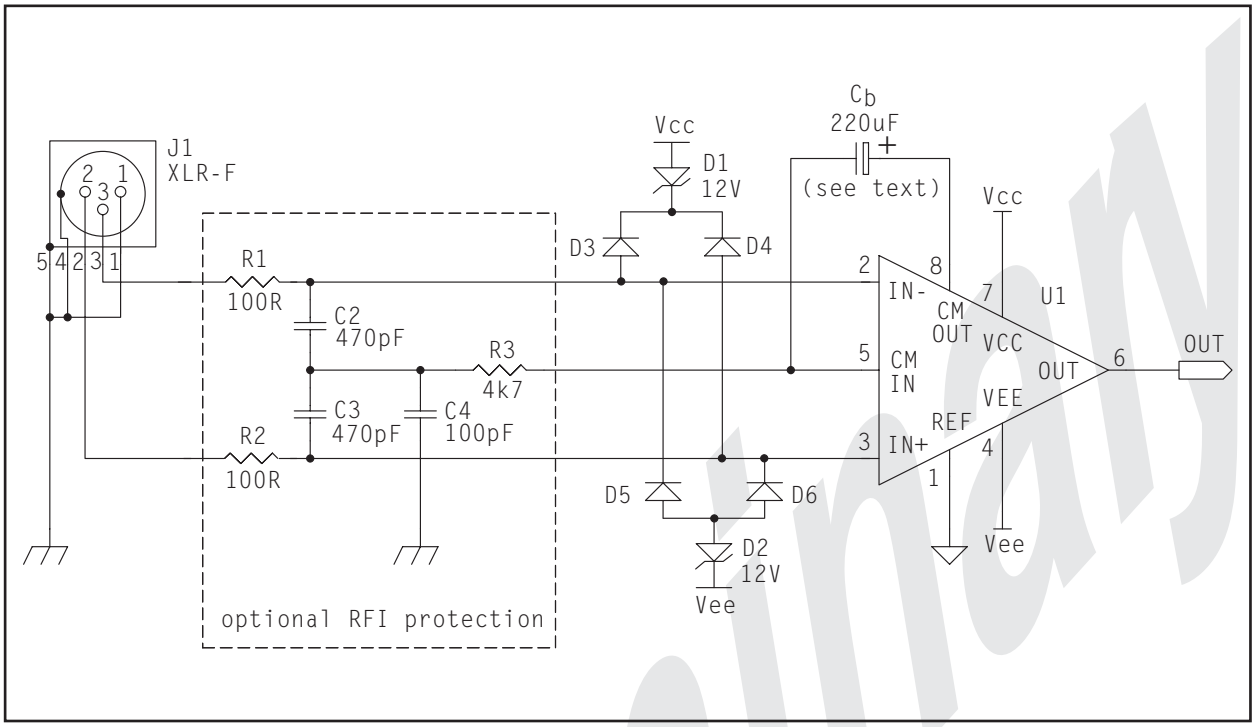


Figure 3. THAT1200P typical application circuit

If, however, there is the possibility of a DC voltage appearing across the inputs of the line receiver, a portion of that voltage will appear directly across the terminals of capacitor Cb. In that case, choose the capacitor's voltage rating so that it is capable of handling the expected level of DC voltage. If the polarity of the DC voltage is unknown, or may swing to either polarity, the use of a non-polarized electolytic is highly recommended.

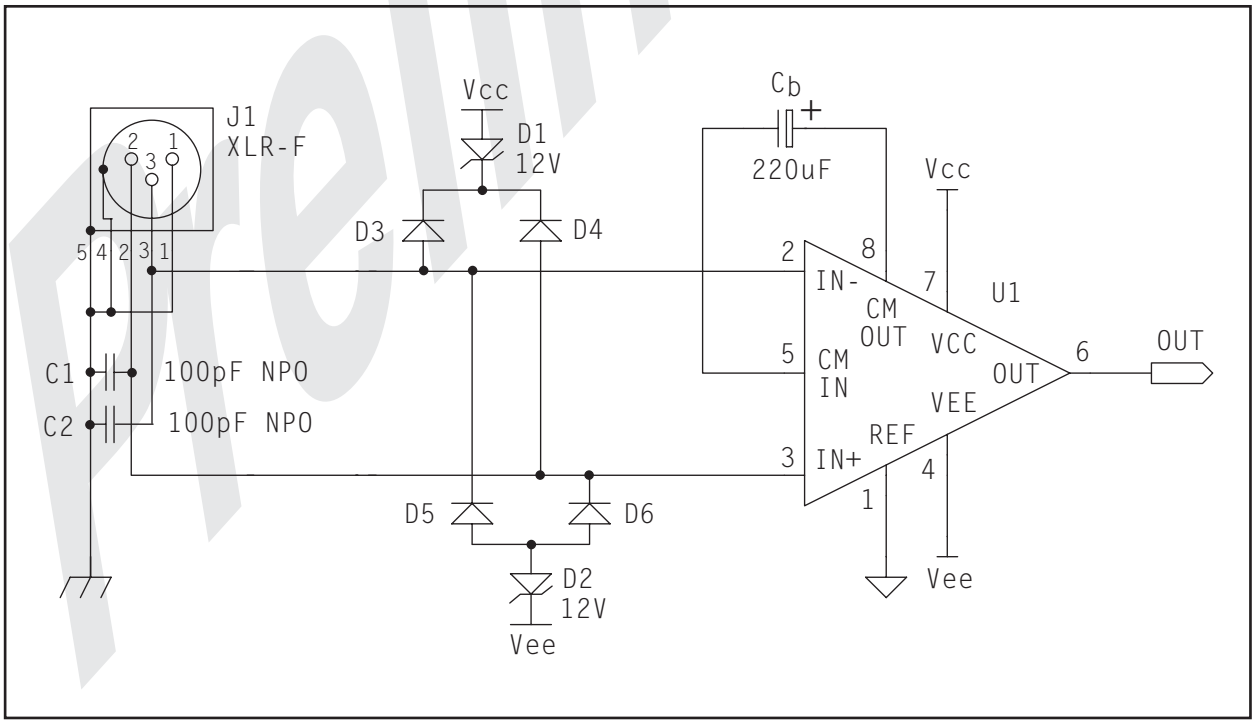


Figure 4. THAT1200P showing simplified RFI protection scheme

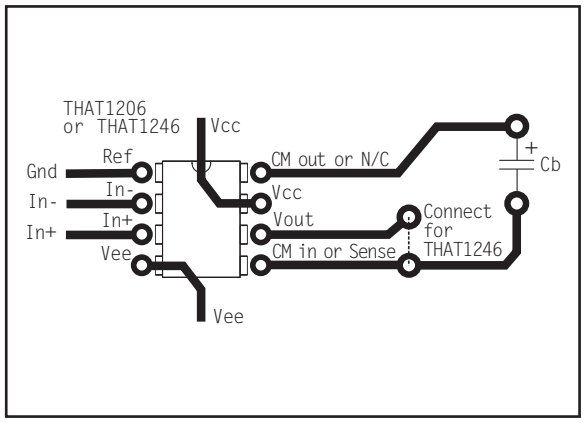


Figure 5. Dual PCB layout for THAT 1206 and THAT 1246 DIP version

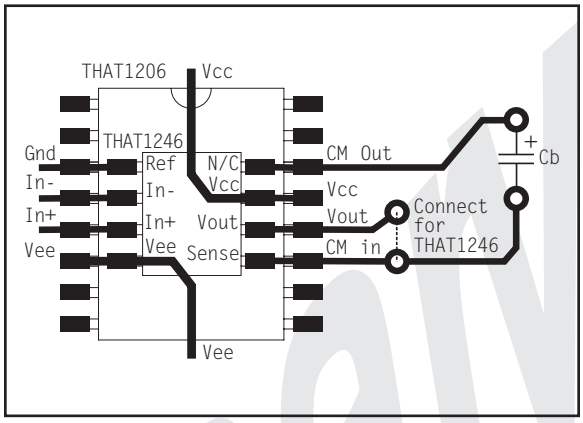


Figure 6. Dual PCB layout for THAT 1206 and THAT 1246 Surface mount versions

Dual Layout Option

The THAT 1246 is a conventional balanced line-receiver that is pin-for-pin compatible with the Analog Devices SSM2143 and Burr-Brown INA137. Though the THAT 1200 series is not pin-compatible with the THAT 1246, the PCB layouts shown in Figures 5 and 6 provide manufacturers with the option to stuff a PCB with any of these input stages. Note that these figures are not to scale. The interconnects should be as short as practicable constrained only by component size and relevant manufacturing considerations.

When a THAT 1200 series IC is installed, capacitor Cb is connected between CM In and CM Out. When the THAT 1246 (or SSM2143 or INA137) is used, capacitor Cb is removed, and a jumper connects the Vout and Sense pins.

Input Protection

Figure 7 shows the internal overvoltage protection circuitry at the IN+, IN-, and CM IN pins. The values of R and R' vary with actual part number as shown in Table 3.

While the internal protection circuitry shown is adequate to keep the combination of signal and common mode voltages from driving the internal inputs beyond the power supply rails, the circuitry does not provide adequate protection against most ESD incidents. Since these ICs will very often connect directly to the outside world, it is mandatory that additional, external protection from ESD be provided. Any unprotected InGenius input will fail when subjected to ESD if this protection circuitry is omitted. Additionally, proper ESD handling precautions must be observed until the IC is properly affixed to the PCB.

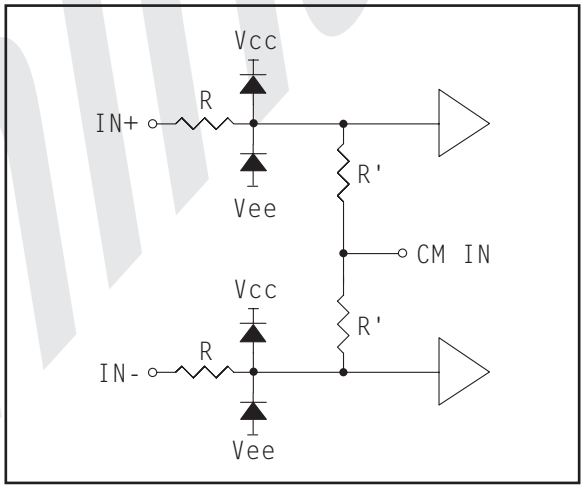


Figure 7. Internal input protection circuitry (see text)

Part No.	R	R'
THAT 1200	500Ω	23.5kΩ
THAT 1203	7kΩ	17kΩ
THAT 1206	7kΩ	17kΩ

Table 3. Input resistance values

Diodes D1-D6 in figures 3 and 4 show our recommended approach to protecting the 1200 series from ESD damage. This arrangement of 1N4148s and 12V Zener diodes permits the maximum allowable input signal to reach the IC's input pins, but directs high-energy ESD impulses to the rails. So long as the supply rails are adequately decoupled, most ESD events will be diminished to harmless levels.

Theory of Operation

Conventional high-CMRR balanced input stages cancel common-mode interference using a differential amplifier with matched (trimmed) resistance elements (Figure 8). When driven from a true voltage source, these conventional stages offer extremely high CMRR (>80dB). However, when driven from real-world sources, the CMRR of these stages degrades rapidly for even small source impedance imbalances.

The reason why this occurs is easily shown. Figure 9 shows that a voltage divider is formed between the impedance of the external signal source and the input impedance of the differential amplifier. For perfectly balanced source impedances (Rs1 = Rs2), and perfectly balanced input impedances (Ri1 = Ri2), the voltage dividers formed at each node ($\frac{Ri1}{Ri1+Rs1}$ and $\frac{Rs2}{Ri2+Rs2}$) will be equal to each other, so the conventional input stage will maintain high CMRR.

However, if the source impedances are not precisely equal, the voltage divider action will result in unequal signals at the plus and minus inputs of the input stage. In this case, no amount of CMRR is sufficient to reject the differential voltage that is generated by the impedance mismatch.

To illustrate, consider Figure 10. A common mode input signal is shown as Vcm. It couples to the positive and negative input of the balanced line receiver via Rs1 and Rs2, repectively. Typically, conventional balanced line receivers have common-mode input impedances of approximately 10 kΩ. In such cases, a source impedance imbalance of only 10 Ω can degrade CMRR to about 65 dB. A 10 Ω mismatch may be easily caused by tolerances in coupling capacitors or output resistors, and variations in contact and wire resistance. The situation becomes even worse when a conventional balanced line receiver is driven from an unbalanced source.

The best solution to this problem is to increase the line receiver's common-mode input impedance enough to minimize the imbalanced voltage divider effect, preferably on the order of several megohms. However, with a conventional differential amplifier, this requires the use of high resistances in the circuit. High resistance carries with it a high noise penalty, making this straightforward approach impractical for quality audio devices.

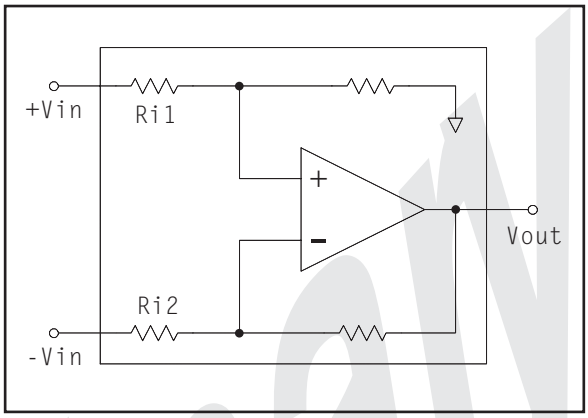


Figure 8. Basic differential amplifier

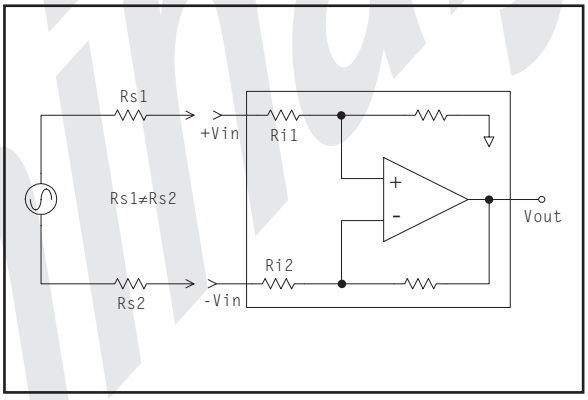


Figure 9. Basic differential amplifier showing mismatched source impedances

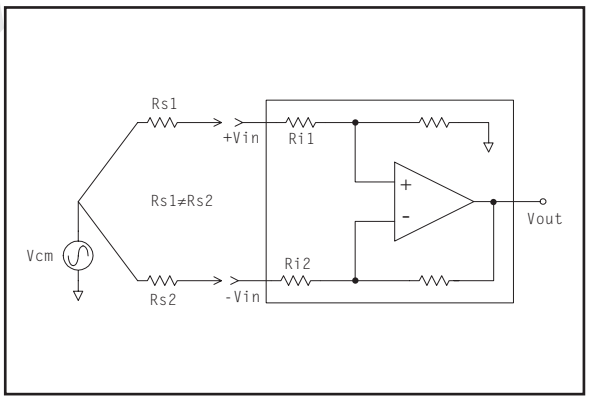


Figure 10. Basic differential amplifier driven by common-mode input signal

An alternative approach is to use the classic instrumentation amplifier configuration shown in Figure 11. In this circuit, the common-mode input impedance is the parallel combination of Ri1 and Ri2. Unfortunately for this approach, to achieve multi-megohm input impedances, the input devices used in the input amplifiers must have extremely low

bias currents since their input bias flows through Ri1 and Ri2. Because of the difficulty of maintaining low noise with low input bias currents, FET op amps may be employed, but they impose their own limitations, as described further on.

The THAT 1200 series of balanced line receivers overcomes this problem by way of an AC bootstrap technique, shown in simplified form in Figure 12. By driving the lower end of R2 to nearly the same AC voltage as the upper end, AC current flow through R2 is greatly reduced, effectively increasing its value. At DC, of course, the input impedance Z is simply R1 + R2. If gain G is unity, for frequencies within the passband of the high-pass filter formed by Cb and R1, the effective value of the input impedance is increased to infinity at sufficiently high frequencies.

Input impedance Z, at frequency f, is described the following equation:

$$Z_i = (R1 + R2)\sqrt{\frac{1+(\frac{f}{fn})^2}{1+(1-G)^2(\frac{f}{fD})^2}}$$

where

$$f_N = \frac{1}{2\pi(\frac{R1\times R2}{R1+R2})C}, \quad f_D = \frac{1}{2\pi R1C}$$

For example, if R1 and R2 are 10 kΩ each, Z_{DC} is 20 kΩ. This resistance provides a DC path for amplifier bias current as well as leakage current that might flow from a signal source. At higher frequencies, the bootstrap greatly increases the input impedance, limited ultimately by how close gain G approaches unity. With the THAT 1200 input stages, common-mode input impedances of several megohms across much of the audio spectrum can be expected.

Figure 1 shows a complete equivalent circuit for the THAT 1200-series ICs. OA1 and OA2 are high-impedance buffers feeding differential amplifier OA3 in an instrumentation amplifier configuration. The common mode signal is extracted at the junction of Rc and Rd, buffered by OA4, and fed back to both inputs via capacitor Cb and resistors Ra and Rb. The junction of Ra, Rb and R5 is driven to the same potential as the common-mode input voltage. Hence no common-mode current flows in resistors Ra and Rb. Since, ideally, no current flows, the input impedance to common mode signals is infinite.

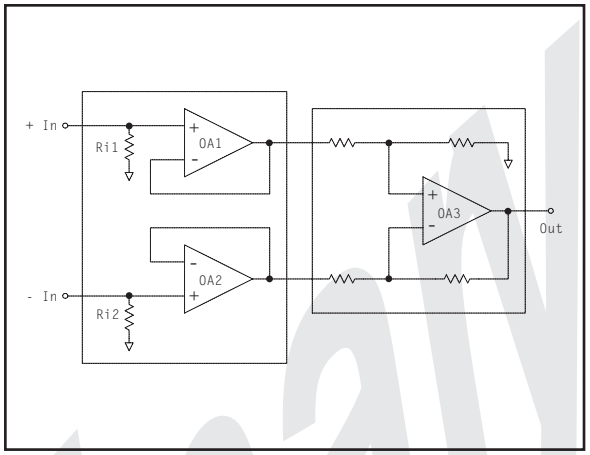


Figure 11. Instrumentation amplifier

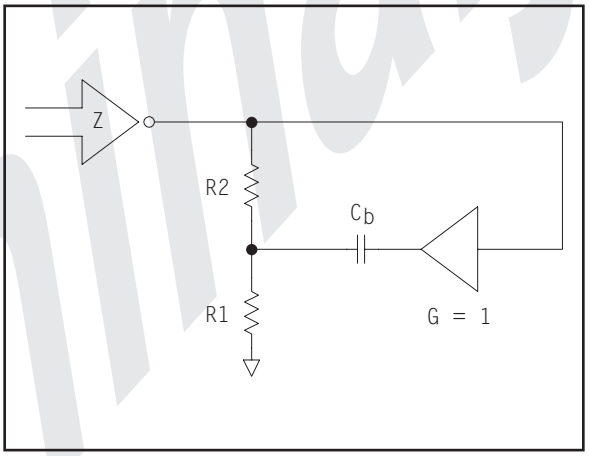


Figure 12. InGenius bootstrap topology

The effectiveness of this topology is limited by the unity gain precision of OA4 and the input impedances of OA1 and OA2, all of which are optimized in THAT's integrated circuit process. Note that OA1 and OA2 isolate OA3 from external source impedances. Therefore, the performance of the differential amplifier OA3 and its associated components are not affected by imbalances in the source impedances.

Alternatives

In the following section we will compare other solutions for minimizing CMRR degradation in the presence of source impedance mismatch, and contrast them with THAT's *InGenius* topology.

Precision 4-resistor op amp stage

This stage (Figure 8) was discussed earlier. To summarize, this solution offers high common-mode rejection only when the source impedances are perfectly balanced, or a tiny fraction of the common-mode input impedance. Because differential- and

common-mode input impedances are inextricably linked, and of similar magnitude, it is not possible to increase common-mode input impedance without compromising noise performance.

3-op amp instrumentation amplifier

This topology, shown in Figure 11, was also discussed earlier. It relies on input buffers OA1 and OA2 to raise the common-mode *and* differential-mode input impedances. The following diff amp, OA3 (which can be of the precision 4-resistor op amp type), is then used to reject the common-mode signal while extracting the differential signal.

This approach will require reasonably low values for Ri1 and Ri2 (< 100 kΩ or so) unless the OA1 and OA2 use FETs at their inputs. This would limit the common-mode input impedance to a few hundred kilohms.

If FET-input devices are used for OA1 and OA2, Ri1 and Ri2 can be made quite large — on the order of 10 megohms. Unlike the resistors in the conventional diff amp stage, these resistors will be shunted by the driving source impedance, and so contribute negligible noise.

At first glance, this might seem to be an excellent solution. However, there are disadvantages to this approach. First, the designer must select a FET-input op amp that is low-noise *and* that exhibits no phase inversion (sign reversal) with large differential- and common-mode signal swings. This, of course, results in a cost penalty that is somewhat exacerbated by the price premium for high-value resistors.

Second, this design requires at least two IC packages — a dual FET op amp and the precision input stage.

Third, while the large-value input resistances are shunted when there is a source connected to the input, there is no guarantee that long cables will always be properly terminated. With an unterminated cable plugged into the associated XLR jack, Ri1 and Ri2 are no longer shunted and become not only large noise sources themselves, but will do little to reduce pickup on the cable.

The THAT 1200-series input stages avoid these problems altogether. They exhibit high common-mode input impedance as a result of their bootstrapped topology, while maintaining reasonable differential input resistances that can be left unshunted with no fear of stray pickup or excessive noise contribution.

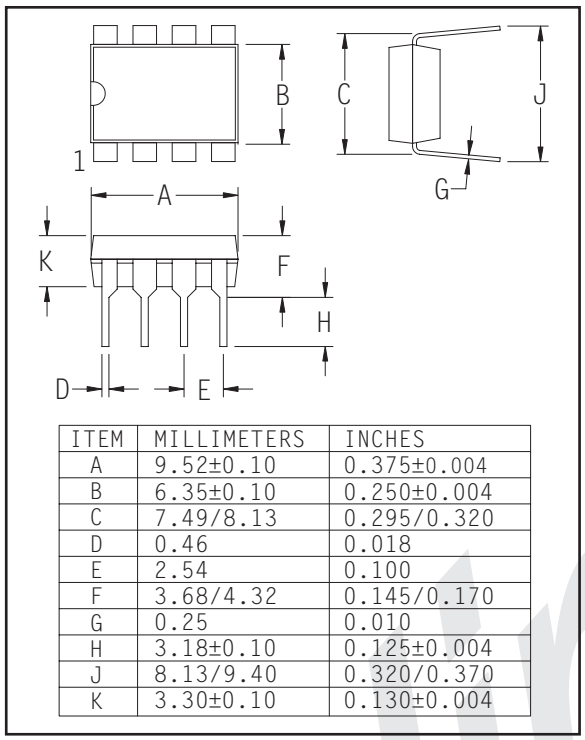
Transformers

When true electrical isolation is required, a transformer may be the only solution. Transformers suitable for pro audio, however, tend to be costly and take up valuable board real estate. In addition, some transformers can color the sound in ways that electronic solutions do not.

Fortunately, it is usually not the case that galvanic isolation is required, and in most cases it is the common-mode signal rejection properties of a transformer that is sought after. By providing the high common-mode input impedance of a transformer with the size and cost of an 8-pin integrated circuit, the THAT 1200-series provides designers with an alternative that provides excellent interference rejection in real-world applications.

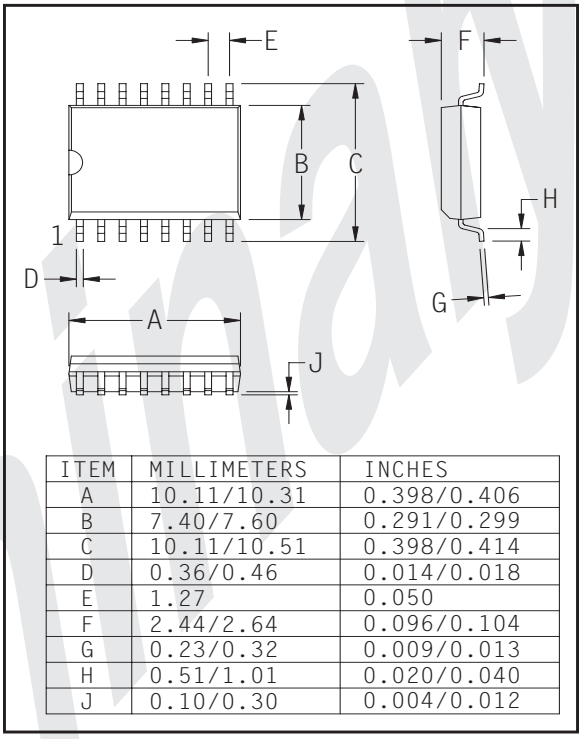
Package Information

The THAT 1200 series is available in both 8-pin mini-DIP and 16-pin SOIC packages. The package dimensions are shown in Figures 13 and 14, while pinouts are given in Table 1.



ITEM	MILLIMETERS	INCHES
A	9.52±0.10	0.375±0.004
B	6.35±0.10	0.250±0.004
C	7.49/8.13	0.295/0.320
D	0.46	0.018
E	2.54	0.100
F	3.68/4.32	0.145/0.170
G	0.25	0.010
H	3.18±0.10	0.125±0.004
J	8.13/9.40	0.320/0.370
K	3.30±0.10	0.130±0.004

Figure 13. -P (DIP) version package outline drawing



ITEM	MILLIMETERS	INCHES
A	10.11/10.31	0.398/0.406
B	7.40/7.60	0.291/0.299
C	10.11/10.51	0.398/0.414
D	0.36/0.46	0.014/0.018
E	1.27	0.050
F	2.44/2.64	0.096/0.104
G	0.23/0.32	0.009/0.013
H	0.51/1.01	0.020/0.040
J	0.10/0.30	0.004/0.012

Figure 14. -S (SO) version package outline drawing