成越科技股份有限公司
Cheng Yue Technology Inc.

DigiTron Technology Limited
迪創科技有限公司

CY2890-D04
Digital TFT-LCD Panel Timing Controller

Resolution : 800 x 600, 640 x 480, 800 x 480, 1024 x 600
1024 x 768, 720 x 480, 320 x 240, 480 x 272

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Revision History

Version	DATE	Description
1.8	2007/09/20	Preliminary Datasheet

Ordering Information

Part No.	Package	Descriptions
CY2890-D04	64pin LQFP, Green package	7x7x1.4mm

Content

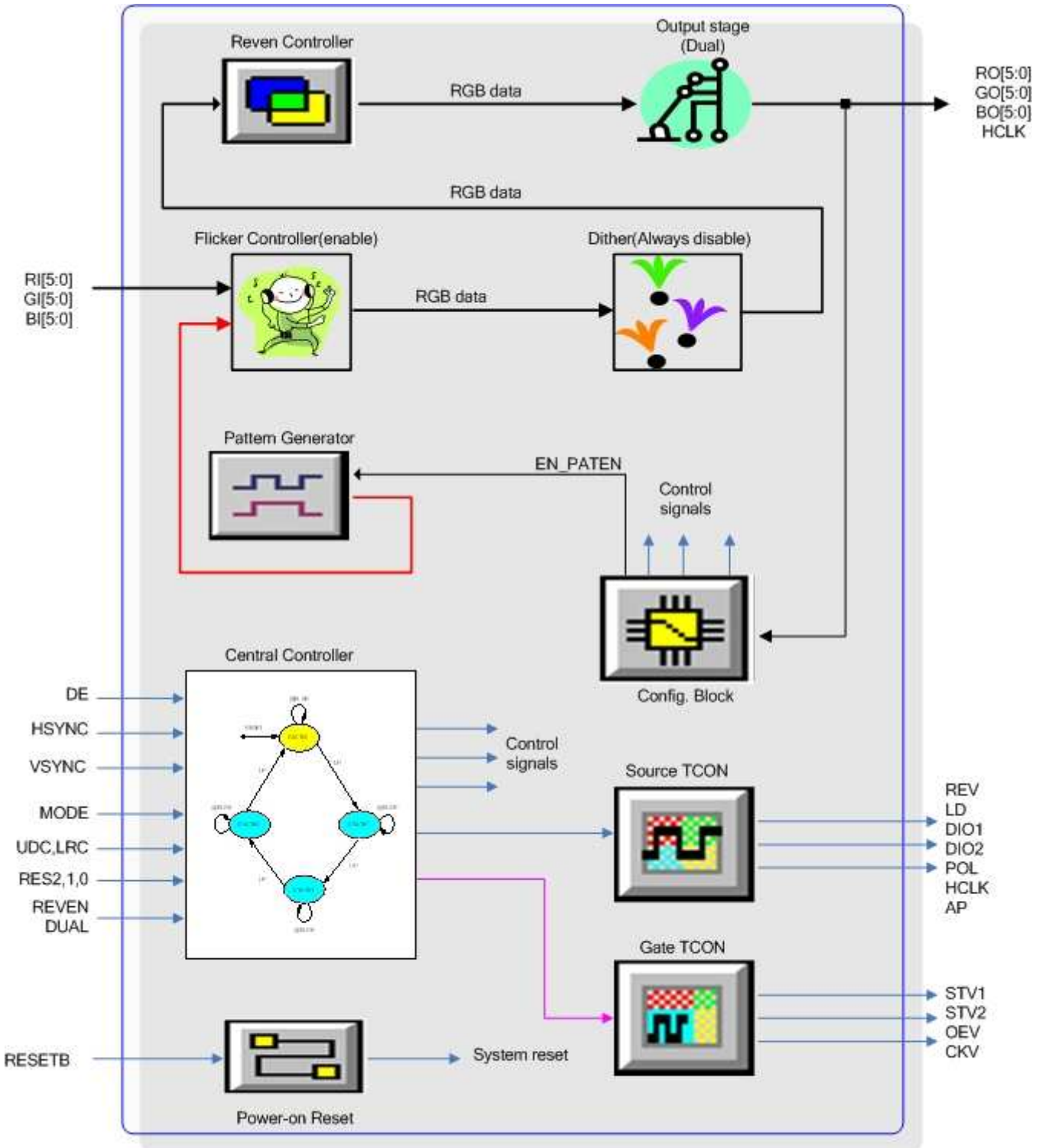
1. General Description

The CY2890-D04 is a digital TFT-LCD timing controller with built-in “reverse”, “dual”, “flicker”, “AP” and “pattern generator” functions. The input signal is digital R/G/B with HSYNC/VSYNC or DE. User can use the MODE pin to select input signal to be either HSYNC mode or DE mode. The R/G/B input is fixed to 6bits data width and the output is always 6 bits. No dither function is on in this chip. The Reverse function is always on which is designed for reducing EMI. The key is to lower down the R/G/B transition count. The “dual” function can set the output HCLK to latch the output data at both edges. Set “dual” on can lower down the HCLK frequency to half. With the “Reverse” and “dual” functions, the board level system design can be relaxed. We also have a built-in test pattern generator for users to do a quick final test or aging burning test. The built-in test pattern generator has 24 very popular patterns. It will be free running when MODE = 1, HSYNC = 1 or MODE = 0, DE = 1. You can stop the free-running built-in test pattern at any time. The “flicker” function is used to reduce the flicker phenomenon. For CY2890-D04, we have three dedicate RES pins to select different panel resolutions. Through CY2890-D04, all the necessary horizontal and vertical control signals to TFT-LCD are handled automatically. This includes the polarity invert control. There is a built-in power-on reset circuit in the chip, no need for user to add external reset circuit. If users want to extend the power-on reset, an external capacitor can be added.

2. Features

- Supporting 8 kinds of different digital TFT-LCD panels, clock frequency up to 85M Hz
  800 x 480 , 640 x 480, 800 x 600, 1024 x 600, 1024 x 768, 720 x 480, 320 x 240, 480 x 272
- Support HSYNC mode or DE mode
- FLICKER reduction function.
- Support DUAL edge function
- Support output data REVERSE function.
- Support AP function.
- UDC/LRC scan control
- Built-in test pattern generator with 24 popular patterns
- Built-In Power-On reset circuit
- Built-in polarity inverted function.
- Provide source and gate drivers control timing.
- Master clock frequency:75 MHz max.
- Single supply voltage : +3.0V to +3.6V
- Wide temperature operation range -40°C / +95°C
- ESD above 4K
- 64 LQFP Green Package

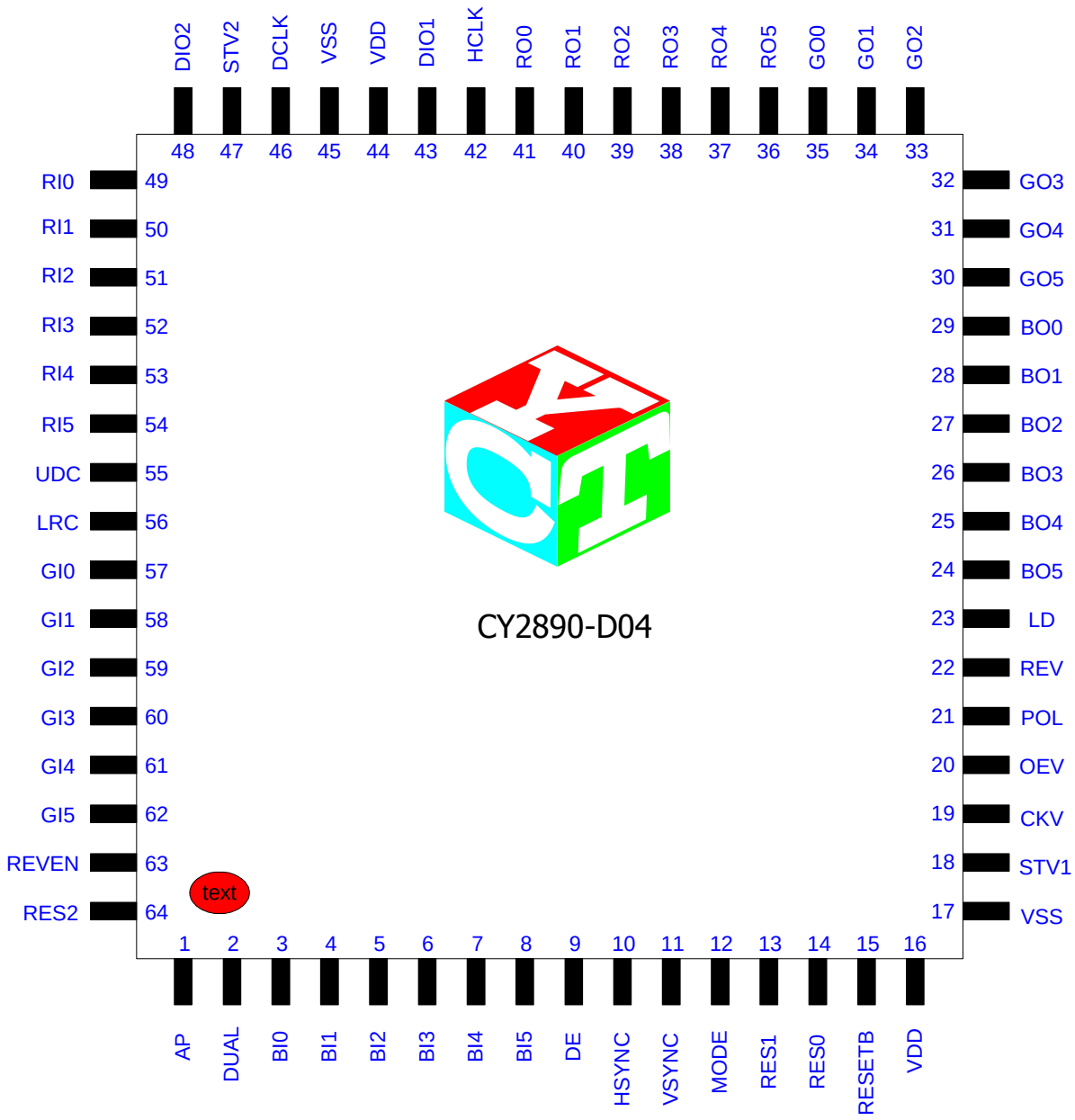
3. Block Diagram



CY2890-D03 Block Diagram

4. Pin Assignment

Pin Assignment for CY2890-D04



5. Pin Description

Pin No.	Symbol	I/O	Description	Internal
1	AP	O	AP out	
2	DUAL	I	Enable dual function H : enable L : disable	pull-down
3	BI0	I	Blue color data input, bit0.	
4	BI1	I	Blue color data input, bit1.	
5	BI2	I	Blue color data input, bit2.	
6	BI3	I	Blue color data input, bit3.	
7	BI4	I	Blue color data input, bit4.	
8	BI5	I	Blue color data input, bit5 (MSB).	
9	DE / ENPG	I	MODE = H : Data enable signal input, active high MODE = L : enable built-in pattern generator when Set to High, Stop when set to Low.	pull-down
10	HSYNC / ENPG	I	MODE = L : Negative polarity horizontal sync input MODE = H : enable built-in pattern generator when Set to High, Stop when set to Low.	pull-down
11	VSYNC / TEST	I	Negative polarity vertical sync input When set mode to DE, this pin must be floating or connected to ground. Tie to VDD at DE mode will force the chip to enter test mode.	pull-down
12	MODE	I	DE / SYNC mode select H : DE mode L : SYNC mode	pull-up
13	RES1	I	Resolution select bit 1	pull-up/down
14	RES0	I	Resolution select bit 0	pull-up/down
15	RESETB	I	Active low system reset pin Set low will reset the CY2890.	pull-up
16	VDD	I	Power supply voltage.	
17	VSS	I	Power supply ground.	
18	STV1	I/O	Gate driver start pulse 1. UDC = 0, Tri-state UDC = 1, Output	
19	CKV	O	Gate driver shift clock.	
20	OEV	O	Gate driver output enable	
21	POL	O	Source driver polarity select	
22	REV	O	Source driver data reverse control.	
23	LD	O	Source driver latch pulse and output enable.	
24	BO5	O	Blue color data output, bit5 (MSB).	
25	BO4	O	Blue color data output, bit4.	
26	BO3	O	Blue color data output, bit3.	
27	BO2	O	Blue color data output, bit2.	
28	BO1	O	Blue color data output, bit1.	
29	BO0	O	Blue color data output, bit0 (LSB).	
30	GO5	O	Green color data output, bit5 (MSB).	

Pin No.	Symbol	I/O	Description	Internal
31	GO4	O	Green color data output, bit4.	
32	GO3	O	Green color data output, bit3.	
33	GO2	O	Green color data output, bit2.	
34	GO1	O	Green color data output, bit1.	
35	GO0	O	Green color data output, bit0. (LSB).	
36	RO5	O	Red data output, bit5 (MSB).	
37	RO4	O	Red color data output, bit4.	
38	RO3	O	Red color data output, bit3	
39	RO2	O	Red color data output, bit2.	
40	RO1	O	Red color data output, bit1.,	
41	RO0	O	Red color data output, bit0. (LSB)	
42	HCLK	O	Source driver clock	
43	DIO1	I/O	Source driver start pulse 1 LRC = 0, Tri-state LRC = 1, Output	
44	VDD	I	Power supply voltage.	
45	VSS	I	Power supply ground.	
46	DCLK	I	Clock signal; latch input data at DCLK falling edge.	
47	STV2	I/O	Gate driver start pulse 2. UDC = 0, output UDC = 1, Tri-state	
48	DIO2	I/O	Source driver start pulse 2 LRC = 0, output LRC = 1, Tri-state	
49	RI0	I	Red color data input, bit0.	
50	RI1	I	Red color data input, bit1.	
51	RI2	I	Red color data input, bit2.	
52	RI3	I	Red color data input, bit3.	
53	RI4	I	Red color data input, bit4.	
54	RI5	I	Red color data input, bit5 (MSB).	
55	UDC	I	Up/Down scan control UDC = 1 => STV1 output, STV2 Tri-state UDC = 0 => STV1 Tri-state, STV2 output	pull-down
56	LRC	I	Left/right scan control LRC = 1 => DIO1 output, DIO2 Tri-state LRC = 0 => DIO1 Tri-state, DIO2 output	pull-down
57	GI0	I	Green color data input, bit0.	
58	GI1	I	Green color data input, bit1.	
59	GI2	I	Green color data input, bit2.	
60	GI3	I	Green color data input, bit3.	
61	GI4	I	Green color data input, bit4.	
62	GI5	I	Green color data input, bit5 (MSB).	
63	REVEN	I	Data reverse enable or disable L : disable H : enable	pull-up
64	RES2	I	Panel resolution select bit 2	pull-up/down

6. Panel Select Table

CY2890-D04 can support 8 different kind panel resolutions.

◆ Panel Select Table for CY2890-D04

RES[2:0]				RESOLUTION	
Value	Pin64	Pin13	Pin14		
0	0	0	0	800x480	
1	0	0	1	1024x600	
2	0	1	0	640x480	(*)
3	0	1	1	800x600	(*)
4	1	0	0	1024x768	
5	1	0	1	720x480	
6	1	1	0	320x240	
7	1	1	1	480x272	

7. DC Characteristics

◆ Absolute maximum ratings

PARAMETER	SYMBOL	RATING	UNIT
Power supply	V_{DD}	2.5 to 3.8	V
Input voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Output voltage	V_{OUT}	-0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	-40 to 125	℃

◆ Recommended operating conditions

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power supply	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IN}	0	-	V_{DD}	V
Operating temperature	T_{OPR}	-40	-	95	℃

◆ DC Electrical characteristics

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
Input low current	I_{IL}	No pull-up or pull-down	-1	-	1	μA	
Input high current	I_{IH}	No pull-up or pull-down	-1	-	1	μA	
Tri-state leakage current	I_{OZ}		-10	-	10	μA	
Logic input low voltage	V_{IL}	CMOS	-	-	$0.2V_{DD}$	V	Note 1
Schmitt input low voltage	V_{SIL}	CMOS	-	-	$0.3V_{DD}$	V	Note 2
Logic input high voltage	V_{IH}	CMOS	$0.8V_{DD}$	-	-	V	Note 1
Schmitt input high voltage	V_{SIH}	CMOS	$0.7V_{DD}$	-	-	V	Note 2
Output low voltage	V_{OL}	I_{OL} = 4mA	-	-	$0.3V_{DD}$	V	Note 3
Output high voltage	V_{OH}	I_{OH} = -4mA	$0.7V_{DD}$	-	-	V	Note 3
Output low voltage	V_{OL}	I_{OL} = 8mA	-	-	$0.3V_{DD}$	V	Note 4
Output high voltage	V_{OH}	I_{OH} = -8mA	$0.7V_{DD}$	-	-	V	Note 4
Input pull up / down resistance	R_I	V_{IL} = 0V or V_{IH} = V_{DD}	-	90	-	KΩ	Note 5

Note 1: MODE, UDC, LRC, RI0~RI5, GI0~GI5, BI0~BI5.
Note 2: DCLK, HSYNC, VSYNC, DE, RESETB
Note 3: CKV, POL, REV, LD, DIO1, DIO2, STV1, STV2, OEV, AP, RO0~RO5, GO0~GO5, BO0~BO5.
Note 4: HCLK
Note 5: RESETB, HSYNC, VSYNC, DE, MODE, UDC, LRC.

8. AC Characteristics

◆ SYNC mode Input signal characteristic, 800 x 480

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK PERIOD	TCLK	25	34	-	NS	
CLOCK FREQUENCY	FCLK	-	29.5	40	MHZ	
CLOCK LOW LEVEL WIDTH	TWCL	8	-	-	NS	
CLOCK HIGH LEVEL WIDTH	TWCH	8	-	-	NS	
CLOCK RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
HSYNC PERIOD	THP	810	928	1600	TCLK	
HSYNC PULSE WIDTH	THW	-	48	-	TCLK	
HSYNC BACK PORCH	THBP	-	40	-	TCLK	
HSYNC WIDTH + BACK PORCH	THW+ THBP	88			TCLK	
HORIZONTAL VALID DATA WIDTH	THV	800			TCLK	
HSYNC FRONT PORCH	THFP	THP – THW - THBP - THV			TCLK	
HORIZONTAL BLANK	THBK	THP – THV			TCLK	
VSYNC PERIOD	TVP	485	525	960	THP	
VSYNC PULSE WIDTH	TVW	-	3	-	THP	
VSYNC BACK PORCH	TVBP	29			THP	
VERTICAL DATA VALID WIDTH	TW	480			THP	
VSYNC FRONT PORCH	TVFP	TVP – TVW - TVBP - TW			THP	
VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA SETUP TIME	TDS	5	-	-	NS	
DATA HOLD TIME	TDH	5	-	-	NS	

◆ DE mode Input signal characteristics, 800 x 480

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK	PERIOD	TCLK	25	34	-	NS	
	FREQUENCY	FCLK	-	29.5	40	MHZ	
	LOW LEVEL WIDTH	TWCL	6	-	-	NS	
	HIGH LEVEL WIDTH	TWCH	6	-	-	NS	
	RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
	DUTY	-	0.45	0.50	0.55	-	
DE	SETUP TIME	TDES	5	-	-	NS	
	HOLD TIME	TDEH	5	-	-	NS	
	RISE, FALL TIME	TDER, TDEF	-	-	5	NS	
	HORIZONTAL PERIOD	THP	810	928	1600	TCLK	
	HORIZONTAL VALID	THV	800			TCLK	
	HORIZONTAL BLANK	THBK	THP - THV			TCLK	
	VERTICAL PERIOD	TVP	485	525	960	THP	
	VERTICAL VALID	TW	480			THP	
	VERTICAL BLANK	TVBK	TVP - TW			THP	
DATA	SETUP TIME	TDS	5	-	-	NS	
	HOLD TIME	TDH	5	-	-	NS	
	RISE, FALL TIME	TDR, TDF	-	-	3	NS	

◆ Output Signal Characteristics, 800 x 480

PARAMETER		SYMBOL	VALUE	UNIT
HCLK FREQUENCY	NORMAL	FHCLK	1	FCLK
HCLK FREQUENCY	DUAL	1/2FHCLK	0.5	FCLK
HCLK PERIOD	NORMAL	THCLK	1	TCLK
HCLK PERIOD	DUAL	2THCLK	2	TCLK
DATA, REV DIO VALID TO HCLK RISING		TSU	0.5	THCLK
HCLK RISING TO DATA, REV, DIO VALID		THD	0.5	THCLK
POL PULSE WIDTH		TPOL	1	THP
POL VALID TO LD RISING		TPSU	0.5 THP + 12	THCLK
LD RISING TO POL VALID		TPHD	THP - TPSU	THCLK
STV PULSE WIDTH		TSTV	1	THP
STV VALID TO CKV RISING		TVSU	0.5	THP
CKV RISING TO STV VALID		TVHD	0.5	THP
DIO PULSE WIDTH		TDIOW	1	THCLK
LD PULSE WIDTH		TLDW	4	THCLK
OEV PULSE WIDTH		TOEV	66	THCLK
CKV PULSE WIDTH		TCKV	0.5	THP
TIME FROM LD TO CKV		TGS	1	THCLK
TIME FROM LD TO DIO		TLDO	THBK – 6	THCLK
TIME FROM THE LAST DATA TO LD		TED	5.5	THCLK
AP PULSE WIDTH		TAPW	THP – 62	THCLK
TIME FROM LD TO AP		TLDAP	44	THCLK

◆ SYNC mode Input signal characteristic, 640 x 480

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK PERIOD	TCLK	25	40	-	NS	
CLOCK FREQUENCY	FCLK	-	25	40	MHZ	
CLOCK LOW LEVEL WIDTH	TWCL	8	20	-	NS	
CLOCK HIGH LEVEL WIDTH	TWCH	8	20	-	NS	
CLOCK RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
HSYNC PERIOD	THP	650	800	1280	TCLK	
HSYNC PULSE WIDTH	THW	-	96	-	TCLK	
HSYNC BACK PORCH	THBP	-	48	-	TCLK	
HSYNC WIDTH + BACK PORCH	THW+ THBP	144			TCLK	
HORIZONTAL VALID DATA WIDTH	THV	640			TCLK	
HSYNC FRONT PORCH	THFP	THP – THW - THBP - THV			TCLK	
HORIZONTAL BLANK	THBK	THP – THV			TCLK	
VSYNC PERIOD	TVP	485	525	960	THP	
VSYNC PULSE WIDTH	TVW	-	3	-	THP	
VSYNC BACK PORCH	TVBP	33			THP	
VERTICAL DATA VALID WIDTH	TW	480			THP	
VSYNC FRONT PORCH	TVFP	TVP – TVW - TVBP - TW			THP	
VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA SETUP TIME	TDS	5	-	-	NS	
DATA HOLD TIME	TDH	5	-	-	NS	

◆ DE mode Input signal characteristics, 640 x 480

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK	PERIOD	TCLK	25	40	-	NS	
	FREQUENCY	FCLK	-	25	40	MHZ	
	LOW LEVEL WIDTH	TWCL	6	-	-	NS	
	HIGH LEVEL WIDTH	TWCH	6	-	-	NS	
	RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
	DUTY	-	0.45	0.50	0.55	-	
DE	SETUP TIME	TDES	5	-	-	NS	
	HOLD TIME	TDEH	5	-	-	NS	
	RISE, FALL TIME	TDER, TDEF	-	-	5	NS	
	HORIZONTAL PERIOD	THP	650	800	1280	TCLK	
	HORIZONTAL VALID	THV	640			TCLK	
	HORIZONTAL BLANK	THBK	THP - THV			TCLK	
	VERTICAL PERIOD	TVP	485	525	960	THP	
	VERTICAL VALID	TW	480			THP	
	VERTICAL BLANK	TVBK	TVP - TW			THP	
DATA	SETUP TIME	TDS	5	-	-	NS	
	HOLD TIME	TDH	5	-	-	NS	
	RISE, FALL TIME	TDR, TDF	-	-	3	NS	

◆ Output Signal Characteristics, 640 x 480

PARAMETER		SYMBOL	VALUE	UNIT
HCLK FREQUENCY	NORMAL	FHCLK	1	FCLK
HCLK FREQUENCY	DUAL	1/2FHCLK	0.5	FCLK
HCLK PERIOD	NORMAL	THCLK	1	TCLK
HCLK PERIOD	DUAL	2THCLK	2	TCLK
DATA, REV DIO VALID TO HCLK RISING		TSU	0.5	THCLK
HCLK RISING TO DATA, REV, DIO VALID		THD	0.5	THCLK
POL PULSE WIDTH		TPOL	1	THP
POL VALID TO LD RISING		TPSU	0.5 THP + 12	THCLK
LD RISING TO POL VALID		TPHD	THP - TPSU	THCLK
STV PULSE WIDTH		TSTV	1	THP
STV VALID TO CKV RISING		TVSU	0.5	THP
CKV RISING TO STV VALID		TVHD	0.5	THP
DIO PULSE WIDTH		TDIOW	1	THCLK
LD PULSE WIDTH		TLDW	4	THCLK
OEV PULSE WIDTH		TOEV	66	THCLK
CKV PULSE WIDTH		TCKV	0.5	THP
TIME FROM LD TO CKV		TGS	1	THCLK
TIME FROM LD TO DIO		TLDO	THBK – 6	THCLK
TIME FROM THE LAST DATA TO LD		TED	5.5	THCLK
AP PULSE WIDTH		TAPW	THP – 62	THCLK
TIME FROM LD TO AP		TLDAP	44	THCLK

◆ SYNC mode Input signal characteristic, 800 x 600

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK PERIOD	TCLK	20	25	-	NS	
CLOCK FREQUENCY	FCLK	-	40	50	MHZ	
CLOCK LOW LEVEL WIDTH	TWCL	8	12.5	-	NS	
CLOCK HIGH LEVEL WIDTH	TWCH	8	12.5	-	NS	
CLOCK RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
HSYNC PERIOD	THP	810	1000	1600	TCLK	
HSYNC PULSE WIDTH	THW	-	48	-	TCLK	
HSYNC BACK PORCH	THBP	-	40	-	TCLK	
HSYNC WIDTH + BACK PORCH	THW+ THBP	88			TCLK	
HORIZONTAL VALID DATA WIDTH	THV	800			TCLK	
HSYNC FRONT PORCH	THFP	THP – THW - THBP - THV			TCLK	
HORIZONTAL BLANK	THBK	THP – THV			TCLK	
VSYNC PERIOD	TVP	605	660	1200	THP	
VSYNC PULSE WIDTH	TVW	-	3	-	THP	
VSYNC BACK PORCH	TVBP	36			THP	
VERTICAL DATA VALID WIDTH	TW	600			THP	
VSYNC FRONT PORCH	TVFP	TVP – TVW - TVBP - TW			THP	
VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA SETUP TIME	TDS	5	-	-	NS	
DATA HOLD TIME	TDH	5	-	-	NS	

◆ DE mode Input signal characteristics, 800 x 600

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK	PERIOD	TCLK	20	25	-	NS	
	FREQUENCY	FCLK	-	40	50	MHZ	
	LOW LEVEL WIDTH	TWCL	8	-	-	NS	
	HIGH LEVEL WIDTH	TWCH	8	-	-	NS	
	RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
	DUTY	-	0.45	0.50	0.55	-	
DE	SETUP TIME	TDES	5	-	-	NS	
	HOLD TIME	TDEH	5	-	-	NS	
	RISE, FALL TIME	TDER, TDEF	-	-	5	NS	
	HORIZONTAL PERIOD	THP	810	1000	1600	TCLK	
	HORIZONTAL VALID	THV	800			TCLK	
	HORIZONTAL BLANK	THBK	THP – THV			TCLK	
	VERTICAL PERIOD	TVP	605	660	1200	THP	
	VERTICAL VALID	TW	600			THP	
	VERTICAL BLANK	TVBK	TVP - TW			THP	
DATA	SETUP TIME	TDS	5	-	-	NS	
	HOLD TIME	TDH	5	-	-	NS	
	RISE, FALL TIME	TDR, TDF	-	-	3	NS	

◆ Output Signal Characteristics, 800 x 600

PARAMETER		SYMBOL	VALUE	UNIT
HCLK FREQUENCY	NORMAL	FHCLK	1	FCLK
HCLK FREQUENCY	DUAL	1/2FHCLK	0.5	FCLK
HCLK PERIOD	NORMAL	THCLK	1	TCLK
HCLK PERIOD	DUAL	2THCLK	2	TCLK
DATA, REV DIO VALID TO HCLK RISING		TSU	0.5	THCLK
HCLK RISING TO DATA, REV, DIO VALID		THD	0.5	THCLK
POL PULSE WIDTH		TPOL	1	THP
POL VALID TO LD RISING		TPSU	0.5 THP + 12	THCLK
LD RISING TO POL VALID		TPHD	THP - TPSU	THCLK
STV PULSE WIDTH		TSTV	1	THP
STV VALID TO CKV RISING		TVSU	0.5	THP
CKV RISING TO STV VALID		TVHD	0.5	THP
DIO PULSE WIDTH		TDIOW	1	THCLK
LD PULSE WIDTH		TLDW	4	THCLK
OEV PULSE WIDTH		TOEV	66	THCLK
CKV PULSE WIDTH		TCKV	0.5	THP
TIME FROM LD TO CKV		TGS	1	THCLK
TIME FROM LD TO DIO		TLDO	THBK – 6	THCLK
TIME FROM THE LAST DATA TO LD		TED	5.5	THCLK
AP PULSE WIDTH		TAPW	THP – 62	THCLK
TIME FROM LD TO AP		TLDAP	44	THCLK

◆ SYNC mode Input signal characteristic, 1024 x 600

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK PERIOD	TCLK	15	20	-	NS	
CLOCK FREQUENCY	FCLK	-	50	66	MHZ	
CLOCK LOW LEVEL WIDTH	TWCL	6	10	-	NS	
CLOCK HIGH LEVEL WIDTH	TWCH	6	10	-	NS	
CLOCK RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
HSYNC PERIOD	THP	1034	1280	2047	TCLK	
HSYNC PULSE WIDTH	THW	-	48	-	TCLK	
HSYNC BACK PORCH	THBP	-	40	-	TCLK	
HSYNC WIDTH + BACK PORCH	THW+ THBP	88			TCLK	
HORIZONTAL VALID DATA WIDTH	THV	1024			TCLK	
HSYNC FRONT PORCH	THFP	THP – THW - THBP - THV			TCLK	
HORIZONTAL BLANK	THBK	THP – THV			TCLK	
VSYNC PERIOD	TVP	605	660	1200	THP	
VSYNC PULSE WIDTH	TVW	-	3	-	THP	
VSYNC BACK PORCH	TVBP	36			THP	
VERTICAL DATA VALID WIDTH	TW	600			THP	
VSYNC FRONT PORCH	TVFP	TVP – TVW - TVBP - TW			THP	
VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA SETUP TIME	TDS	5	-	-	NS	
DATA HOLD TIME	TDH	5	-	-	NS	

◆ DE mode Input signal characteristics, 1024 x 600

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK	PERIOD	TCLK	15	20	-	NS	
	FREQUENCY	FCLK	-	50	66	MHZ	
	LOW LEVEL WIDTH	TWCL	6	10	-	NS	
	HIGH LEVEL WIDTH	TWCH	6	10	-	NS	
	RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
	DUTY	-	0.45	0.50	0.55	-	
DE	SETUP TIME	TDES	5	-	-	NS	
	HOLD TIME	TDEH	5	-	-	NS	
	RISE, FALL TIME	TDER, TDEF	-	-	5	NS	
	HORIZONTAL PERIOD	THP	1034	1280	2047	TCLK	
	HORIZONTAL VALID	THV	1024			TCLK	
	HORIZONTAL BLANK	THBK	THP – THV			TCLK	
	VERTICAL PERIOD	TVP	605	660	1200	THP	
	VERTICAL VALID	TW	600			THP	
	VERTICAL BLANK	TVBK	TVP - TW			THP	
DATA	SETUP TIME	TDS	5	-	-	NS	
	HOLD TIME	TDH	5	-	-	NS	
	RISE, FALL TIME	TDR, TDF	-	-	3	NS	

◆ Output Signal Characteristics, 1024 x 600

PARAMETER		SYMBOL	VALUE	UNIT
HCLK FREQUENCY	NORMAL	FHCLK	1	FCLK
HCLK FREQUENCY	DUAL	1/2FHCLK	0.5	FCLK
HCLK PERIOD	NORMAL	THCLK	1	TCLK
HCLK PERIOD	DUAL	2THCLK	2	TCLK
DATA, REV DIO VALID TO HCLK RISING		TSU	0.5	THCLK
HCLK RISING TO DATA, REV, DIO VALID		THD	0.5	THCLK
POL PULSE WIDTH		TPOL	1	THP
POL VALID TO LD RISING		TPSU	0.5 THP + 12	THCLK
LD RISING TO POL VALID		TPHD	THP - TPSU	THCLK
STV PULSE WIDTH		TSTV	1	THP
STV VALID TO CKV RISING		TVSU	0.5	THP
CKV RISING TO STV VALID		TVHD	0.5	THP
DIO PULSE WIDTH		TDIOW	1	THCLK
LD PULSE WIDTH		TLDW	4	THCLK
OEV PULSE WIDTH		TOEV	66	THCLK
CKV PULSE WIDTH		TCKV	0.5	THP
TIME FROM LD TO CKV		TGS	1	THCLK
TIME FROM LD TO DIO		TLDO	THBK – 6	THCLK
TIME FROM THE LAST DATA TO LD		TED	5.5	THCLK
AP PULSE WIDTH		TAPW	THP – 62	THCLK
TIME FROM LD TO AP		TLDAP	44	THCLK

◆ SYNC mode Input signal characteristic, 1024 x 768

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK PERIOD	TCLK	12	15	-	NS	
CLOCK FREQUENCY	FCLK	-	65	83	MHZ	
CLOCK LOW LEVEL WIDTH	TWCL	5	7.5	-	NS	
CLOCK HIGH LEVEL WIDTH	TWCH	5	7.5	-	NS	
CLOCK RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
HSYNC PERIOD	THP	1034	1280	2047	TCLK	
HSYNC PULSE WIDTH	THW	-	48	-	TCLK	
HSYNC BACK PORCH	THBP	-	40	-	TCLK	
HSYNC WIDTH + BACK PORCH	THW+ THBP	88			TCLK	
HORIZONTAL VALID DATA WIDTH	THV	1024			TCLK	
HSYNC FRONT PORCH	THFP	THP – THW - THBP - THV			TCLK	
HORIZONTAL BLANK	THBK	THP – THV			TCLK	
VSYNC PERIOD	TVP	773	845	1536	THP	
VSYNC PULSE WIDTH	TVW	-	3	-	THP	
VSYNC BACK PORCH	TVBP	36			THP	
VERTICAL DATA VALID WIDTH	TW	768			THP	
VSYNC FRONT PORCH	TVFP	TVP – TVW - TVBP - TW			THP	
VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA SETUP TIME	TDS	5	-	-	NS	
DATA HOLD TIME	TDH	5	-	-	NS	

◆ DE mode Input signal characteristics, 1024 x 768

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK	PERIOD	TCLK	12	15	-	NS	
	FREQUENCY	FCLK	-	65	83	MHZ	
	LOW LEVEL WIDTH	TWCL	5	7.5	-	NS	
	HIGH LEVEL WIDTH	TWCH	5	7.5	-	NS	
	RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
	DUTY	-	0.45	0.50	0.55	-	
DE	SETUP TIME	TDES	5	-	-	NS	
	HOLD TIME	TDEH	5	-	-	NS	
	RISE, FALL TIME	TDER, TDEF	-	-	5	NS	
	HORIZONTAL PERIOD	THP	1034	1280	2047	TCLK	
	HORIZONTAL VALID	THV	1024			TCLK	
	HORIZONTAL BLANK	THBK	THP – THV			TCLK	
	VERTICAL PERIOD	TVP	773	845	1536	THP	
	VERTICAL VALID	TW	768			THP	
	VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA	SETUP TIME	TDS	5	-	-	NS	
	HOLD TIME	TDH	5	-	-	NS	
	RISE, FALL TIME	TDR, TDF	-	-	3	NS	

◆ Output Signal Characteristics, 1024 x 768

PARAMETER		SYMBOL	VALUE	UNIT
HCLK FREQUENCY	NORMAL	FHCLK	1	FCLK
HCLK FREQUENCY	DUAL	1/2FHCLK	0.5	FCLK
HCLK PERIOD	NORMAL	THCLK	1	TCLK
HCLK PERIOD	DUAL	2THCLK	2	TCLK
DATA, REV DIO VALID TO HCLK RISING		TSU	0.5	THCLK
HCLK RISING TO DATA, REV, DIO VALID		THD	0.5	THCLK
POL PULSE WIDTH		TPOL	1	THP
POL VALID TO LD RISING		TPSU	0.5 THP + 12	THCLK
LD RISING TO POL VALID		TPHD	THP - TPSU	THCLK
STV PULSE WIDTH		TSTV	1	THP
STV VALID TO CKV RISING		TVSU	0.5	THP
CKV RISING TO STV VALID		TVHD	0.5	THP
DIO PULSE WIDTH		TDIOW	1	THCLK
LD PULSE WIDTH		TLDW	4	THCLK
OEV PULSE WIDTH		TOEV	66	THCLK
CKV PULSE WIDTH		TCKV	0.5	THP
TIME FROM LD TO CKV		TGS	1	THCLK
TIME FROM LD TO DIO		TLDO	THBK – 6	THCLK
TIME FROM THE LAST DATA TO LD		TED	5.5	THCLK
AP PULSE WIDTH		TAPW	THP – 62	THCLK
TIME FROM LD TO AP		TLDAP	44	THCLK

◆ SYNC mode Input signal characteristic, 720 x 480

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK PERIOD	TCLK	28.6	34.5	-	NS	
CLOCK FREQUENCY	FCLK	-	29	35	MHZ	
CLOCK LOW LEVEL WIDTH	TWCL	8	17.25	-	NS	
CLOCK HIGH LEVEL WIDTH	TWCH	8	17.25	-	NS	
CLOCK RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
HSYNC PERIOD	THP	730	900	1440	TCLK	
HSYNC PULSE WIDTH	THW	-	32	-	TCLK	
HSYNC BACK PORCH	THBP	-	48	-	TCLK	
HSYNC WIDTH + BACK PORCH	THW+ THBP	80			TCLK	
HORIZONTAL VALID DATA WIDTH	THV	720			TCLK	
HSYNC FRONT PORCH	THFP	THP – THW - THBP - THV			TCLK	
HORIZONTAL BLANK	THBK	THP – THV			TCLK	
VSYNC PERIOD	TVP	485	525	960	THP	
VSYNC PULSE WIDTH	TVW	-	3	-	THP	
VSYNC BACK PORCH	TVBP	29			THP	
VERTICAL DATA VALID WIDTH	TW	480			THP	
VSYNC FRONT PORCH	TVFP	TVP – TVW - TVBP - TW			THP	
VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA SETUP TIME	TDS	5	-	-	NS	
DATA HOLD TIME	TDH	5	-	-	NS	

◆ DE mode Input signal characteristics, 720 x 480

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK	PERIOD	TCLK	28.6	34.5	-	NS	
	FREQUENCY	FCLK	-	29	35	MHZ	
	LOW LEVEL WIDTH	TWCL	8	17.25	-	NS	
	HIGH LEVEL WIDTH	TWCH	8	17.25	-	NS	
	RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
	DUTY	-	0.45	0.50	0.55	-	
DE	SETUP TIME	TDES	5	-	-	NS	
	HOLD TIME	TDEH	5	-	-	NS	
	RISE, FALL TIME	TDER, TDEF	-	-	5	NS	
	HORIZONTAL PERIOD	THP	730	900	1440	TCLK	
	HORIZONTAL VALID	THV	720			TCLK	
	HORIZONTAL BLANK	THBK	THP – THV			TCLK	
	VERTICAL PERIOD	TVP	485	525	960	THP	
	VERTICAL VALID	TW	480			THP	
	VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA	SETUP TIME	TDS	5	-	-	NS	
	HOLD TIME	TDH	5	-	-	NS	
	RISE, FALL TIME	TDR, TDF	-	-	3	NS	

◆ Output Signal Characteristics, 720 x 480

PARAMETER		SYMBOL	VALUE	UNIT
HCLK FREQUENCY	NORMAL	FHCLK	1	FCLK
HCLK FREQUENCY	DUAL	1/2FHCLK	0.5	FCLK
HCLK PERIOD	NORMAL	THCLK	1	TCLK
HCLK PERIOD	DUAL	2THCLK	2	TCLK
DATA, REV DIO VALID TO HCLK RISING		TSU	0.5	THCLK
HCLK RISING TO DATA, REV, DIO VALID		THD	0.5	THCLK
POL PULSE WIDTH		TPOL	1	THP
POL VALID TO LD RISING		TPSU	0.5 THP + 12	THCLK
LD RISING TO POL VALID		TPHD	THP - TPSU	THCLK
STV PULSE WIDTH		TSTV	1	THP
STV VALID TO CKV RISING		TVSU	0.5	THP
CKV RISING TO STV VALID		TVHD	0.5	THP
DIO PULSE WIDTH		TDIOW	1	THCLK
LD PULSE WIDTH		TLDW	4	THCLK
OEV PULSE WIDTH		TOEV	66	THCLK
CKV PULSE WIDTH		TCKV	0.5	THP
TIME FROM LD TO CKV		TGS	1	THCLK
TIME FROM LD TO DIO		TLDO	THBK – 6	THCLK
TIME FROM THE LAST DATA TO LD		TED	5.5	THCLK
AP PULSE WIDTH		TAPW	THP – 62	THCLK
TIME FROM LD TO AP		TLDAP	44	THCLK

◆ SYNC mode Input signal characteristic, 854 x 480

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK PERIOD	TCLK	25	30	-	NS	
CLOCK FREQUENCY	FCLK	-	33	40	MHZ	
CLOCK LOW LEVEL WIDTH	TWCL	8	15	-	NS	
CLOCK HIGH LEVEL WIDTH	TWCH	8	15	-	NS	
CLOCK RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
HSYNC PERIOD	THP	864	1068	1708	TCLK	
HSYNC PULSE WIDTH	THW	-	48	-	TCLK	
HSYNC BACK PORCH	THBP	-	44	-	TCLK	
HSYNC WIDTH + BACK PORCH	THW+ THBP	92			TCLK	
HORIZONTAL VALID DATA WIDTH	THV	854			TCLK	
HSYNC FRONT PORCH	THFP	THP – THW - THBP - THV			TCLK	
HORIZONTAL BLANK	THBK	THP – THV			TCLK	
VSYNC PERIOD	TVP	485	525	960	THP	
VSYNC PULSE WIDTH	TVW	-	3	-	THP	
VSYNC BACK PORCH	TVBP	29			THP	
VERTICAL DATA VALID WIDTH	TW	480			THP	
VSYNC FRONT PORCH	TVFP	TVP – TVW - TVBP - TW			THP	
VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA SETUP TIME	TDS	5	-	-	NS	
DATA HOLD TIME	TDH	5	-	-	NS	

◆ DE mode Input signal characteristics, 854 x 480

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK	PERIOD	TCLK	25	30	-	NS	
	FREQUENCY	FCLK	-	33	40	MHZ	
	LOW LEVEL WIDTH	TWCL	8	15	-	NS	
	HIGH LEVEL WIDTH	TWCH	8	15	-	NS	
	RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
	DUTY	-	0.45	0.50	0.55	-	
DE	SETUP TIME	TDES	5	-	-	NS	
	HOLD TIME	TDEH	5	-	-	NS	
	RISE, FALL TIME	TDER, TDEF	-	-	5	NS	
	HORIZONTAL PERIOD	THP	864	1068	1708	TCLK	
	HORIZONTAL VALID	THV	854			TCLK	
	HORIZONTAL BLANK	THBK	THP – THV			TCLK	
	VERTICAL PERIOD	TVP	485	525	960	THP	
	VERTICAL VALID	TW	480			THP	
	VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA	SETUP TIME	TDS	5	-	-	NS	
	HOLD TIME	TDH	5	-	-	NS	
	RISE, FALL TIME	TDR, TDF	-	-	3	NS	

◆ Output Signal Characteristics, 854 x 480

PARAMETER		SYMBOL	VALUE	UNIT
HCLK FREQUENCY	NORMAL	FHCLK	1	FCLK
HCLK FREQUENCY	DUAL	1/2FHCLK	0.5	FCLK
HCLK PERIOD	NORMAL	THCLK	1	TCLK
HCLK PERIOD	DUAL	2THCLK	2	TCLK
DATA, REV DIO VALID TO HCLK RISING		TSU	0.5	THCLK
HCLK RISING TO DATA, REV, DIO VALID		THD	0.5	THCLK
POL PULSE WIDTH		TPOL	1	THP
POL VALID TO LD RISING		TPSU	0.5 THP + 12	THCLK
LD RISING TO POL VALID		TPHD	THP - TPSU	THCLK
STV PULSE WIDTH		TSTV	1	THP
STV VALID TO CKV RISING		TVSU	0.5	THP
CKV RISING TO STV VALID		TVHD	0.5	THP
DIO PULSE WIDTH		TDIOW	1	THCLK
LD PULSE WIDTH		TLDW	4	THCLK
OEV PULSE WIDTH		TOEV	66	THCLK
CKV PULSE WIDTH		TCKV	0.5	THP
TIME FROM LD TO CKV		TGS	1	THCLK
TIME FROM LD TO DIO		TLDO	THBK – 6	THCLK
TIME FROM THE LAST DATA TO LD		TED	5.5	THCLK
AP PULSE WIDTH		TAPW	THP – 62	THCLK
TIME FROM LD TO AP		TLDAP	44	THCLK

◆ SYNC mode Input signal characteristic, 480 x 272

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK PERIOD	TCLK	25	93	-	NS	
CLOCK FREQUENCY	FCLK	-	10.7	40	MHZ	
CLOCK LOW LEVEL WIDTH	TWCL	8	46.5	-	NS	
CLOCK HIGH LEVEL WIDTH	TWCH	8	46.5	-	NS	
CLOCK RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
HSYNC PERIOD	THP	490	600	960	TCLK	
HSYNC PULSE WIDTH	THW	-	36	-	TCLK	
HSYNC BACK PORCH	THBP	-	30	-	TCLK	
HSYNC WIDTH + BACK PORCH	THW+ THBP	66			TCLK	
HORIZONTAL VALID DATA WIDTH	THV	480			TCLK	
HSYNC FRONT PORCH	THFP	THP – THW - THBP - THV			TCLK	
HORIZONTAL BLANK	THBK	THP – THV			TCLK	
VSYNC PERIOD	TVP	277	299	544	THP	
VSYNC PULSE WIDTH	TVW	-	3	-	THP	
VSYNC BACK PORCH	TVBP	19			THP	
VERTICAL DATA VALID WIDTH	TW	272			THP	
VSYNC FRONT PORCH	TVFP	TVP – TVW - TVBP - TW			THP	
VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA SETUP TIME	TDS	5	-	-	NS	
DATA HOLD TIME	TDH	5	-	-	NS	

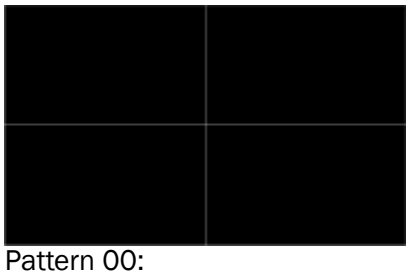
◆ DE mode Input signal characteristics, 480 x 272

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK	PERIOD	TCLK	25	93	-	NS	
	FREQUENCY	FCLK	-	10.7	40	MHZ	
	LOW LEVEL WIDTH	TWCL	8	46.5	-	NS	
	HIGH LEVEL WIDTH	TWCH	8	46.5	-	NS	
	RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
	DUTY	-	0.45	0.50	0.55	-	
DE	SETUP TIME	TDES	5	-	-	NS	
	HOLD TIME	TDEH	5	-	-	NS	
	RISE, FALL TIME	TDER, TDEF	-	-	5	NS	
	HORIZONTAL PERIOD	THP	490	600	960	TCLK	
	HORIZONTAL VALID	THV	480			TCLK	
	HORIZONTAL BLANK	THBK	THP – THV			TCLK	
	VERTICAL PERIOD	TVP	277	299	544	THP	
	VERTICAL VALID	TW	272			THP	
	VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA	SETUP TIME	TDS	5	-	-	NS	
	HOLD TIME	TDH	5	-	-	NS	
	RISE, FALL TIME	TDR, TDF	-	-	3	NS	

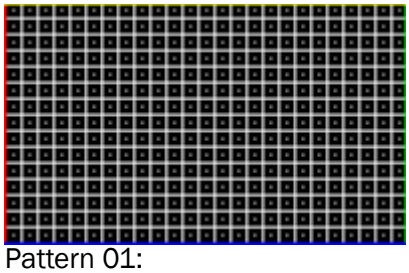
◆ Output Signal Characteristics, 480 x 272

PARAMETER		SYMBOL	VALUE	UNIT
HCLK FREQUENCY	NORMAL	FHCLK	1	FCLK
HCLK FREQUENCY	DUAL	1/2FHCLK	0.5	FCLK
HCLK PERIOD	NORMAL	THCLK	1	TCLK
HCLK PERIOD	DUAL	2THCLK	2	TCLK
DATA, REV DIO VALID TO HCLK RISING		TSU	0.5	THCLK
HCLK RISING TO DATA, REV, DIO VALID		THD	0.5	THCLK
POL PULSE WIDTH		TPOL	1	THP
POL VALID TO LD RISING		TPSU	0.5 THP + 12	THCLK
LD RISING TO POL VALID		TPHD	THP - TPSU	THCLK
STV PULSE WIDTH		TSTV	1	THP
STV VALID TO CKV RISING		TVSU	0.5	THP
CKV RISING TO STV VALID		TVHD	0.5	THP
DIO PULSE WIDTH		TDIOW	1	THCLK
LD PULSE WIDTH		TLDW	4	THCLK
OEV PULSE WIDTH		TOEV	66	THCLK
CKV PULSE WIDTH		TCKV	0.5	THP
TIME FROM LD TO CKV		TGS	1	THCLK
TIME FROM LD TO DIO		TLDO	THBK – 6	THCLK
TIME FROM THE LAST DATA TO LD		TED	5.5	THCLK
AP PULSE WIDTH		TAPW	THP – 40	THCLK
TIME FROM LD TO AP		TLDAP	22	THCLK

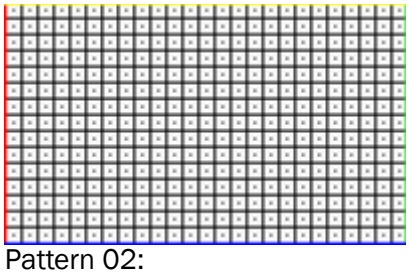
9. Built-in Patterns



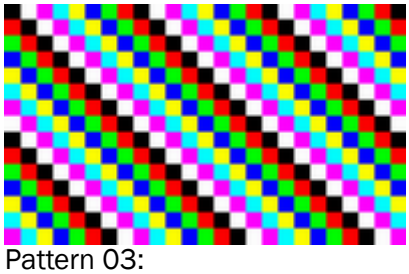
Pattern 00:
Black with white cross line,
White line boundary.



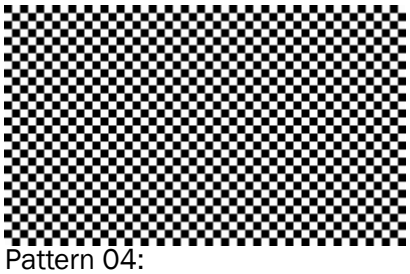
Pattern 01:
White cross hatch and dot
4 border lines



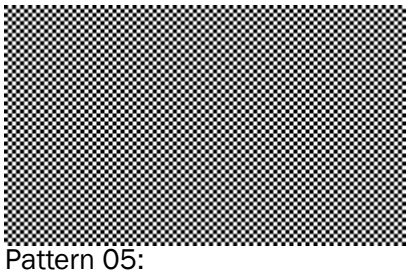
Pattern 02:
Black cross hatch and dot
4 border lines



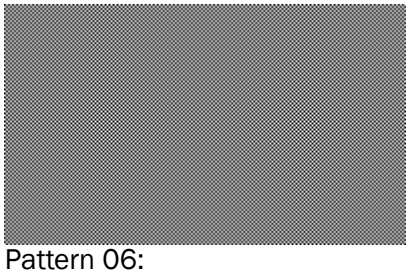
Pattern 03:
Diagonal color



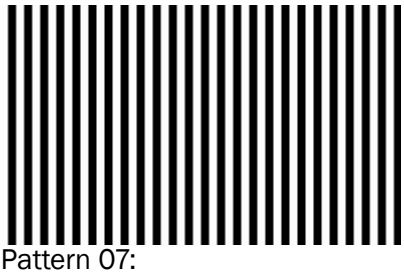
Pattern 04:
Black and white checkerboard
four pixels



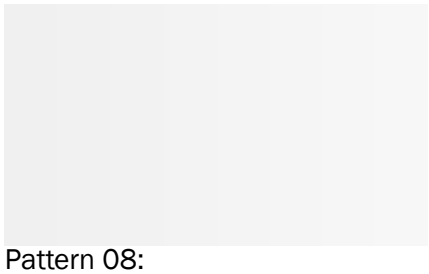
Pattern 05:
Black and white checkerboard
two pixels



Pattern 06:
Black and white checkerboard
one pixel and boundary

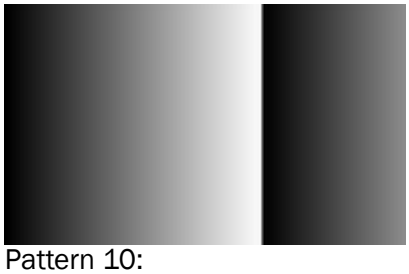


Pattern 07:
Vertical black and white bar.,
Coarse.



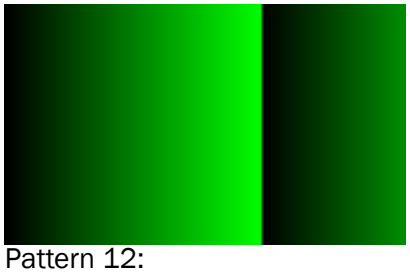
Pattern 08:
61,62 gray color, dither off
240 ~ 247 gray color, dither on

Pattern 09:
Vertical gray 8 levels
64 pixels

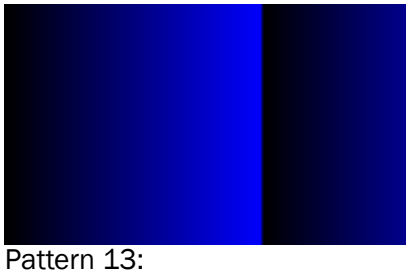


Pattern 10:
Dither pattern for gray

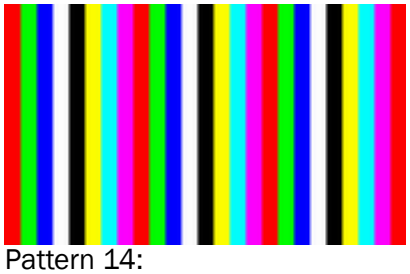
Pattern 11:
Dither pattern for red



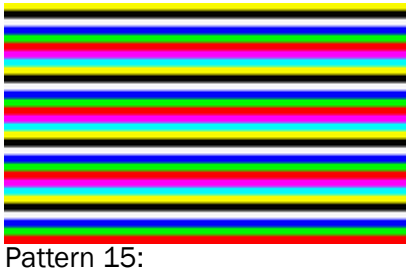
Pattern 12:
Dither pattern for green



Pattern 13:
Dither pattern for blue



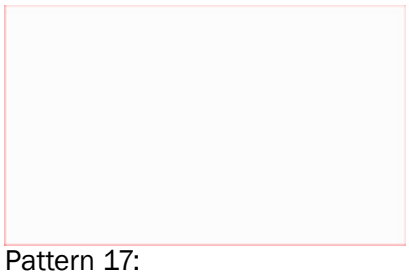
Pattern 14:
Vertical colors bar.



Pattern 15:
Horizontal colors bar.

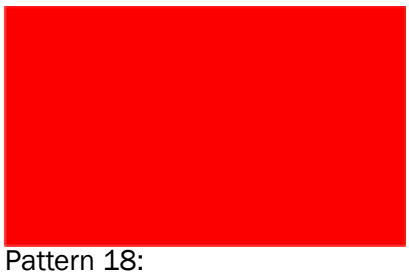
Pattern 16:
Black color with white line boundary

Pattern 20:
Blue with white line boundary



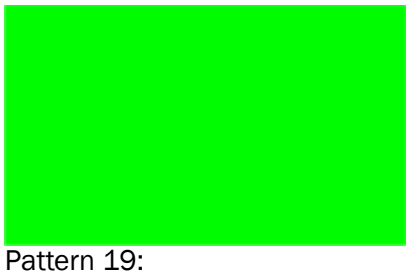
Pattern 17:
White color with red line boundary

Pattern 21:
Yellow with white line boundary

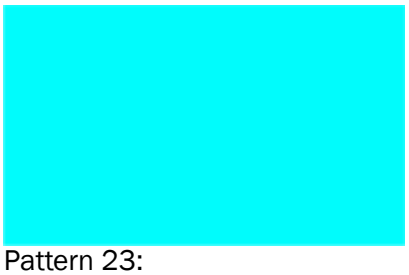


Pattern 18:
Red with white line boundary

Pattern 22:
Magenta with white line boundary



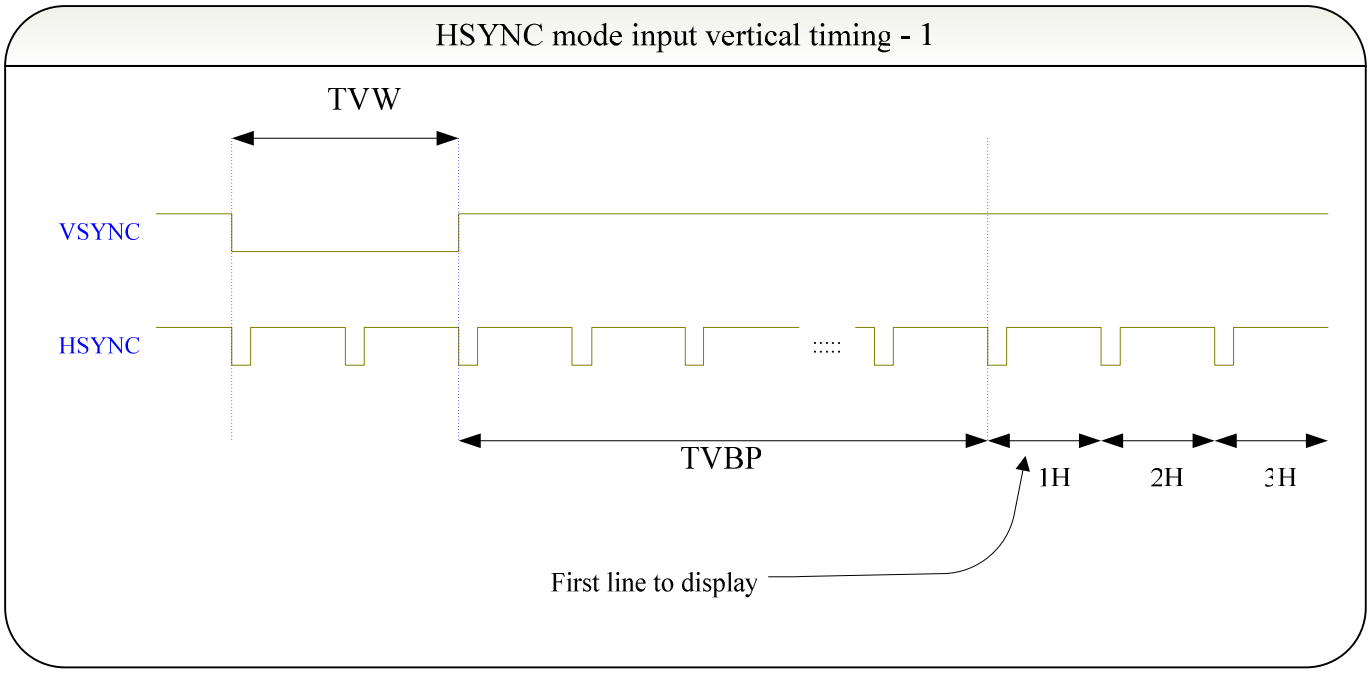
Pattern 19:
Green with white line boundary



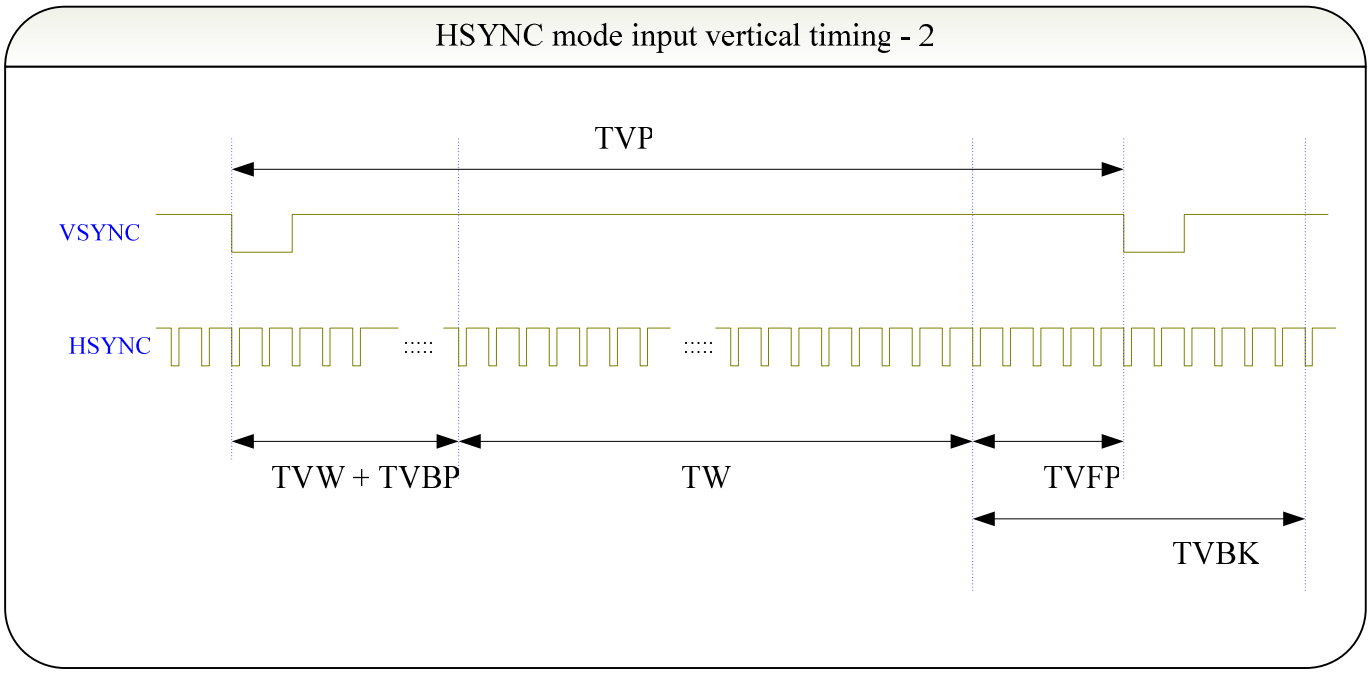
Pattern 23:
Cyan with white line boundary

10. Waveforms

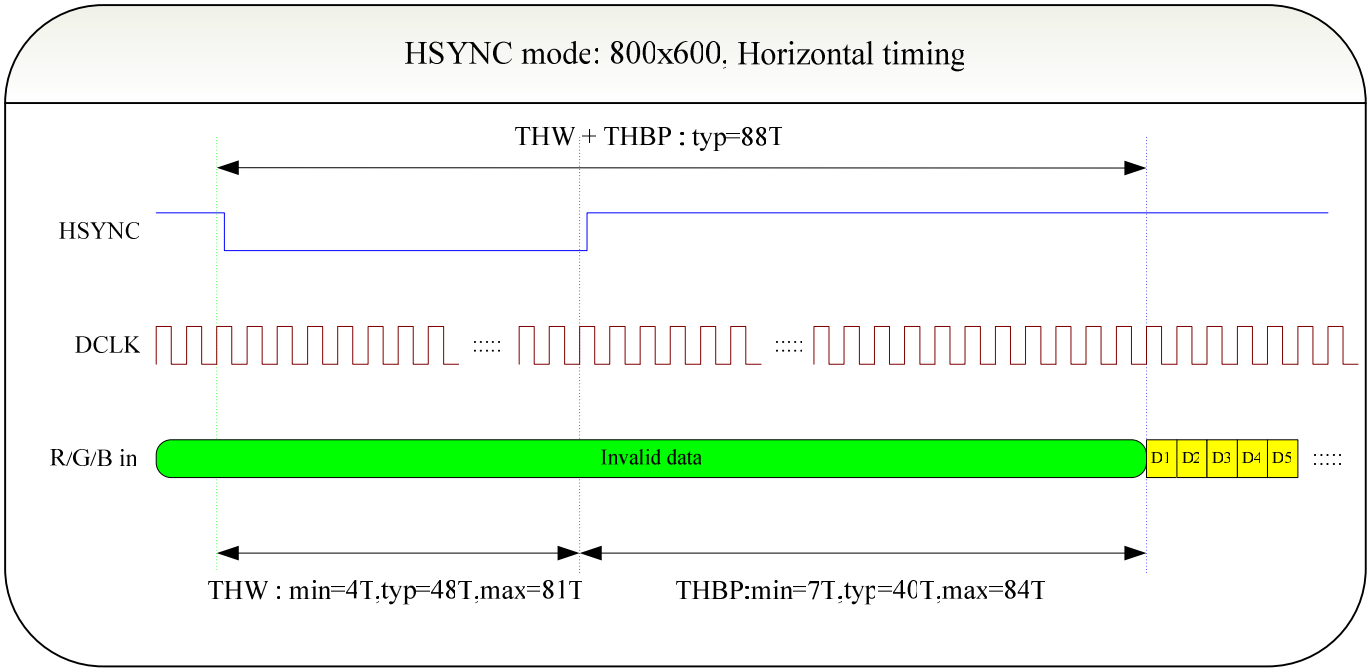
- Waveform 1: HSYNC mode input vertical timing - 1



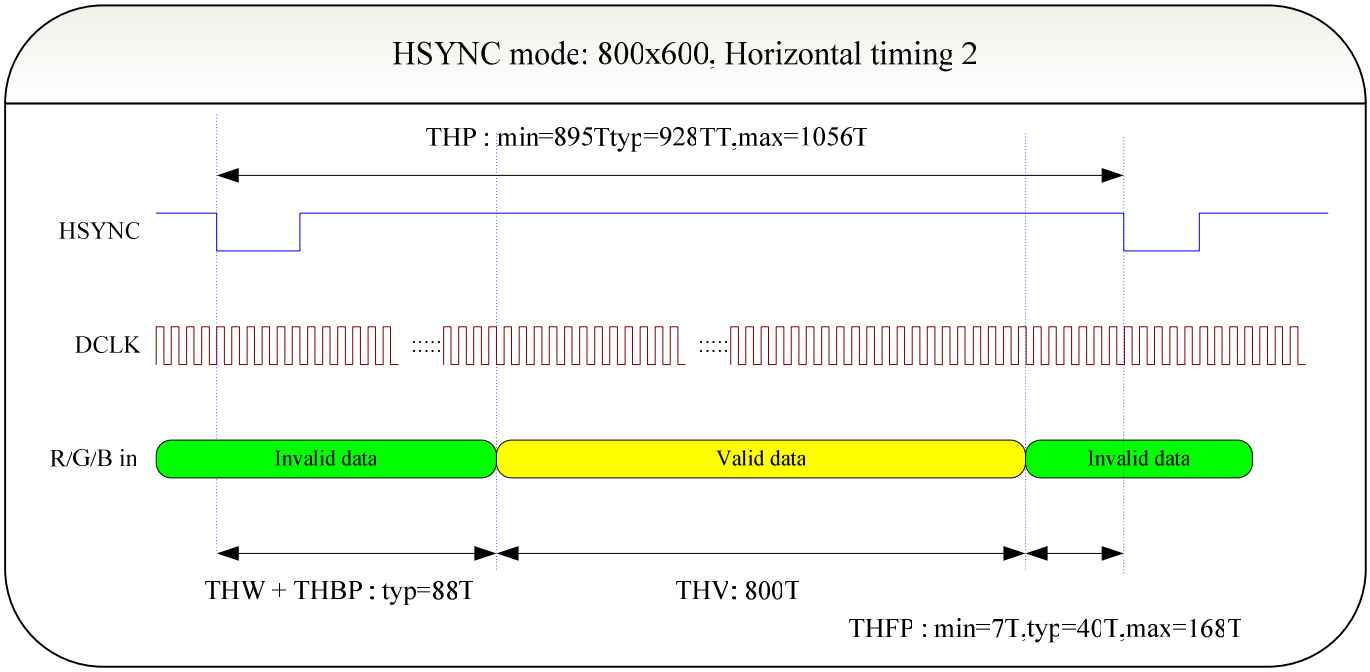
- Waveform 2: HSYNC mode input vertical timing - 2



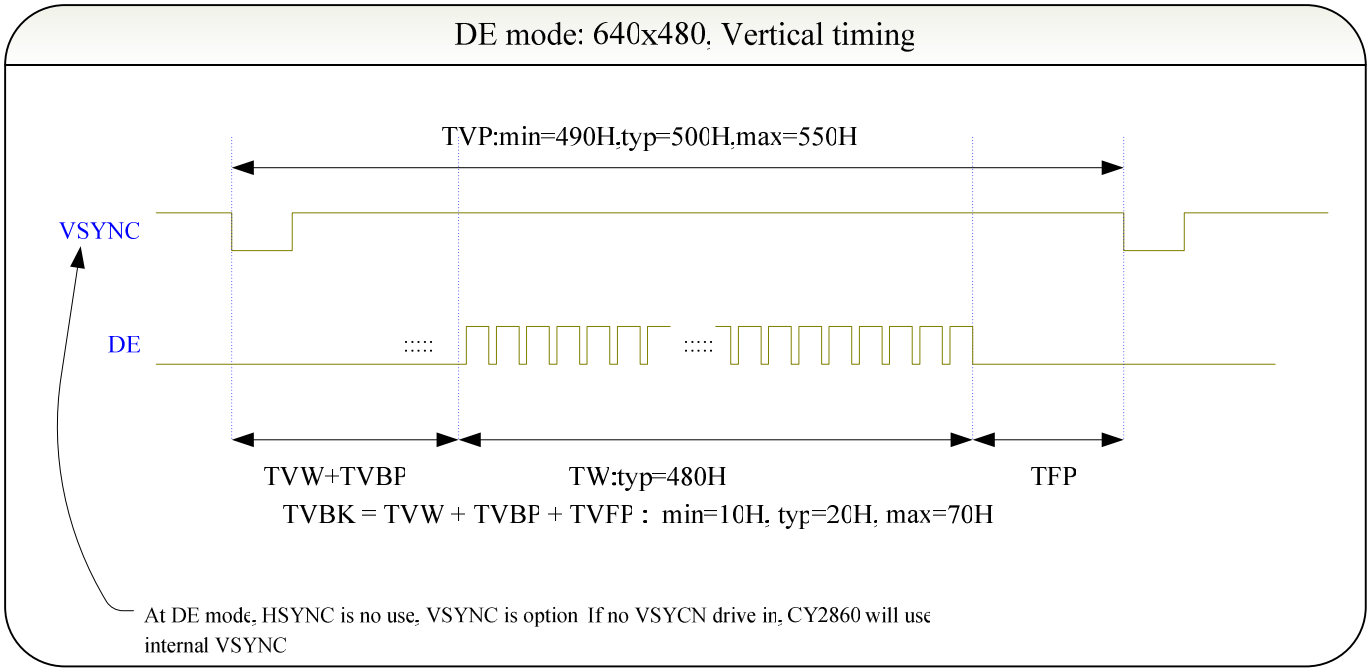
◆ Waveform 3 : HSYNC mode, 800x600, Horizontal timing 1



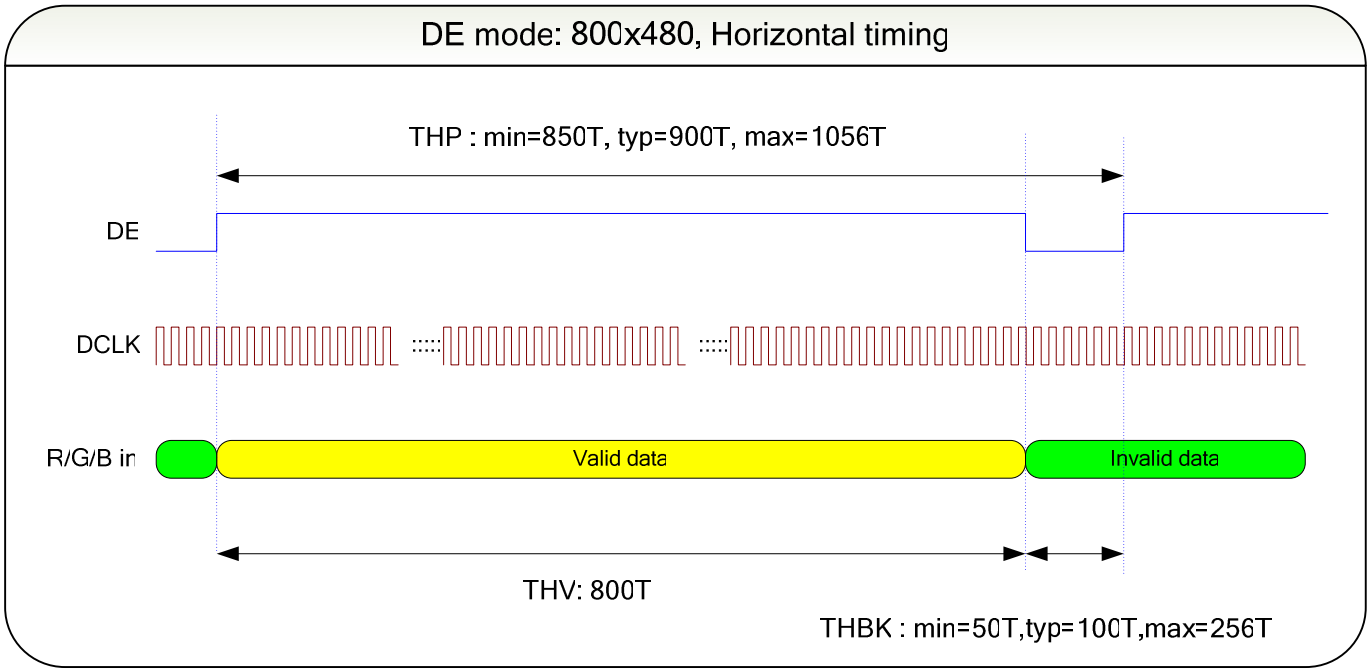
◆ Waveform 4 : HSYNC mode, 800x600, Horzontal timing 2



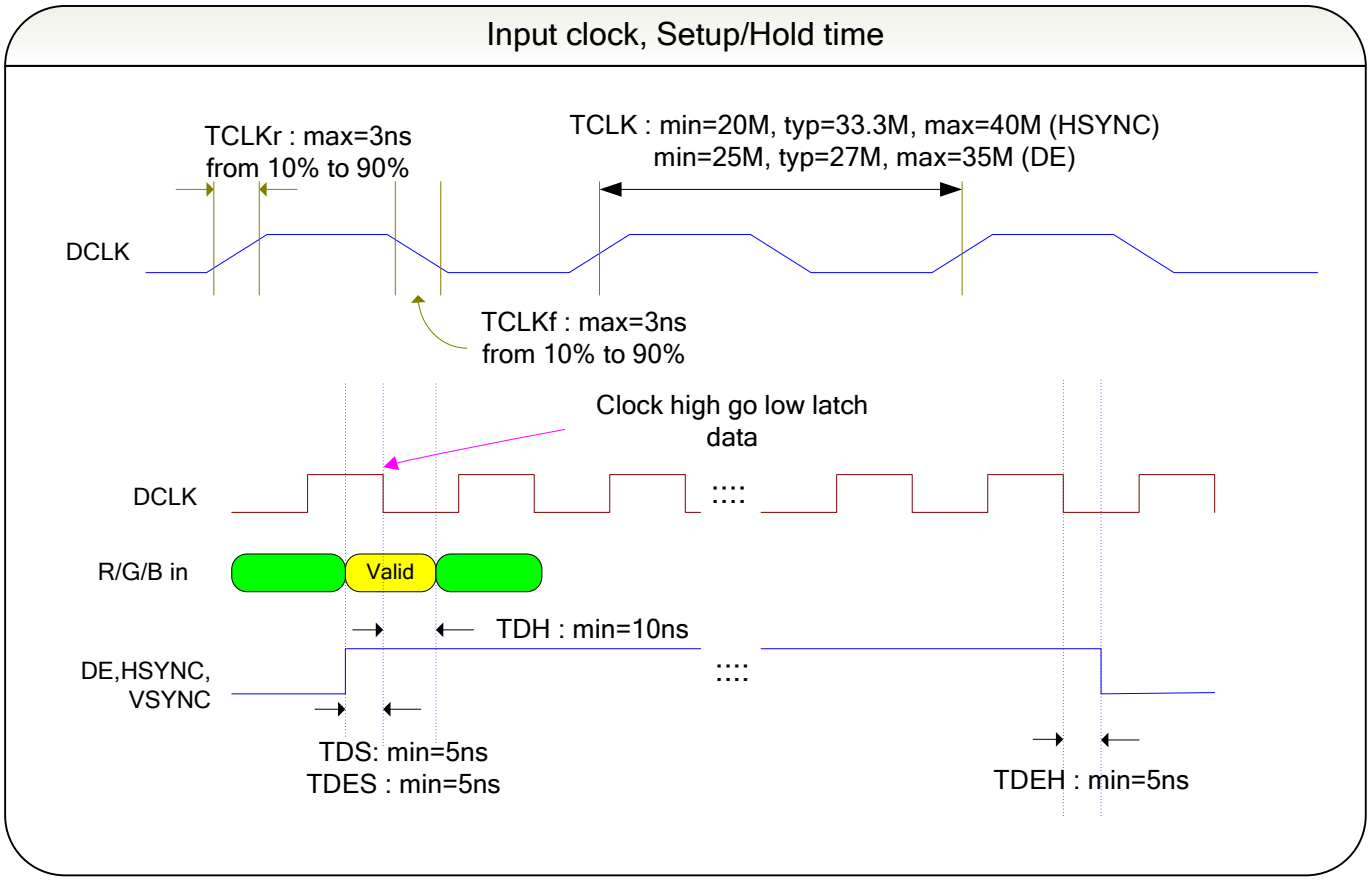
◆ Waveform 5 : DE mode, 640x480, Vertical timing



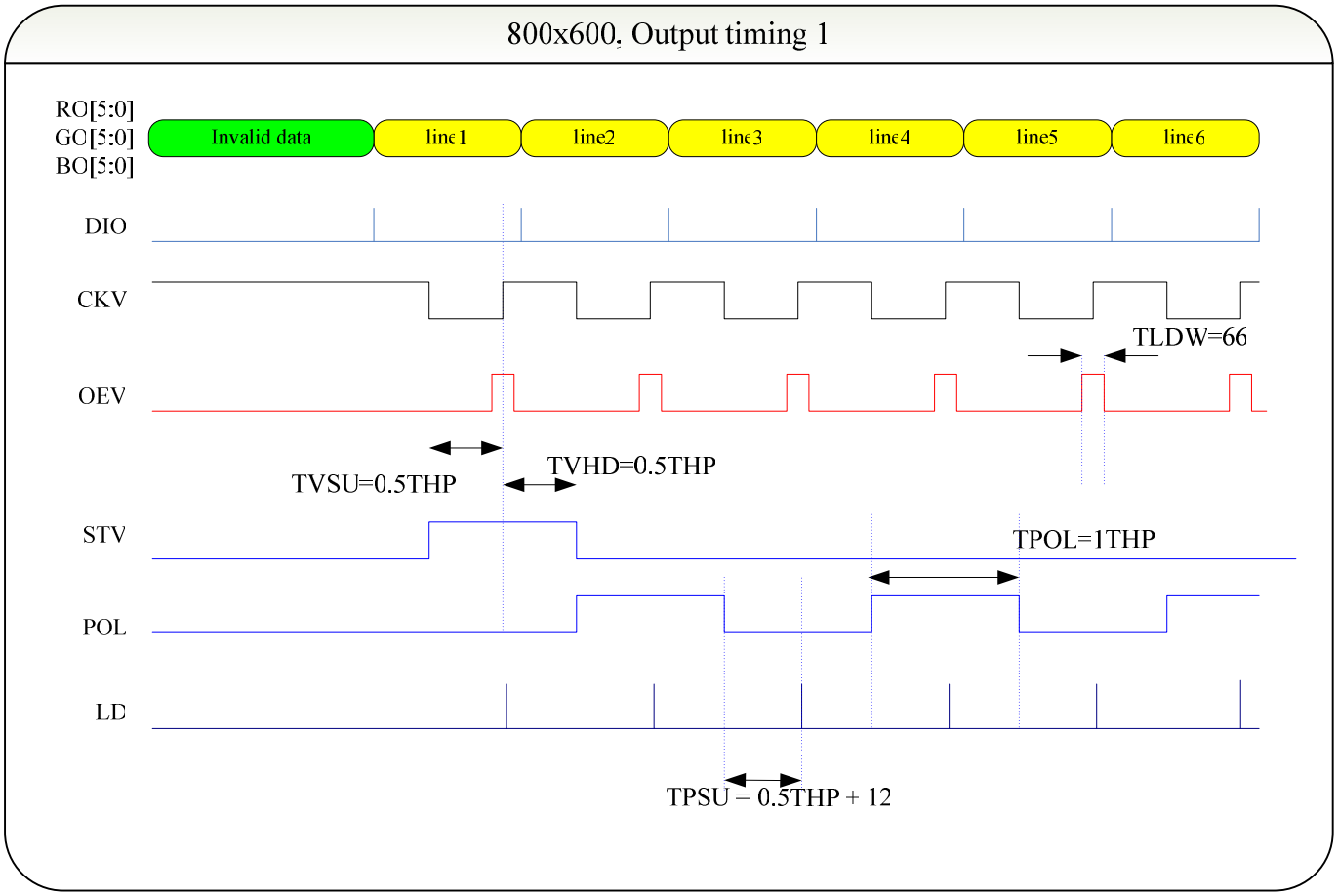
◆ Waveform 6 : DE mode, 800x600, Horizontal timing



◆ Waveform 7: input clock, setup/hold time

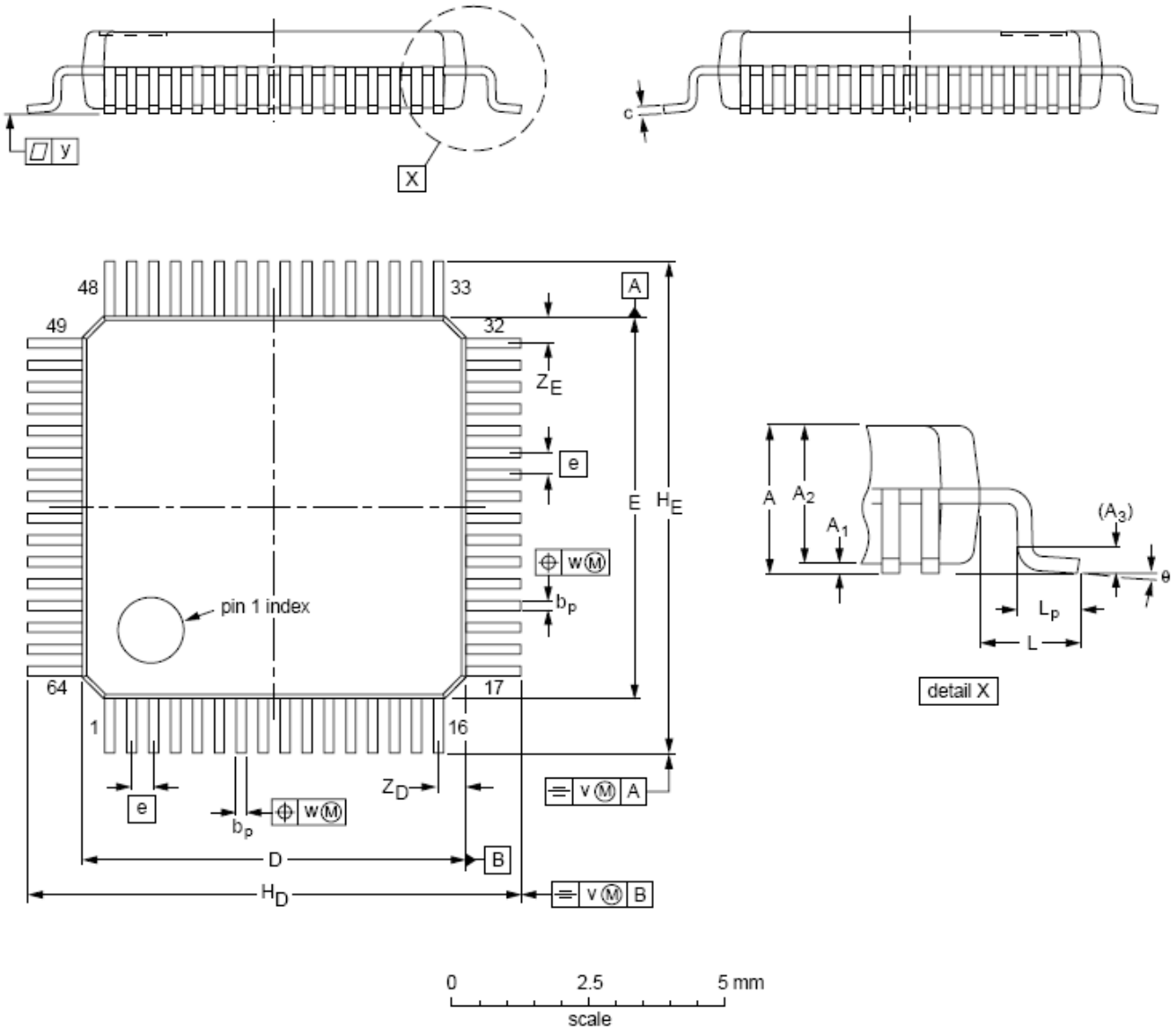


◆ Waveform 8 : 800 x 600, Output timing – 1



11. Package Information

LQFP-64 (7x7x1.4mm)



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.23 0.13	0.20 0.09	7.1 6.9	7.1 6.9	0.4	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.08	0.08	0.64 0.36	0.64 0.36	7° 0°