AO4448

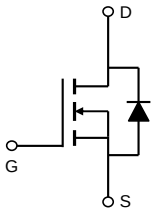
80V N-Channel MOSFET

General Description

The AO4448 is fabricated with SDMOS™ trench technology that combines excellent $R_{DS(ON)}$ with low gate charge and low Qrr.The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

Features

V_{DS}	80V
I_D (at V_{GS}=10V)	10A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 16mΩ
$R_{DS(ON)}$ (at V_{GS} = 7V)	< 20mΩ



Absolute Maximum Ratings T_A=25℃ unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_A=25℃	I_D	10	A
	T_A=70℃		8	
Pulsed Drain Current [C]		I_{DM}	70	
Avalanche Current [C]		I_{AS}, I_{AR}	45	A
Avalanche energy L=0.1mH [C]		E_{AS}, E_{AR}	101	mJ
Power Dissipation [B]	T_A=25℃	P_D	3.1	W
	T_A=70℃		2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	31	40	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		59	75	℃/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	16	24	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	80			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V, V_{GS}=0V			10	μA
		T_J=55℃			50	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±25V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	2.8	3.3	4.2	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	70			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=10A		13	16	mΩ
		T_J=125℃		23.5	28.5	
		V_{GS}=7V, I_D=8A		15.4	20	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=10A		23		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				4	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=40V, f=1MHz	1335	1670	2005	pF
C_{oss}	Output Capacitance		150	215	280	pF
C_{rss}	Reverse Transfer Capacitance		40	72	100	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.35	0.75	1.2	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=40V, I_D=10A	22	28	34	nC
Q_{gs}	Gate Source Charge		8.8	11	13	nC
Q_{gd}	Gate Drain Charge		5	8	11	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=40V, R_L=4Ω, R_{GEN}=3Ω		12		ns
t_r	Turn-On Rise Time			9		ns
$t_{D(off)}$	Turn-Off DelayTime			20		ns
t_f	Turn-Off Fall Time			8		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=10A, dI/dt=500A/μs	14.5	21	27.5	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=10A, dI/dt=500A/μs	45.5	65	85	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25℃. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150℃, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃. Ratings are based on low frequency and duty cycles to keep initialT_J=25℃.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150℃. The SOA curve provides a single pulse ratin g.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

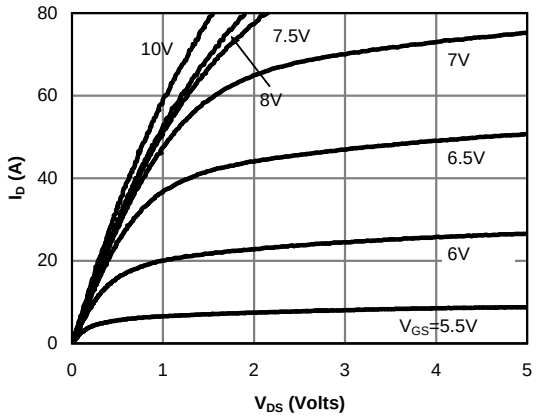


Fig 1: On-Region Characteristics (Note E)

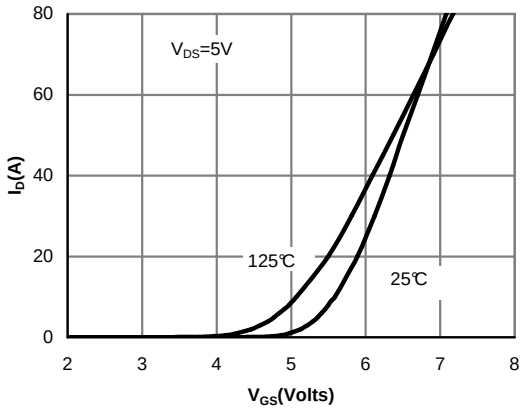


Figure 2: Transfer Characteristics (Note E)

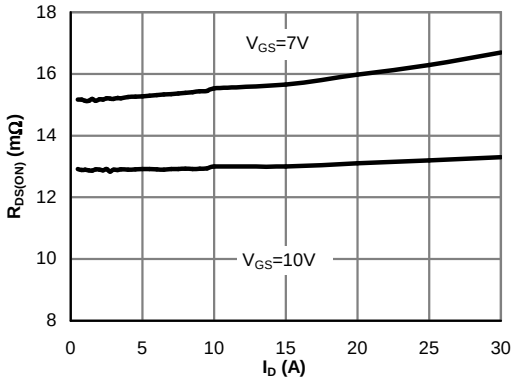


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

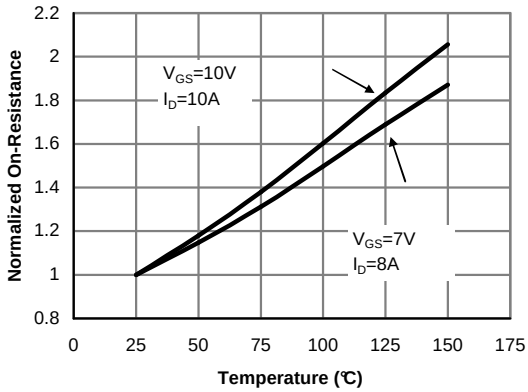


Figure 4: On-Resistance vs. Junction Temperature (Note E)

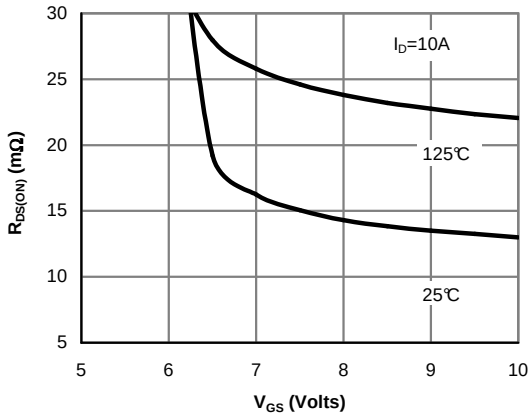


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

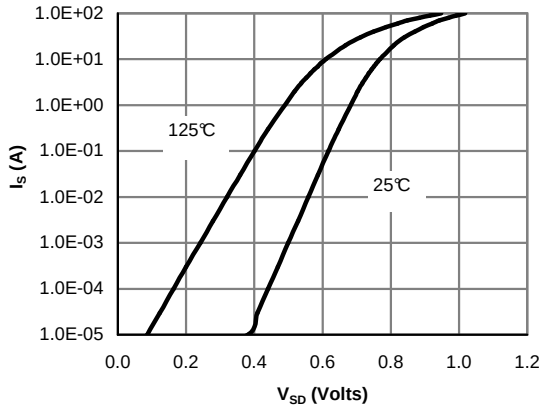


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

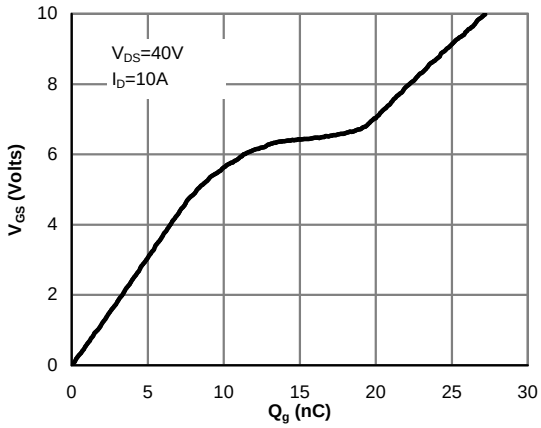


Figure 7: Gate-Charge Characteristics

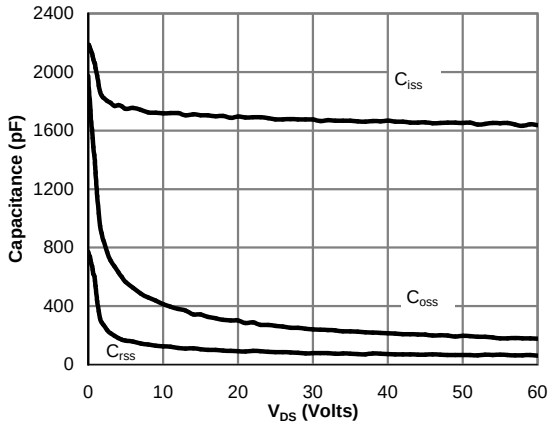


Figure 8: Capacitance Characteristics

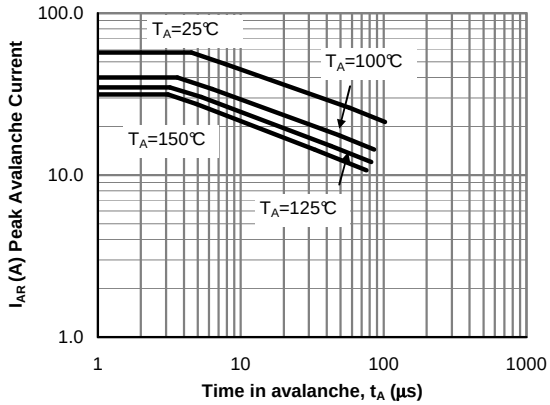


Figure 9: Single Pulse Avalanche capability (Note C)

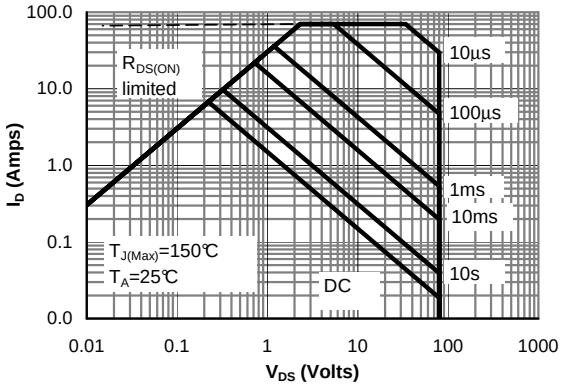


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

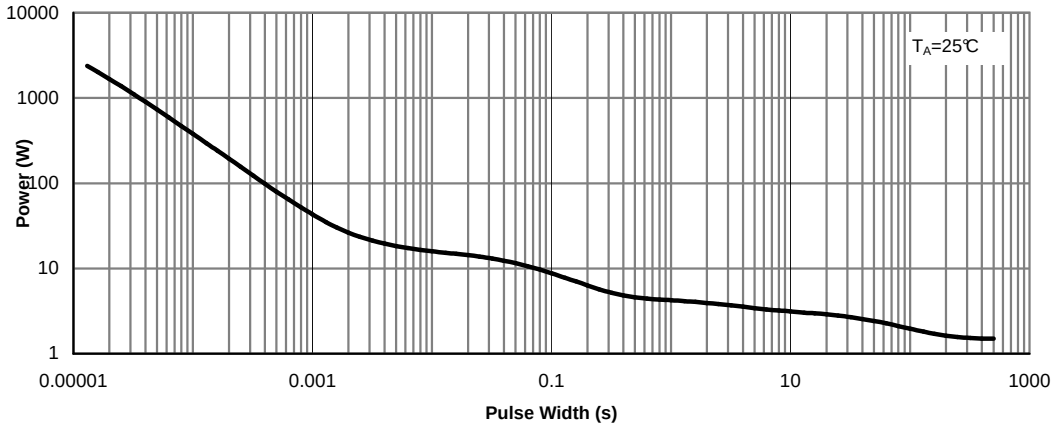


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

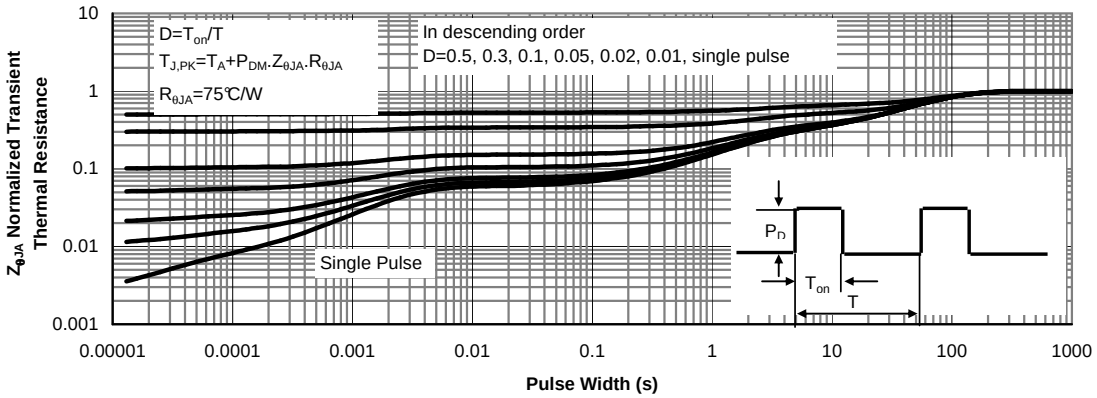


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

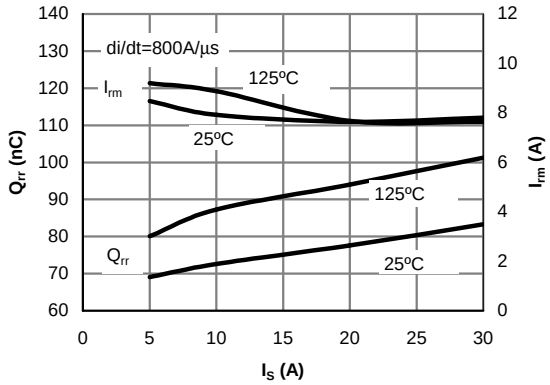


Figure 13: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

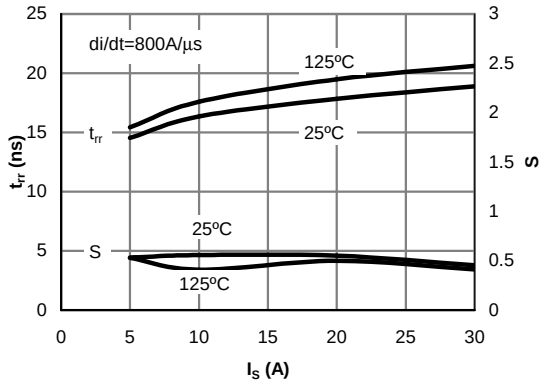


Figure 14: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

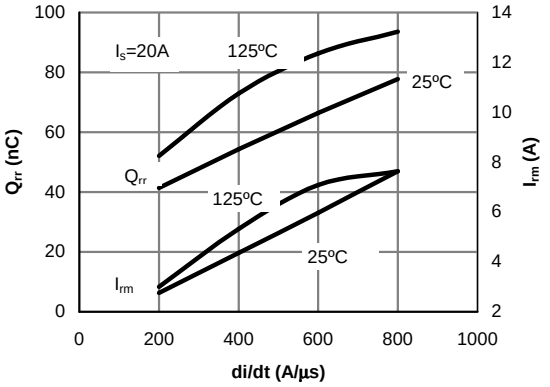


Figure 15: Diode Reverse Recovery Charge and Peak Current vs. di/dt

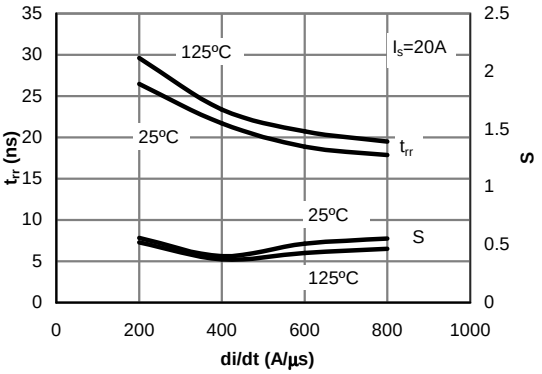
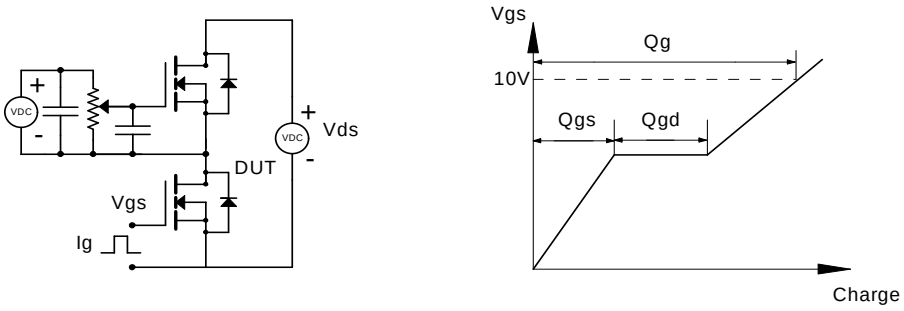
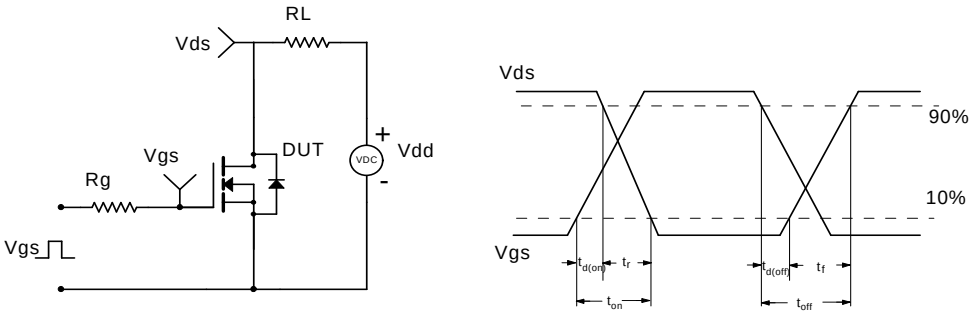


Figure 16: Diode Reverse Recovery Time and Softness Factor vs. di/dt

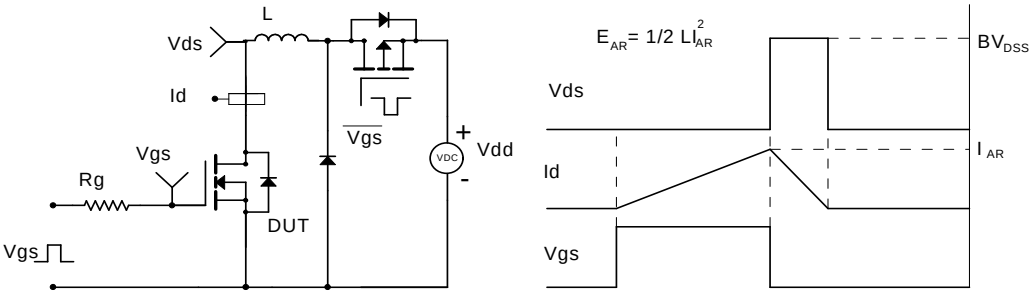
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms