

General Description

The AO4494 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is for PWM applications.

Features

V_{DS} (V) = 30V

I_D = 18A

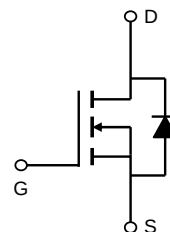
(V_{GS} = 10V)

$R_{DS(ON)} < 6.5m\Omega$

(V_{GS} = 10V)

$R_{DS(ON)} < 9.5m\Omega$

(V_{GS} = 4.5V)



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	18	A
		14	
Pulsed Drain Current ^C	I_{DM}	130	
Avalanche Current ^C	I_{AR}	32	A
Repetitive avalanche energy $L=0.1mH$ ^C	E_{AR}	51	mJ
Power Dissipation ^B	P_D	3.1	W
		2	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	28	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A,B}		59	75	$^\circ\text{C/W}$
Maximum Junction-to-Lead	$R_{\theta JL}$	16	24	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =125°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1.5	2	2.5	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	130			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =18A T _J =125°C		5.4 8.4	6.5 10.1	mΩ
		V _{GS} =4.5V, I _D =16A		7.5	9.5	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =18A		70		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.75	1	V
I _S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz	1270	1590	1900	pF
C _{oss}	Output Capacitance		170	240	310	pF
C _{rss}	Reverse Transfer Capacitance		87	145	200	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.8	1.5	2.3	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =18A	24	30	36	nC
Q _{g(4.5V)}	Total Gate Charge		12	15	18	nC
Q _{gs}	Gate Source Charge		4.2	5.2	6.2	nC
Q _{gd}	Gate Drain Charge		4.7	7.8	11	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =0.83Ω, R _{GEN} =3Ω		6.7		ns
t _r	Turn-On Rise Time			3.5		ns
t _{D(off)}	Turn-Off DelayTime			22.5		ns
t _f	Turn-Off Fall Time			4		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =18A, dI/dt=500A/μs	22	28	34	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =18A, dI/dt=500A/μs	19	24	30	nC

- A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
- B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.
- D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.
- Rev1: Nov. 2010

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

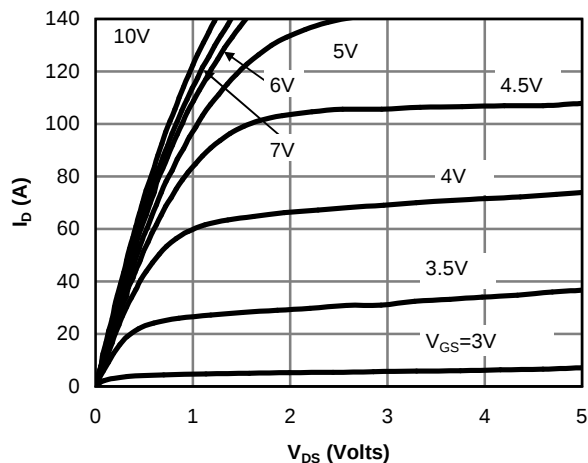


Fig 1: On-Region Characteristics (Note E)

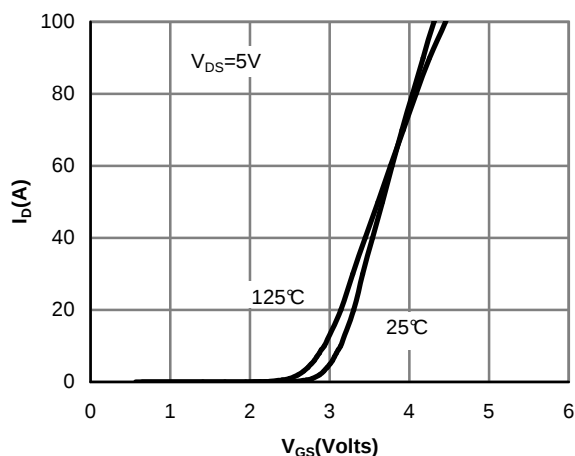


Figure 2: Transfer Characteristics (Note E)

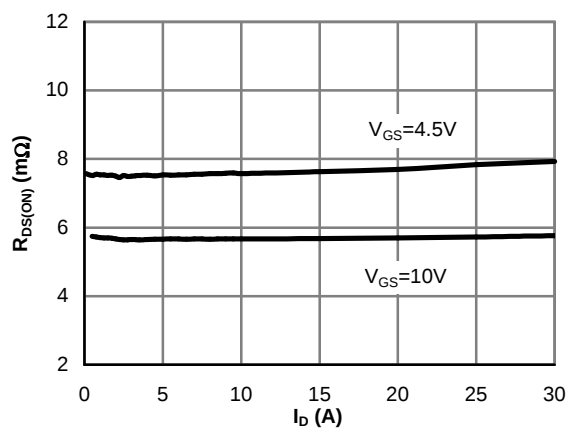


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

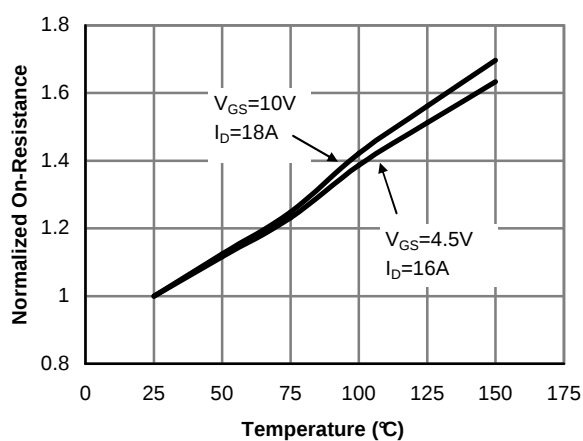


Figure 4: On-Resistance vs. Junction Temperature (Note E)

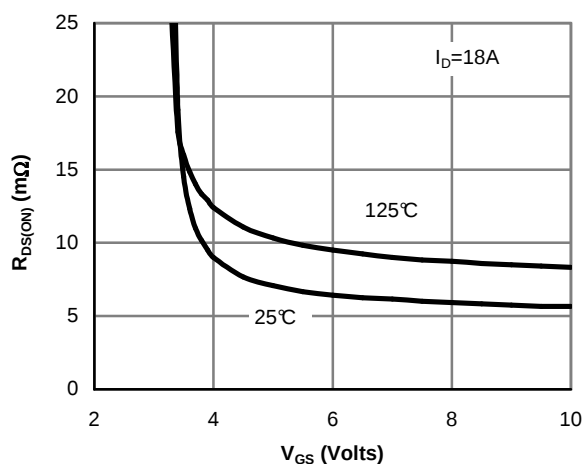


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

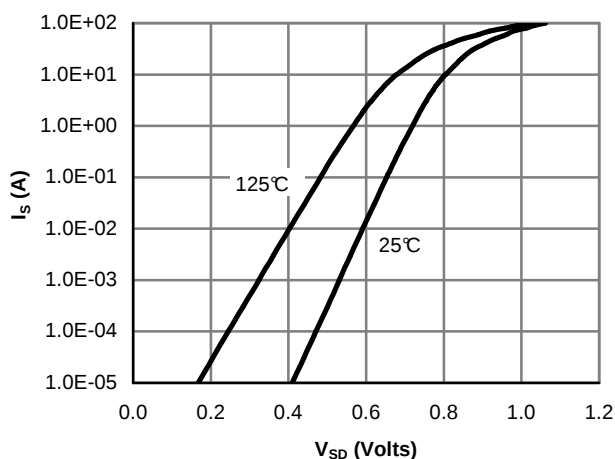
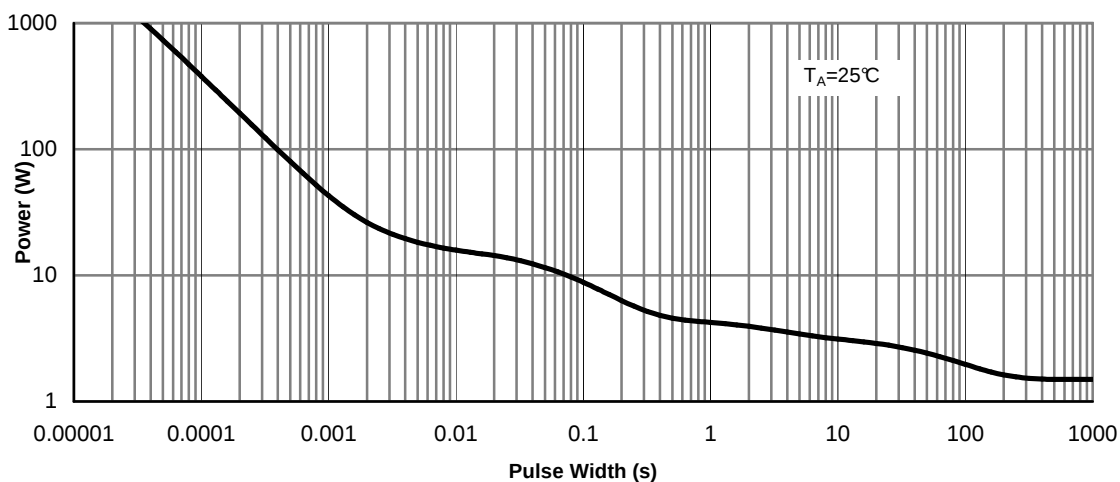
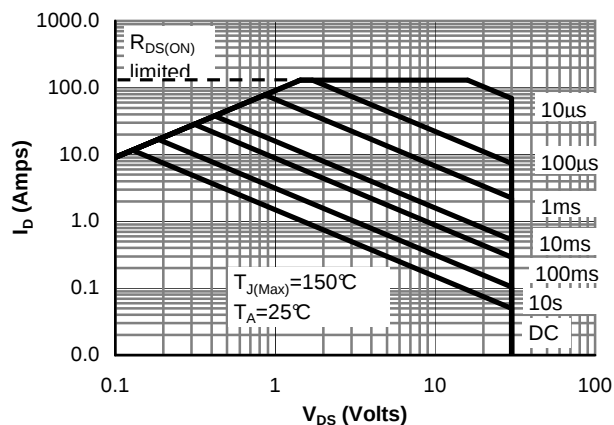
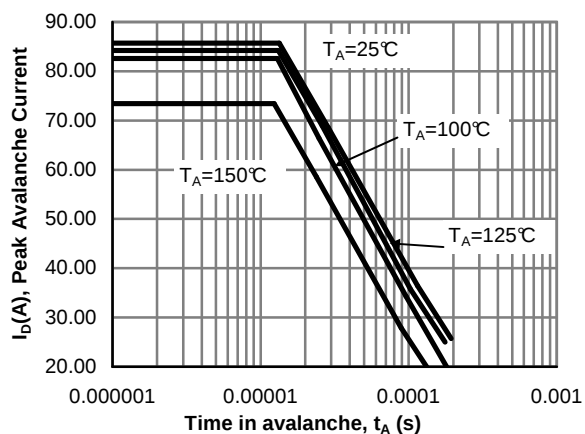
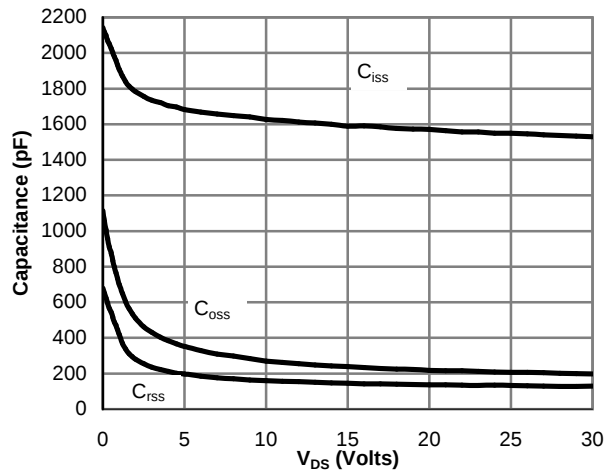
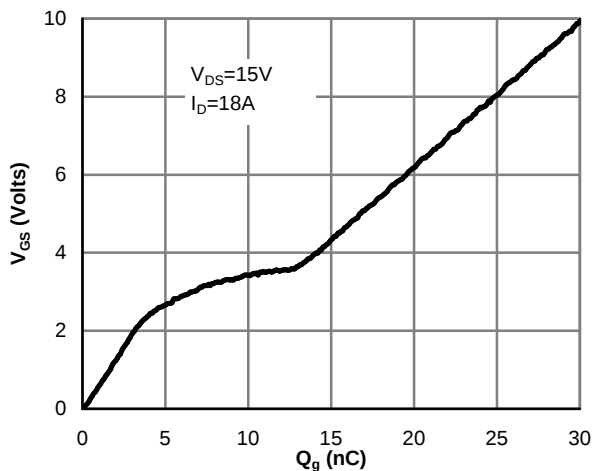


Figure 6: Body-Diode Characteristics (Note E)

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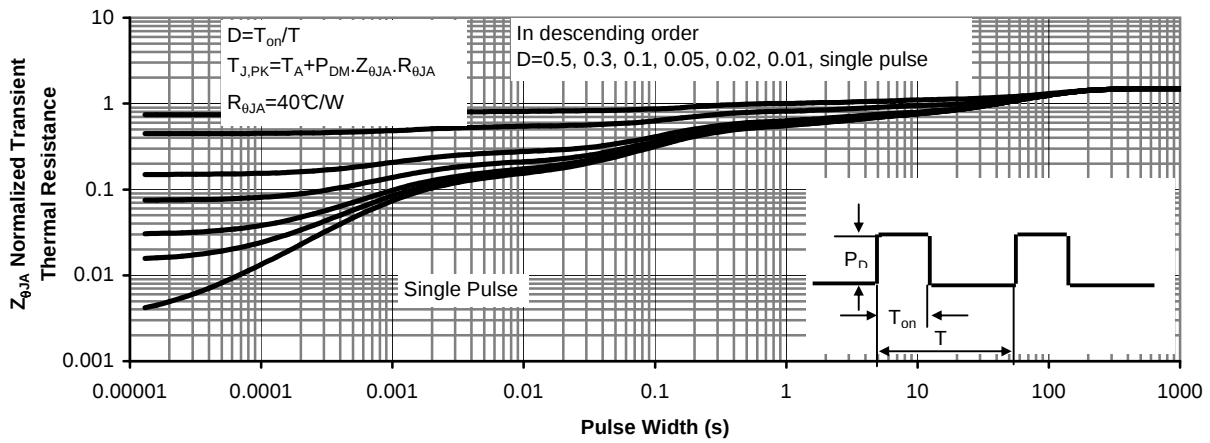
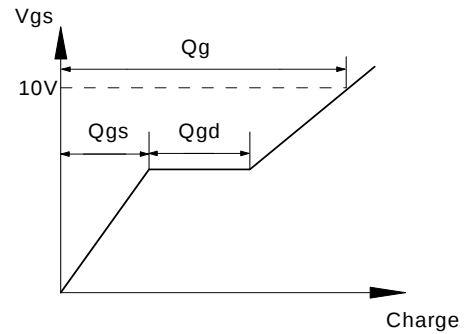
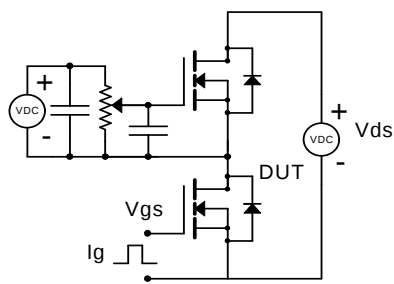
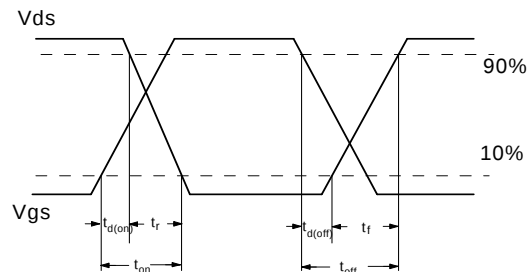
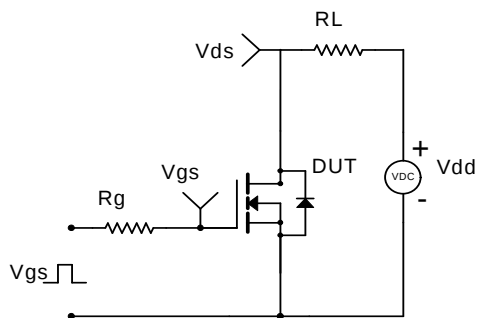


Figure 16: Normalized Maximum Transient Thermal Impedance (Note F)

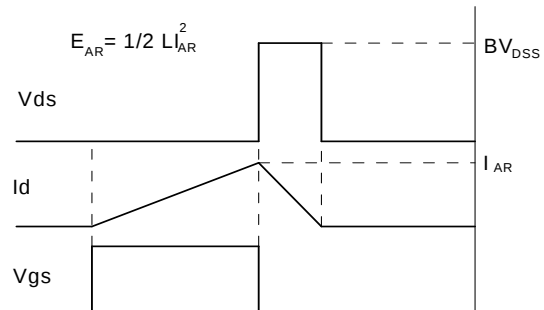
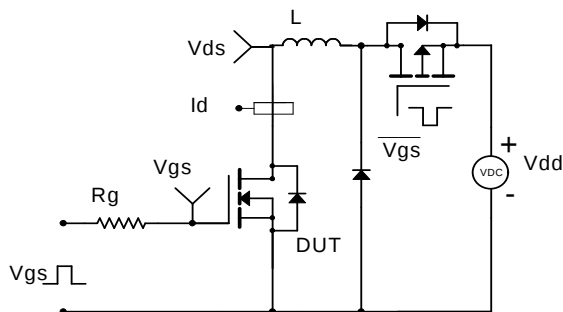
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

