AO4722

30V N-Channel MOSFET

General Description

SRFET™ The AO4722 uses advanced trench technology with a monolithically integrated Schottky diode to provide excellent $R_{DS(ON)}$,and low gate charge. This device is suitable for use as a low side FET in SMPS, load switching and general purpose applications.

Features

V_{DS} (V) = 30V
I_D =11.6A (V_{GS} = 10V)
$R_{DS(ON)}$ < 14mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 22mΩ (V_{GS} = 4.5V)

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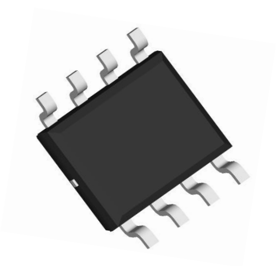

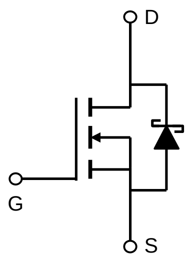

Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	10 Sec	Steady State	Units
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±20		V
Continuous Drain Current [A]	T_A=25℃	I_{DSM}	11.6	8.5	A
	T_A=70℃		9.3	6.8	
Pulsed Drain Current [B]		I_{DM}	100		A
Avalanche Current [B]		I_{AR}	17		A
Repetitive avalanche energy L=0.3mH [B]		E_{AR}	43		mJ
Power Dissipation	T_A=25℃	P_{DSM}	3.1	1.7	W
	T_A=70℃		2.0	1.1	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	32	40	℃/W
Maximum Junction-to-Ambient [A]	Steady-State		60	75	℃/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	17	24	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250uA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			0.1	mA
		T_J=125℃			10	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			0.1	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.3	1.65	2.5	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	100			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=11.6A		11.5	14	mΩ
		T_J=125℃		17	21	
		V_{GS}=4.5V, I_D=9.3A		17.5	22	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=11.6A		28		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.43	0.5	V
I_S	Maximum Body-Diode + Schottky Continuous Current				4	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		903	1100	pF
C_{oss}	Output Capacitance			225		pF
C_{rss}	Reverse Transfer Capacitance			91		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.7	2.6	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=11.6A		15.3	20	nC
Q_g(4.5V)	Total Gate Charge			7.8	10	nC
Q_{gs}	Gate Source Charge			2.0		nC
Q_{gd}	Gate Drain Charge			3.9		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.3Ω, R_{GEN}=3Ω		5.0		ns
t_r	Turn-On Rise Time			9.2		ns
$t_{D(off)}$	Turn-Off DelayTime			17.8		ns
t_f	Turn-Off Fall Time			4.4		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=11.6A, dI/dt=300A/µs		17	20	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=11.6A, dI/dt=300A/µs		30.0		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃. The value in any given application depends on the user's specific board design.
B: Repetitive rating, pulse width limited by junction temperature.
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
D. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
E. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃. The SOA curve provides a single pulse rating.
F. The current rating is based on the t≤ 10s junction to ambient thermal resistance rating.
Rev2: Nov. 2010

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

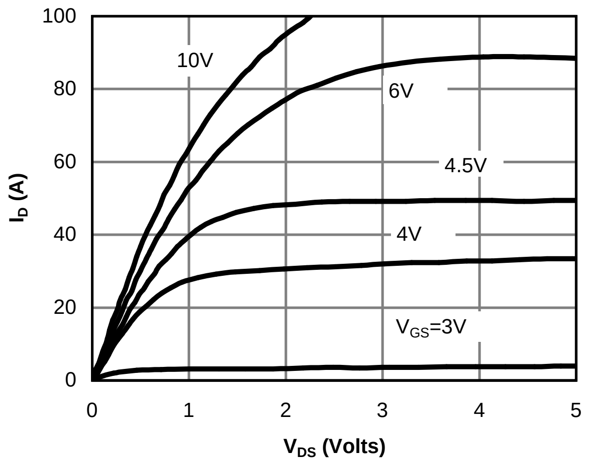

Figure 1: On-Region Characteristics

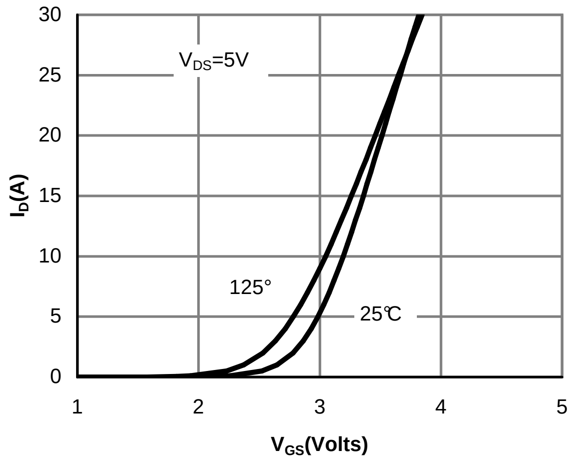

Figure 2: Transfer Characteristics

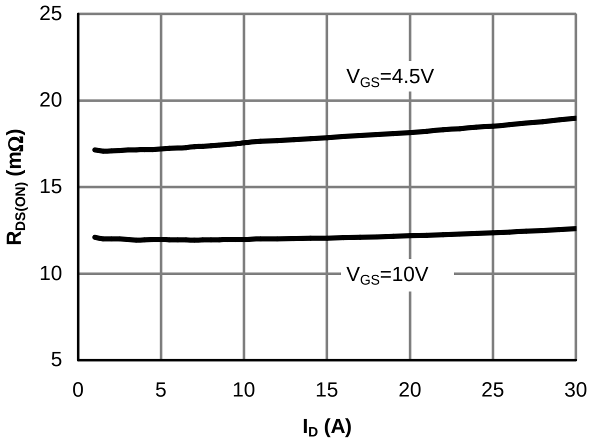

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

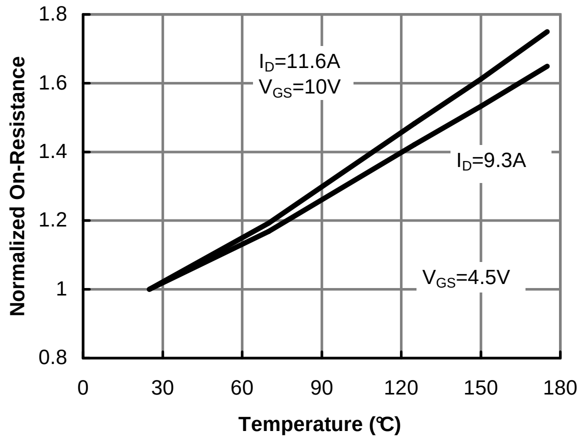

Figure 4: On-Resistance vs. Junction Temperature

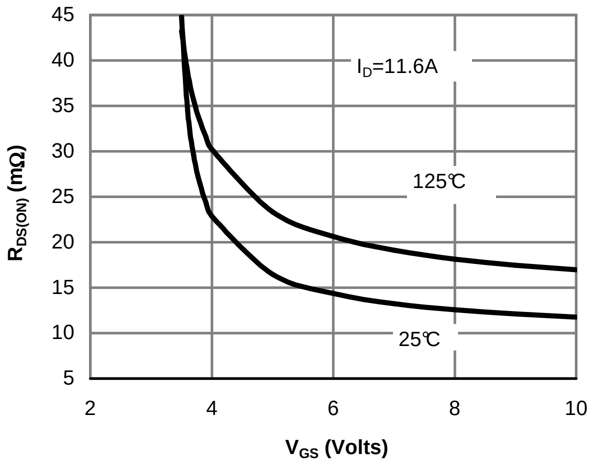

Figure 5: On-Resistance vs. Gate-Source Voltage

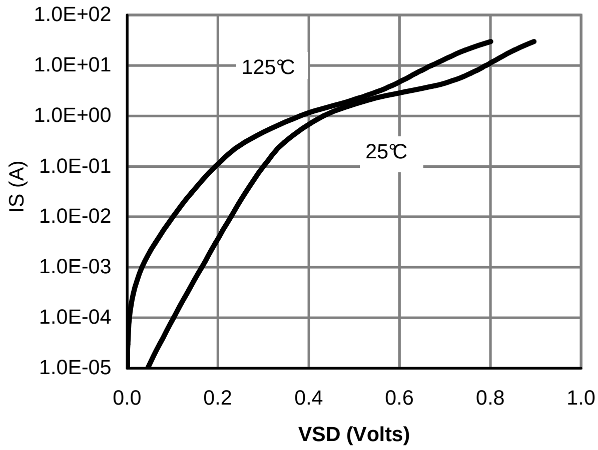

Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

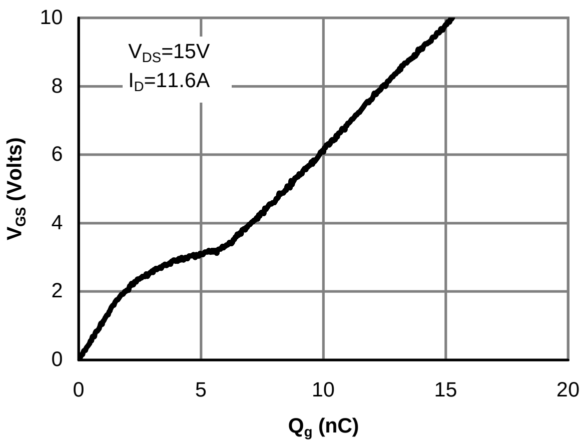

Figure 7: Gate-Charge Characteristics

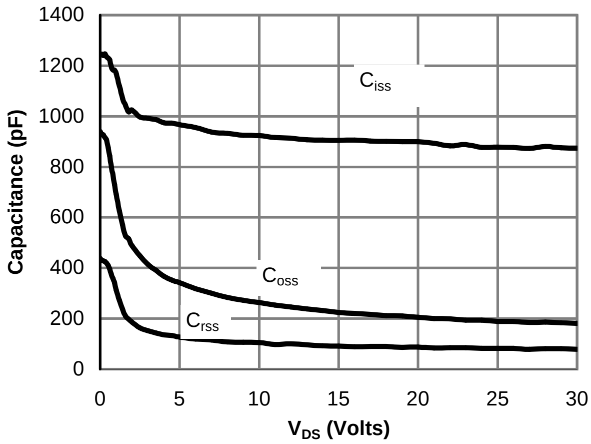

Figure 8: Capacitance Characteristics

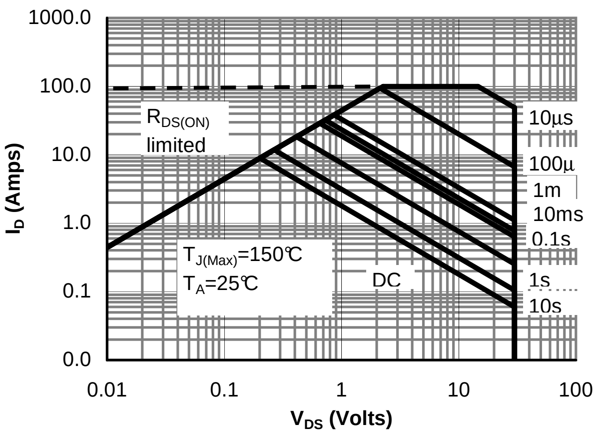

Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

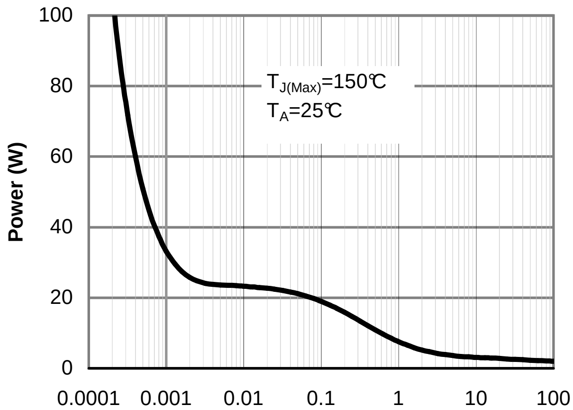

Figure10: Single Pulse Power Rating Junction-to-Ambient (Note E)

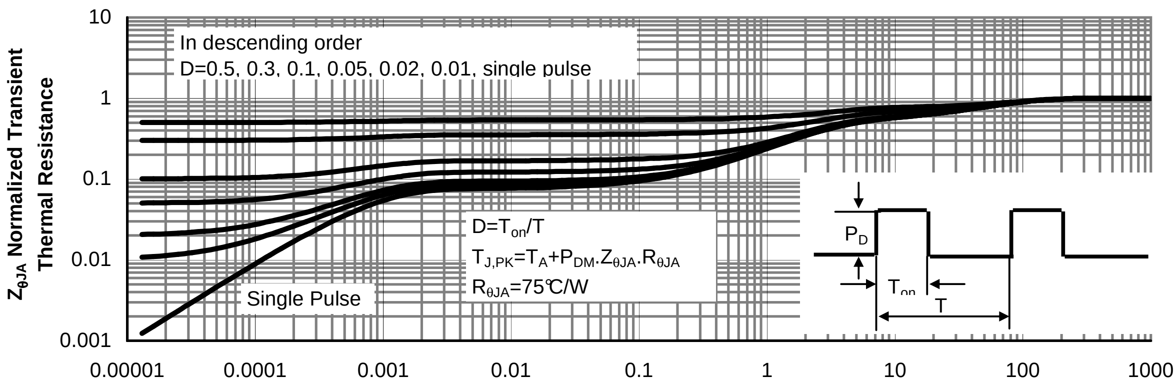

Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)