AO4724

30V N-Channel MOSFET

General Description

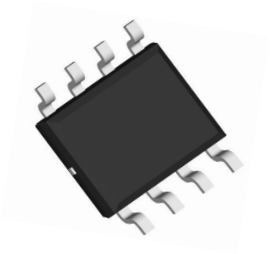
SRFET^{TM} The AO4724 uses advanced trench technology with a monolithically integrated Schottky diode to provide excellent $R_{DS(ON)}$,and low gate charge. This device is suitable for use as a low side FET in SMPS, load switching and general purpose applications.

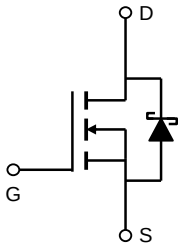
Features

V_{DS} (V) = 30V
I_D = 10.5A (V_{GS} = 10V)
$R_{DS(ON)}$ < 17.5mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 29 mΩ (V_{GS} = 4.5V)

Green Product

SOIC-8





Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum 10 Sec	Maximum Steady State	Units
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±20		V
Continuous Drain Current [AF]	T_A=25℃	I_D	10.5	7.7	A
	T_A=70℃		8.5	6.2	
Pulsed Drain Current [B]		I_{DM}	80		
Power Dissipation	T_A=25℃	P_D	3.1	1.7	W
	T_A=70℃		2.0	1.1	
Avalanche Current [B]		I_{AR}	13		A
Repetitive avalanche energy 0.3mH [B]		E_{AR}	25		mJ
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [AF]	t ≤ 10s	$R_{\theta JA}$	31	40	℃/W
Maximum Junction-to-Ambient [A]	Steady-State		59	75	℃/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	16	24	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			0.1	mA
		T_J=55℃			20	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	1.3	1.64	2	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	80			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=10.5A		14.4	17.5	mΩ
		T_J=125℃		21.5	25.8	
		V_{GS}=4.5V, I_D=8A		22.7	29.0	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=10.5A		23		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.4	0.5	V
I_S	Maximum Body-Diode + Schottky Continuous Current				4.8	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		696	900	pF
C_{oss}	Output Capacitance			199		pF
C_{rss}	Reverse Transfer Capacitance			81		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.2	1.8	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=10.5A		12.4	16	nC
Q_g(4.5V)	Total Gate Charge			6.1	8	nC
Q_{gs}	Gate Source Charge			2.04		nC
Q_{gd}	Gate Drain Charge			2.7		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.43Ω, R_{GEN}=3Ω		2.6		ns
t_r	Turn-On Rise Time			6.8		ns
$t_{D(off)}$	Turn-Off DelayTime			17		ns
t_f	Turn-Off Fall Time			3.6		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=10.5A, dI/dt=300A/μs		20.2	26	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=10.5A, dI/dt=300A/μs		7.9		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃. The value in any given application depends on the user's specific board design.
B: Repetitive rating, pulse width limited by junction temperature.
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
D. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.
E. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃. The SOA curve provides a single pulse rating.
F. The current rating is based on the t≤ 10s junction to ambient thermal resistance rating.
Rev2: Nov. 2010

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

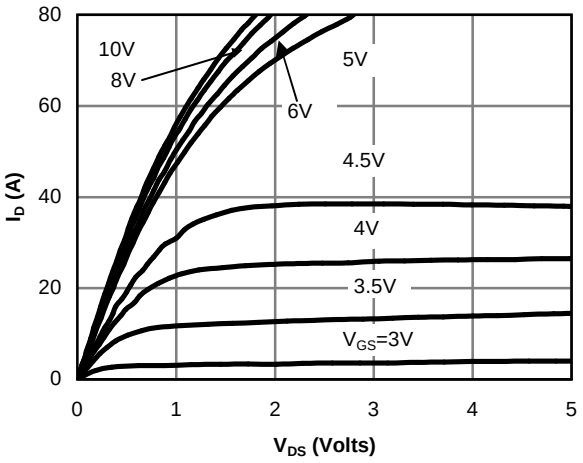


Fig 1: On-Region Characteristics

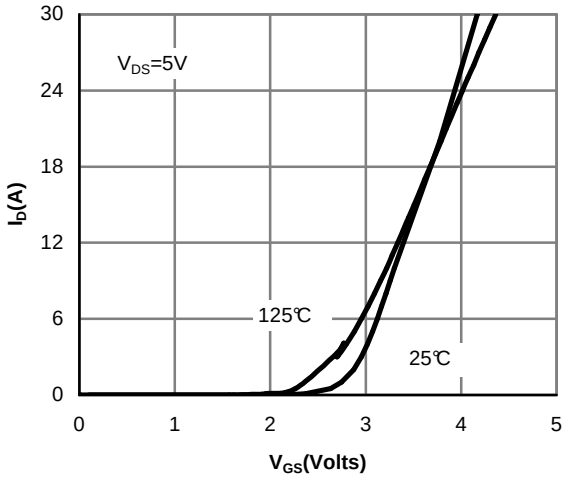


Figure 2: Transfer Characteristics

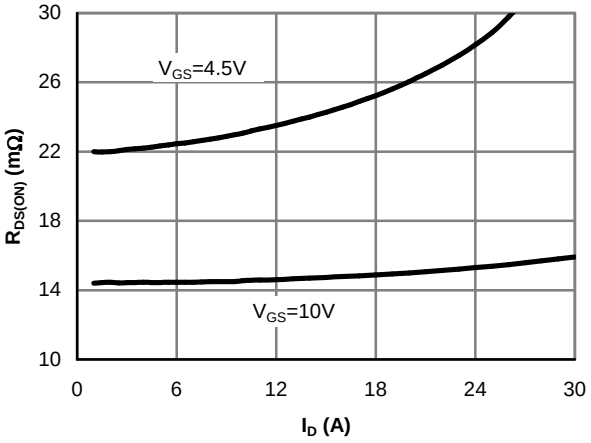


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

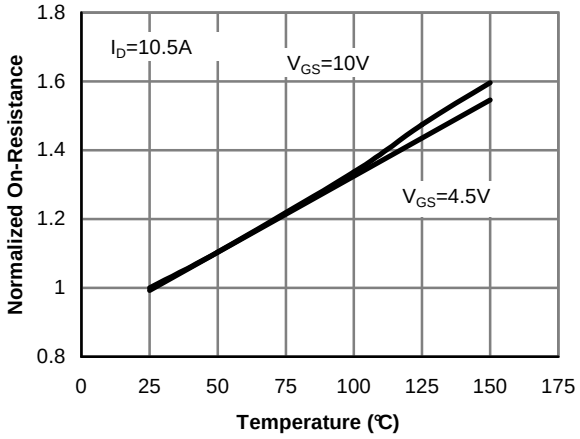


Figure 4: On-Resistance vs. Junction Temperature

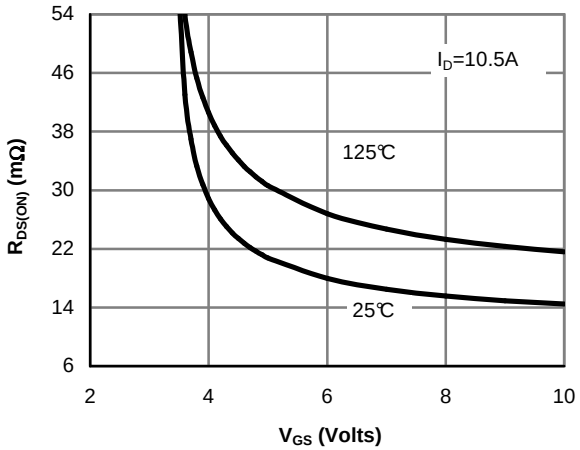


Figure 5: On-Resistance vs. Gate-Source Voltage

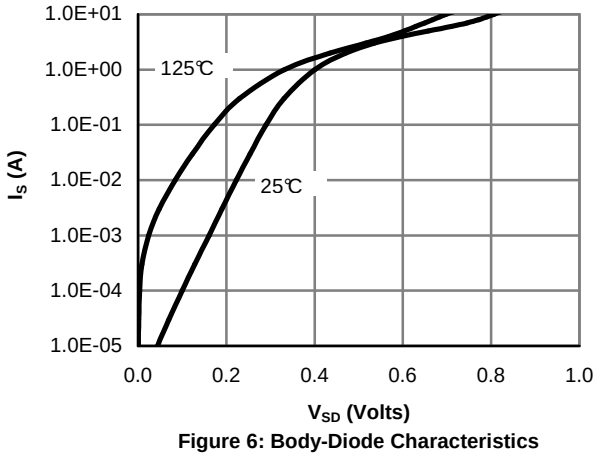


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

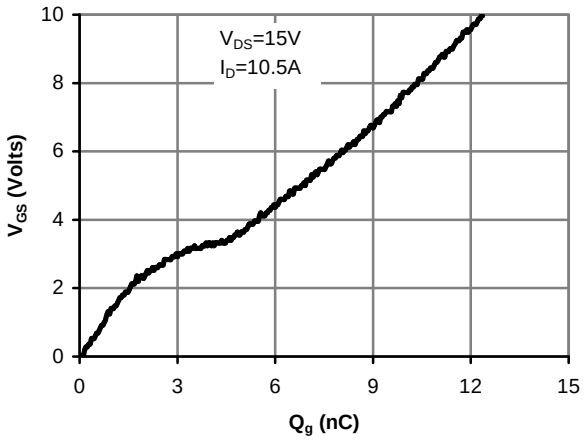


Figure 7: Gate-Charge Characteristics

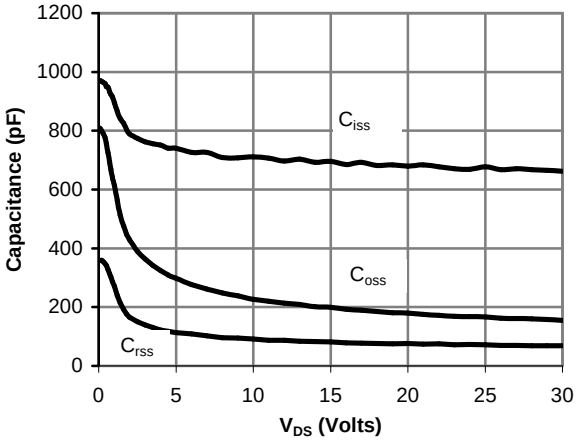


Figure 8: Capacitance Characteristics

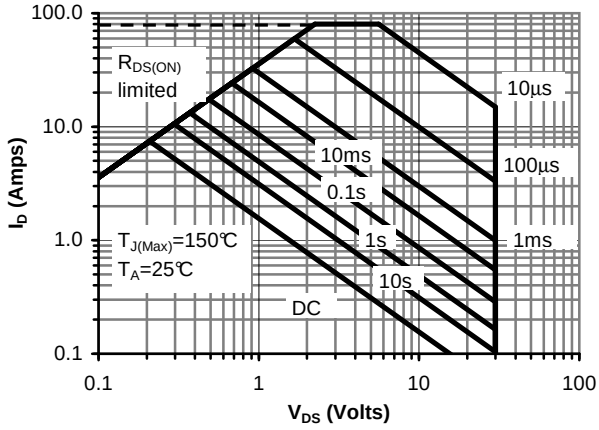


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

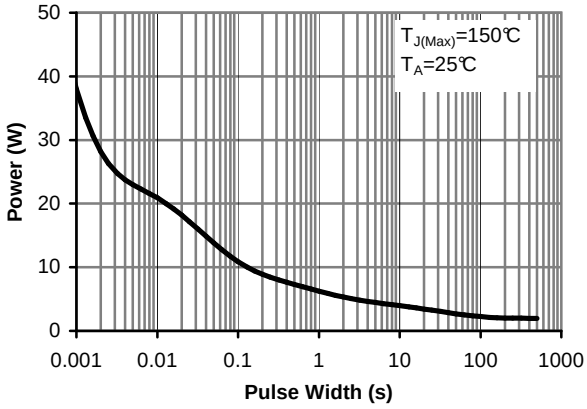


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

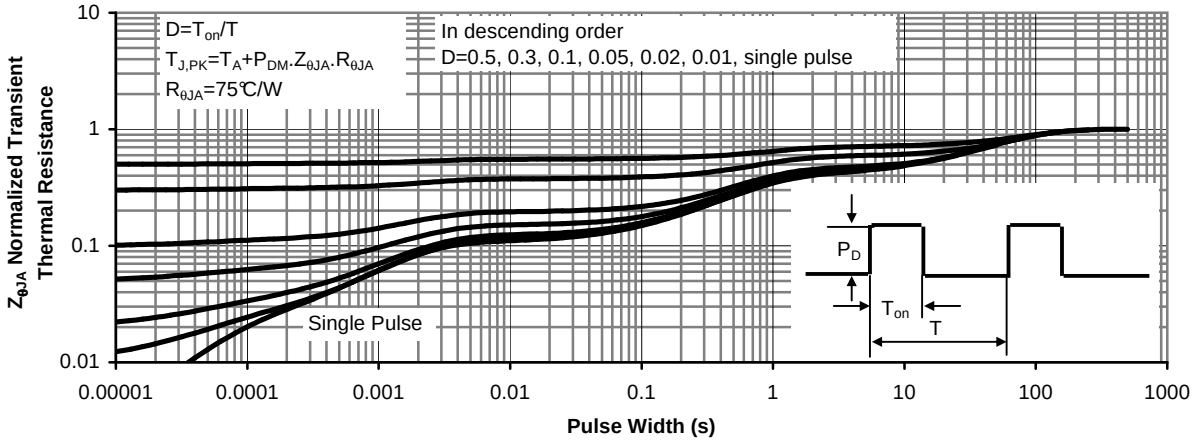


Figure 11: Normalized Maximum Transient Thermal Impedance