AO4826

60V *Dual N-channel MOSFET*

General Description

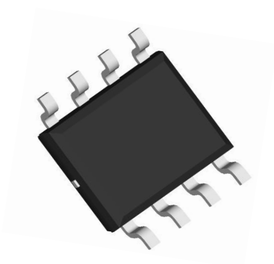
The AO4826 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications.

Features

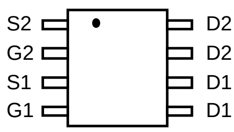
V_{DS} (V) = 60V
I_D = 6.3A (V_{GS} = 10V)
$R_{DS(ON)}$ < 25mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 30mΩ (V_{GS} = 4.5V)

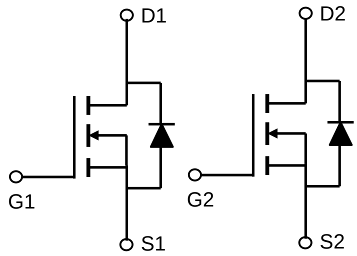
100% UIS Tested
100% Rg Tested

SOIC-8



Top View





Absolute Maximum Ratings T_A=25℃ unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [A]	T_A=25℃	I_D	6.3	A
	T_A=70℃		5	
Pulsed Drain Current [B]		I_{DM}	40	
Power Dissipation	T_A=25℃	P_D	2	W
	T_A=70℃		1.28	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	50	62.5	℃/W
Maximum Junction-to-Ambient [A]	Steady-State		73	110	℃/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	31	40	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V		60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=48V, V_{GS}=0V				1	µA
			T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V				100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA		1	2.1	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V		40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=6.3A			20	25	mΩ
			T_J=125℃		34	42	
		V_{GS}=4.5V, I_D=5.7A			22	30	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=6.3A			27		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V			0.74	1	V
I_S	Maximum Body-Diode Continuous Current					3	A
I_{SM}	Pulsed Body Diode Current [B]					40	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, f=1MHz			1920	2300	pF
C_{oss}	Output Capacitance				155		pF
C_{rss}	Reverse Transfer Capacitance				116		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz			0.65	0.8	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=30V, I_D=6.3A			47.6	58	nC
Q_g(4.5V)	Total Gate Charge				24.2	30	nC
Q_{gs}	Gate Source Charge				6		nC
Q_{gd}	Gate Drain Charge				14.4		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=30V, R_L=4.7Ω, R_{GEN}=3Ω			7.6		ns
t_r	Turn-On Rise Time				5		ns
$t_{D(off)}$	Turn-Off DelayTime				28.9		ns
t_f	Turn-Off Fall Time				5.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=6.3A, dI/dt=100A/µs			33.2	40	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=6.3A, dI/dt=100A/µs			43		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.
B: Repetitive rating, pulse width limited by junction temperature.
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
D. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃. The SOA curve provides a single pulse rating.
Rev 6 : Nov. 2010

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

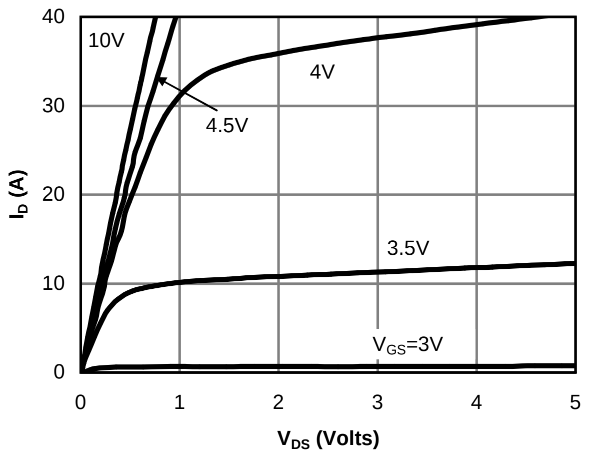


Fig 1: On-Region Characteristics

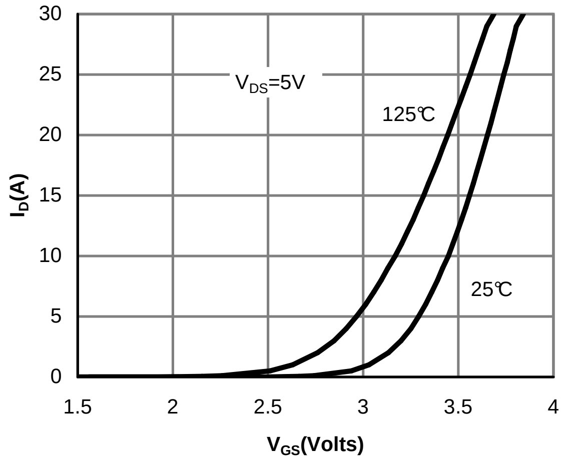


Figure 2: Transfer Characteristics

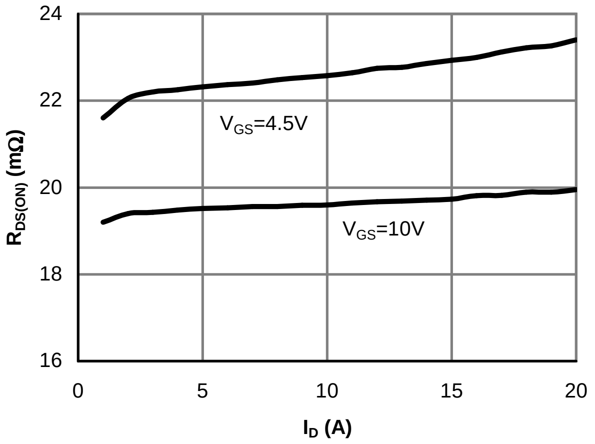


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

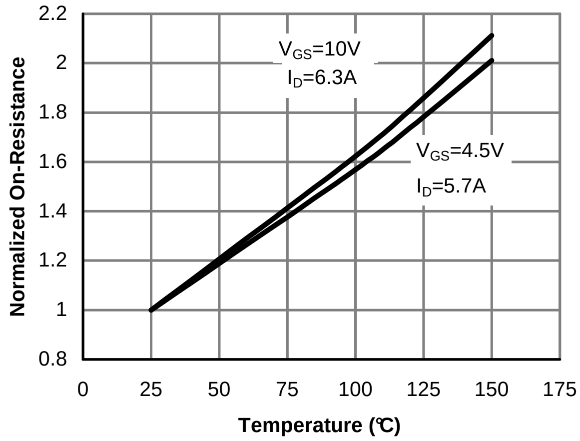


Figure 4: On-Resistance vs. Junction Temperature

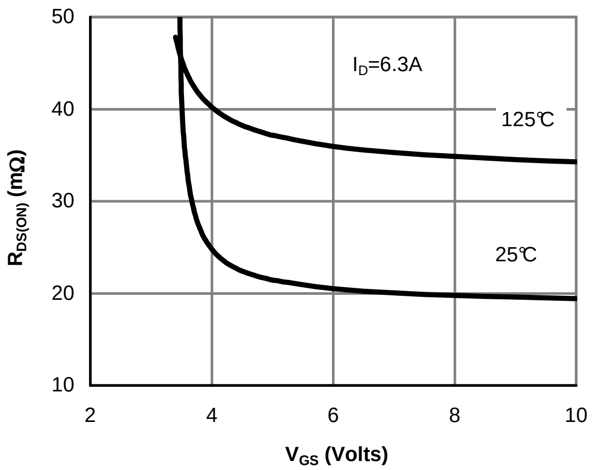


Figure 5: On-Resistance vs. Gate-Source Voltage

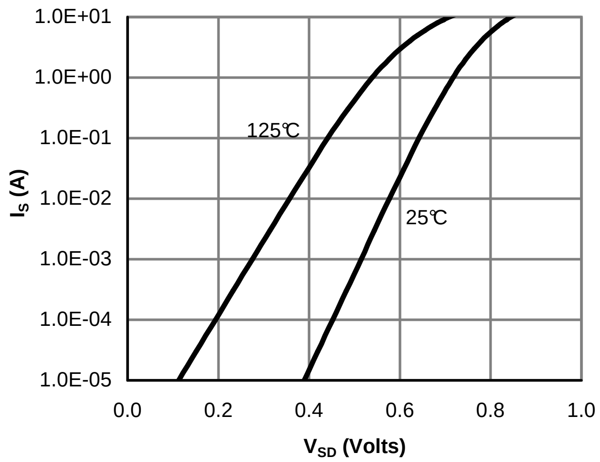


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

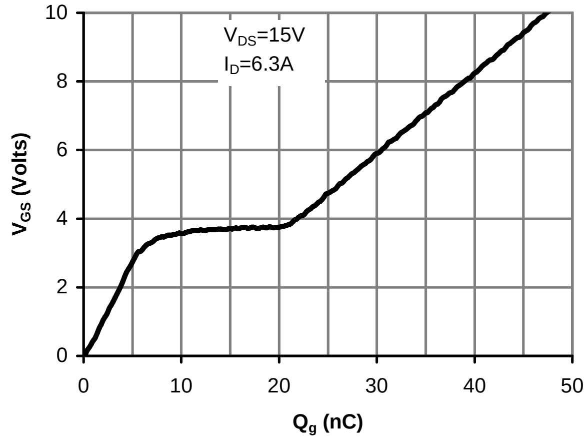


Figure 7: Gate-Charge Characteristics

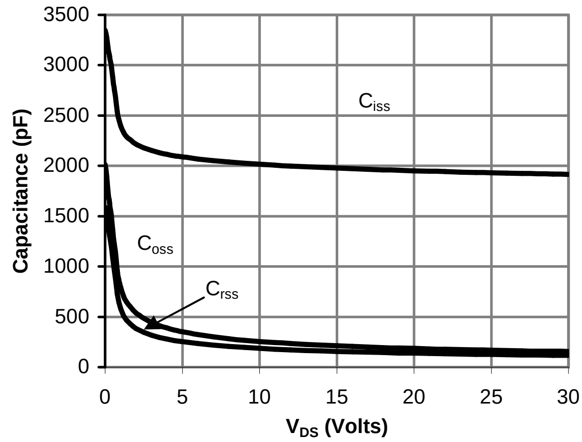


Figure 8: Capacitance Characteristics

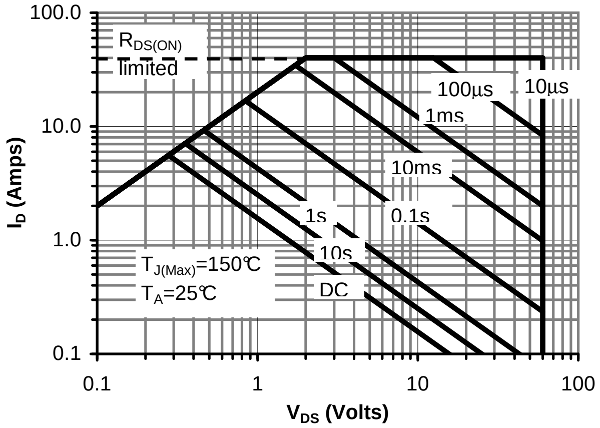


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

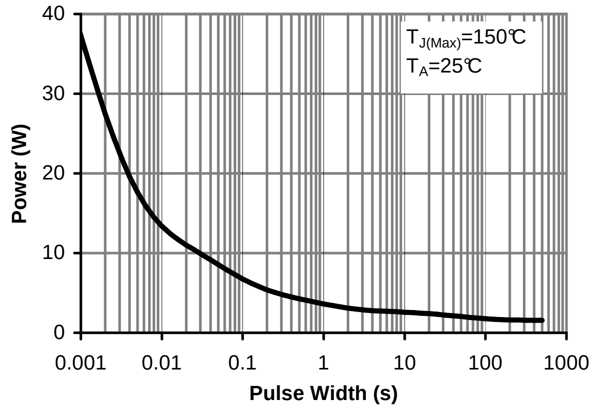


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

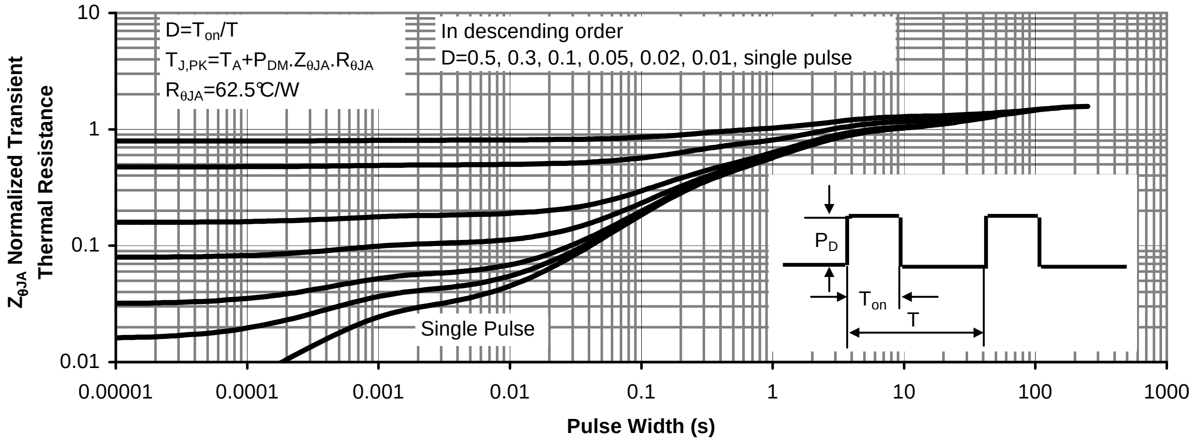


Figure 11: Normalized Maximum Transient Thermal Impedance