# AO4948

## 30V Dual N-Channel MOSFET

## General Description

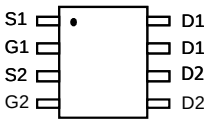
The AO4948 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. The two MOSFETs make a compact and efficient switch and synchronous rectifier combination for use in DC-DC converters. A monolithically integrated Schottky diode in parallel with the synchronous MOSFET to boost efficiency further.

## Features

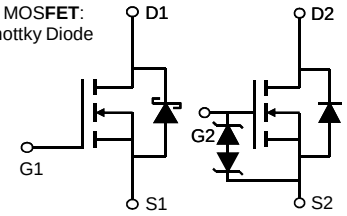
| FET1(N-Channel) | FET2(N-Channel) |
|---|---|
| $V_{DS}$= 30V | 30V |
| $I_D$= 8.8A ($V_{GS}$=10V) | 8A ($V_{GS}$=10V) |
| $R_{DS(ON)}$ | $R_{DS(ON)}$ |
| < 16mΩ ($V_{GS}$=10V) | < 19mΩ ($V_{GS}$=10V) |
| < 22mΩ ($V_{GS}$=4.5V) | < 28mΩ ($V_{GS}$=4.5V) |

Green Product

Top View




SRFET™
Soft Recovery MOSFET: Integrated Schottky Diode




| Absolute Maximum Ratings $T_A$=25℃ unless otherwise noted | | | | | |
|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Max FET1** | **Max FET2** | **Units** |
| Drain-Source Voltage | | $V_{DS}$ | 30 | 30 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | ±20 | V |
| Continuous Drain Current | $T_A$=25℃ | $I_D$ | 8.8 | 8 | A |
| | $T_A$=70℃ | | 7.1 | 6.5 | |
| Pulsed Drain Current [C] | | $I_{DM}$ | 60 | 40 | |
| Avalanche Current [C] | | $I_{AS}$, $I_{AR}$ | 21 | 13 | A |
| Avalanche energy L=0.3mH [C] | | $E_{AS}$, $E_{AR}$ | 66 | 25 | mJ |
| Power Dissipation [B] | $T_A$=25℃ | $P_D$ | 2 | 2 | W |
| | $T_A$=70℃ | | 1.3 | 1.3 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | | ℃ |

| Thermal Characteristics | | | | | |
|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Typ** | **Max** | **Units** |
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 48 | 62.5 | ℃/W |
| Maximum Junction-to-Ambient [A D] | Steady-State | | 74 | 90 | ℃/W |
| Maximum Junction-to-Lead | Steady-State | $R_{\theta JL}$ | 32 | 40 | ℃/W |

**FET1 Electrical Characteristics ($T_J$=25℃ unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=250uA, $V_{GS}$=0V | 30 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=30V, $V_{GS}$=0V | | | 0.1 | mA |
| | | $T_J$=125℃ | | | 20 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$=±20V | | | 100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ $I_D$=250μA | 1.1 | 1.65 | 2.2 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=10V, $V_{DS}$=5V | 60 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=10V, $I_D$=8.8A | | 13.3 | 16 | mΩ |
| | | $T_J$=125℃ | | 20 | 25 | |
| | | $V_{GS}$=4.5V, $I_D$=7A | | 18 | 22 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=8.8A | | 29 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=1A,$V_{GS}$=0V | | 0.41 | 0.5 | V |
| $I_S$ | Maximum Body-Diode + Schottky Continuous Current | | | | 3.5 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=15V, f=1MHz | | 1267 | 1600 | pF |
| $C_{oss}$ | Output Capacitance | | | 308 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 118 | | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | | 1.3 | 2.0 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$=10V, $V_{DS}$=15V, $I_D$=8.8A | | 21 | 30 | nC |
| $Q_g$(4.5V) | Total Gate Charge | | | 10.4 | | nC |
| $Q_{gs}$ | Gate Source Charge | | | 3 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | 3.6 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=15V, $R_L$=1.7Ω, $R_{GEN}$=3Ω | | 5.2 | | ns |
| $t_r$ | Turn-On Rise Time | | | 3.8 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 21.2 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 4.4 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=8.8A, dI/dt=300A/μs | | 11.2 | 15 | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=8.8A, dI/dt=300A/μs | | 10.5 | | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial$T_J$=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

## FET1: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

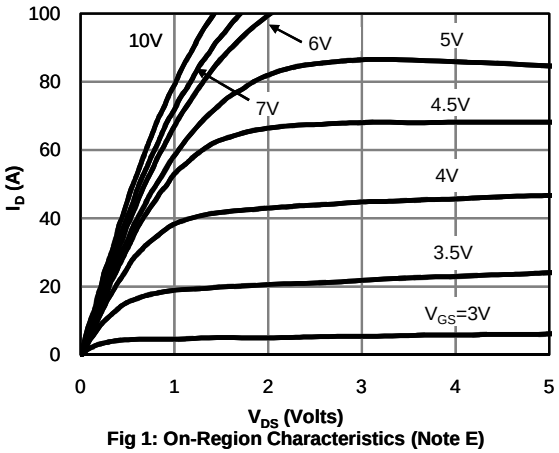



Fig 1: On-Region Characteristics (Note E)

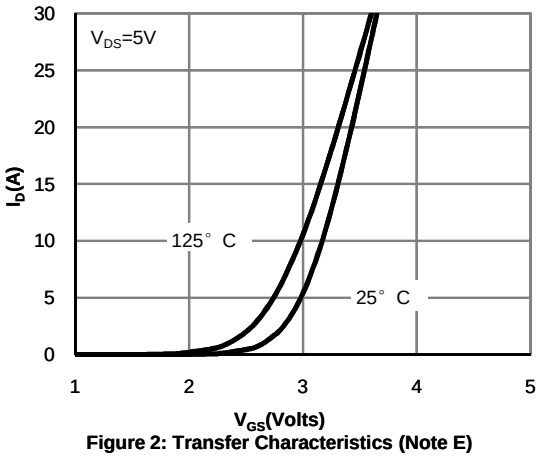



Figure 2: Transfer Characteristics (Note E)

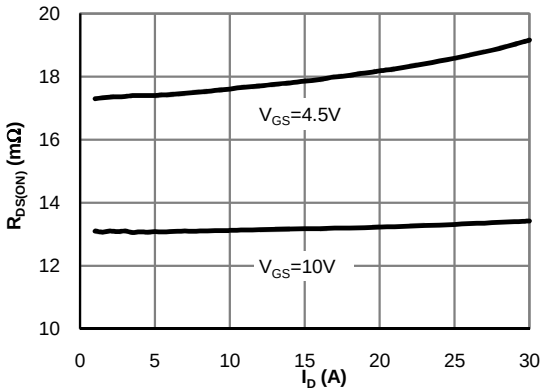



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

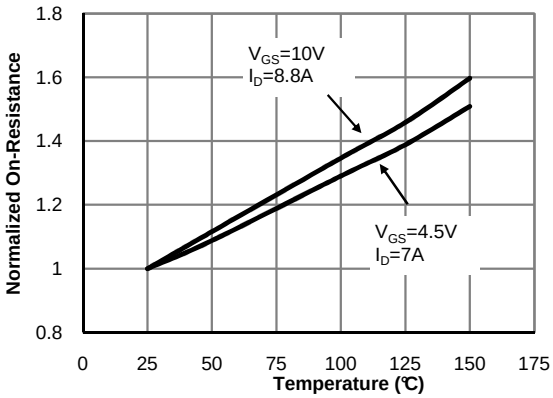



Figure 4: On-Resistance vs. Junction Temperature (Note E)

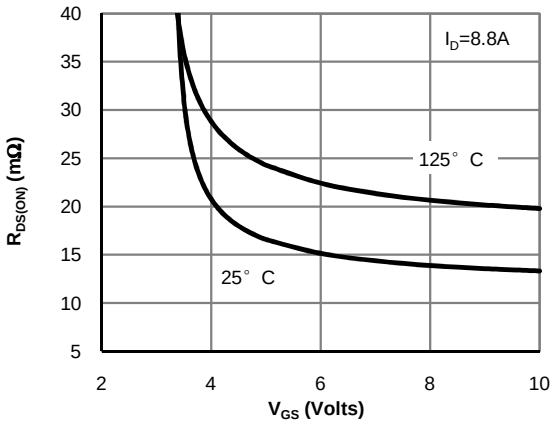



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

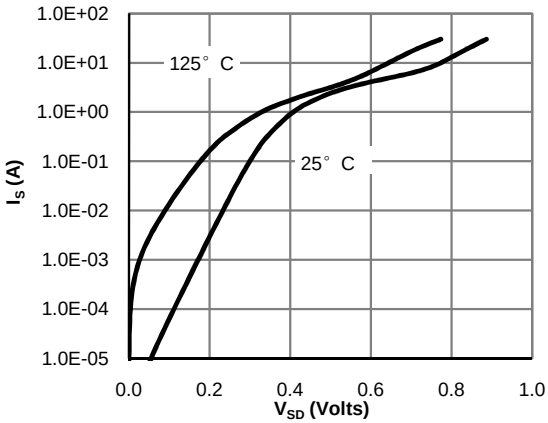



Figure 6: Body-Diode Characteristics (Note E)

## FET1: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

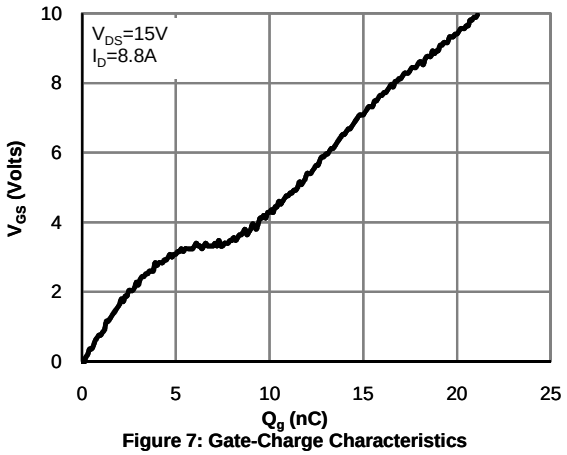



Figure 7: Gate-Charge Characteristics

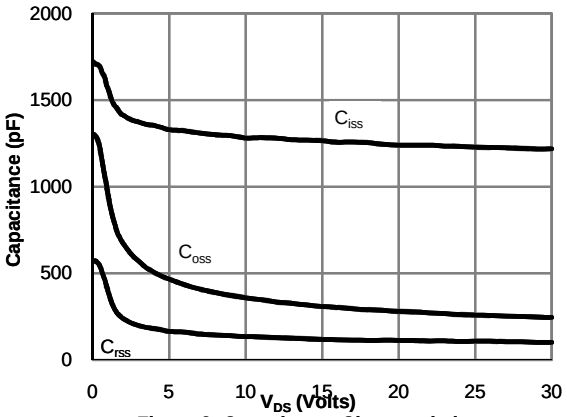



Figure 8: Capacitance Characteristics

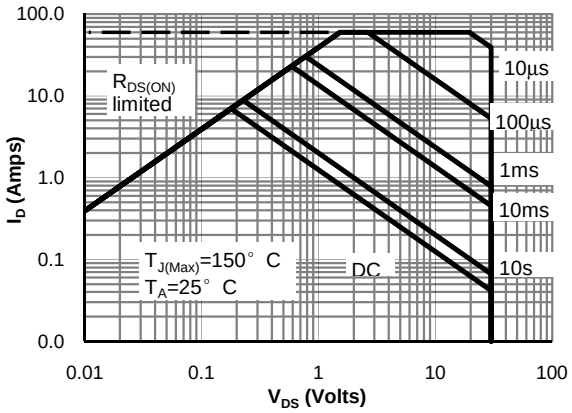



Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

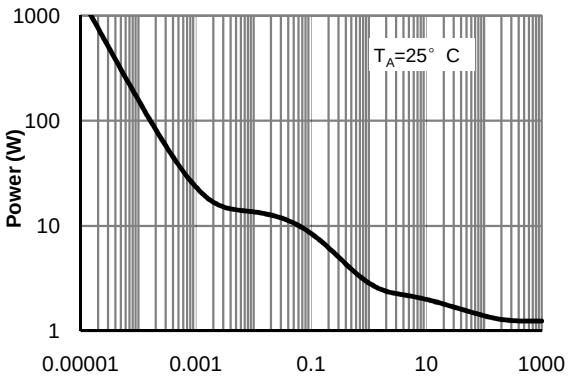



Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

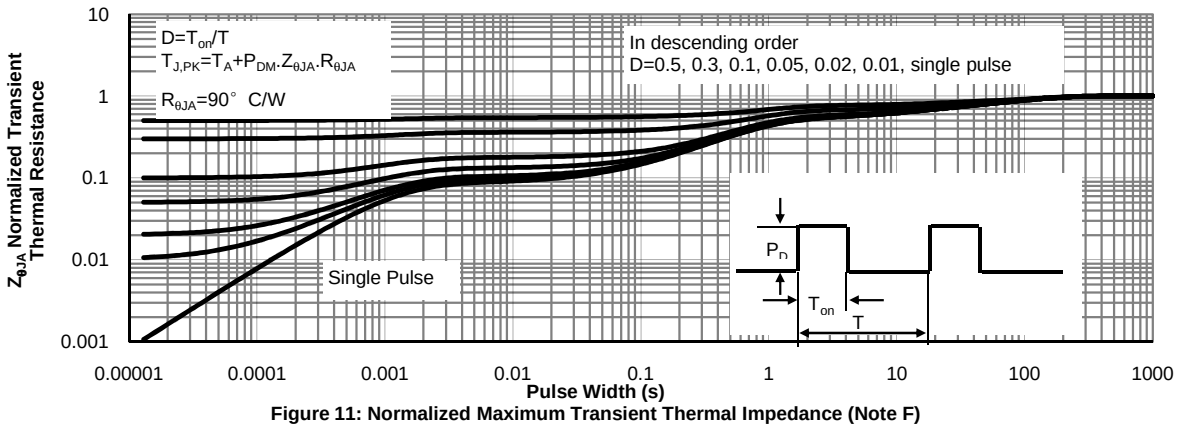



Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

**FET2 Electrical Characteristics ($T_J$=25℃ unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=250µA, $V_{GS}$=0V | 30 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=30V, $V_{GS}$=0V | | | 1 | µA |
| | | $T_J$=55℃ | | | 5 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$= ±16V | | | 10 | µA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ $I_D$=250µA | 1.2 | 1.8 | 2.4 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=10V, $V_{DS}$=5V | 40 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=10V, $I_D$=8A | | 15.5 | 19 | mΩ |
| | | $T_J$=125℃ | | 21 | 25 | |
| | | $V_{GS}$=4.5V, $I_D$=4A | | 18.6 | 28 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=8A | | 30 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=1A,$V_{GS}$=0V | | 0.75 | 1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | 2.5 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=15V, f=1MHz | 600 | 740 | 888 | pF |
| $C_{oss}$ | Output Capacitance | | 77 | 110 | 145 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | 50 | 82 | 115 | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | 0.5 | 1.1 | 1.7 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$=10V, $V_{DS}$=15V, $I_D$=8A | 12 | 15 | 18 | nC |
| $Q_g$(4.5V) | Total Gate Charge | | 6 | 7.5 | 9 | nC |
| $Q_{gs}$ | Gate Source Charge | | 2 | 2.5 | 3 | nC |
| $Q_{gd}$ | Gate Drain Charge | | 2 | 3 | 5 | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=15V, $R_L$=1.8Ω, $R_{GEN}$=3Ω | | 5 | | ns |
| $t_r$ | Turn-On Rise Time | | | 3.5 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 19 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 3.5 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=8A, dI/dt=500A/µs | 6 | 8 | 10 | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=8A, dI/dt=500A/µs | 14 | 18 | 22 | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial$T_J$=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

## FET2: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

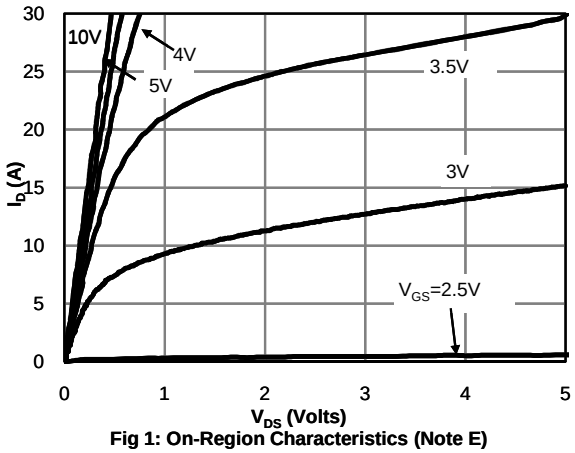



Fig 1: On-Region Characteristics (Note E)

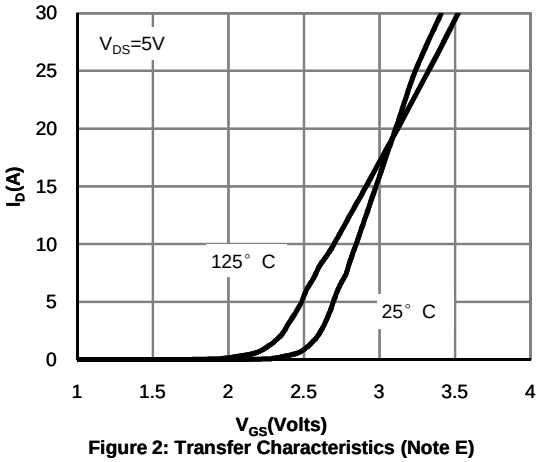



Figure 2: Transfer Characteristics (Note E)

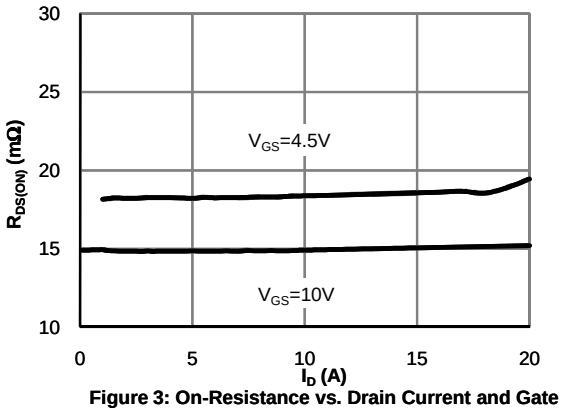



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

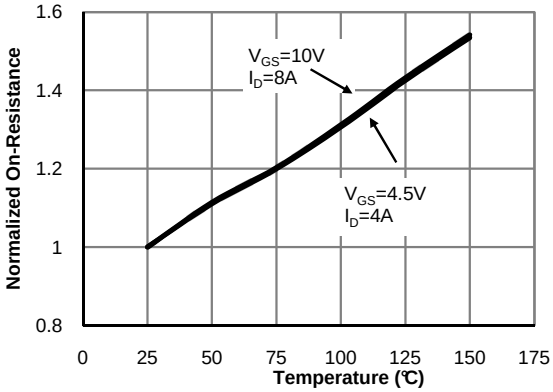



Figure 4: On-Resistance vs. Junction Temperature (Note E)

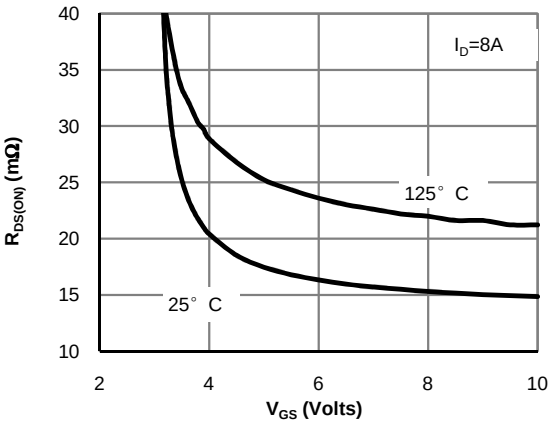



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

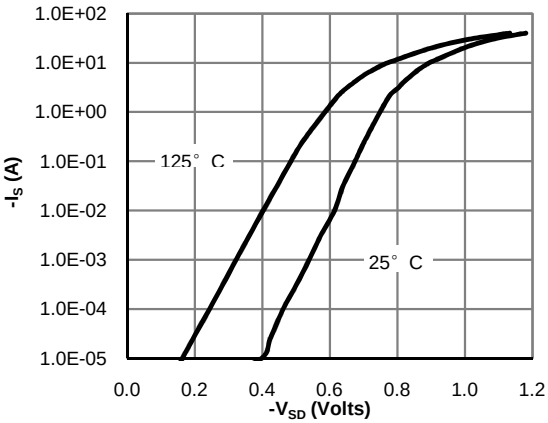



Figure 6: Body-Diode Characteristics (Note E)

## FET2: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

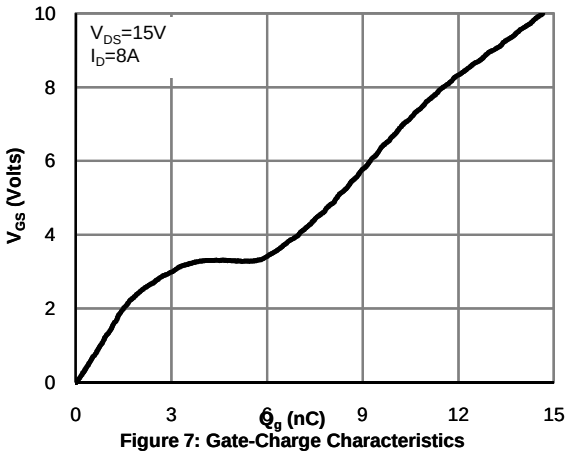



Figure 7: Gate-Charge Characteristics

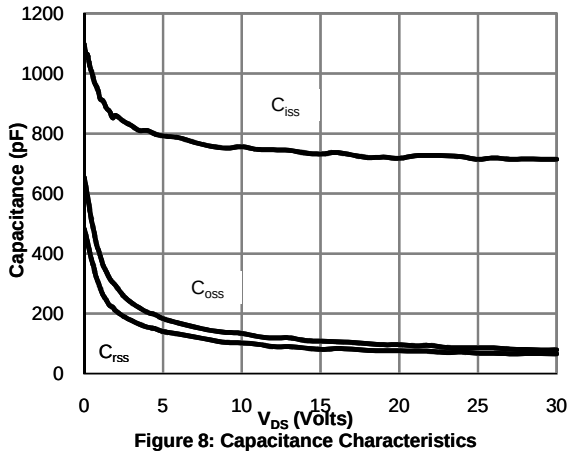



Figure 8: Capacitance Characteristics

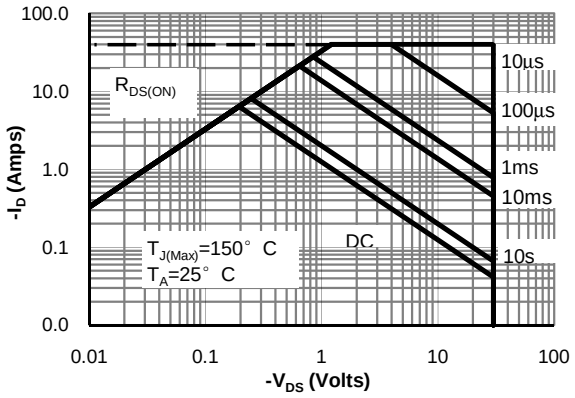



Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

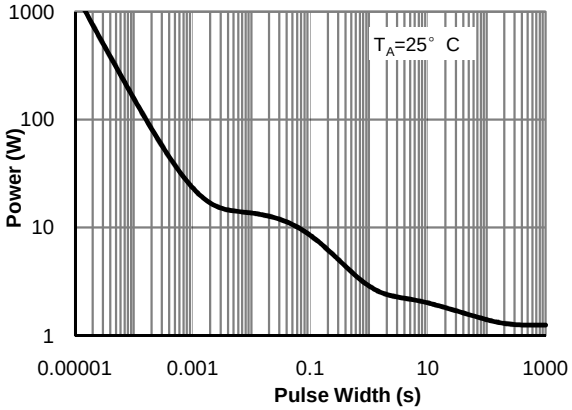



Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

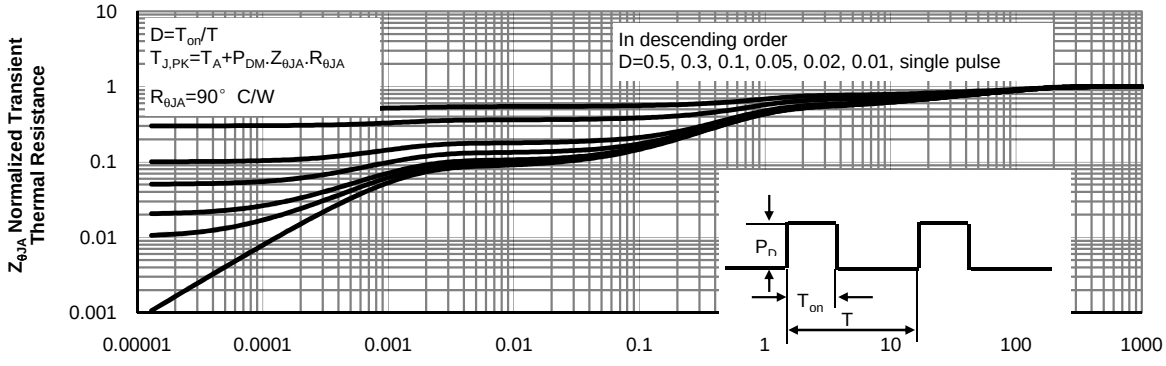
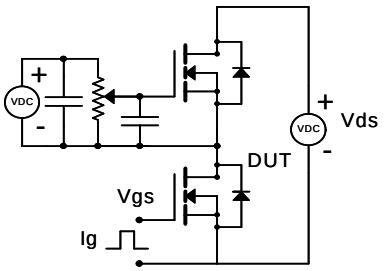
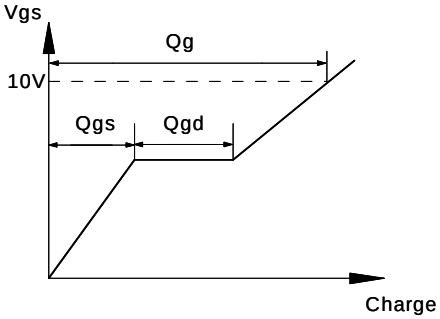


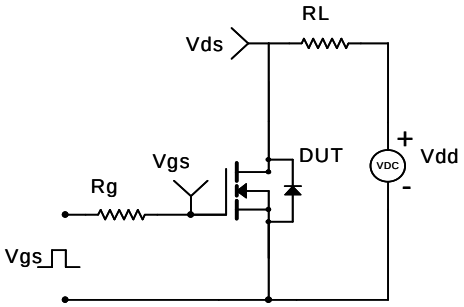

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

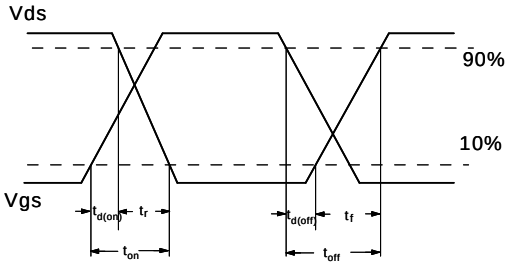
Gate Charge Test Circuit & Waveform



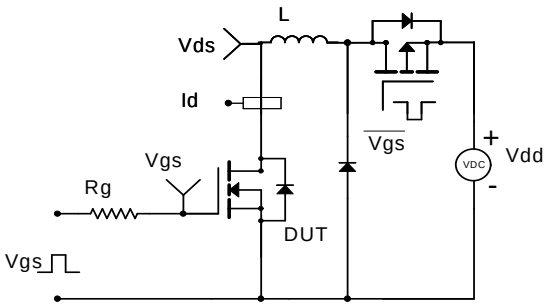



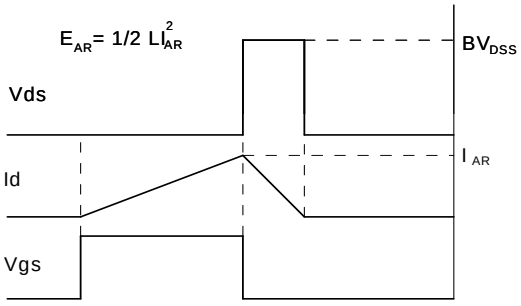

Resistive Switching Test Circuit & Waveforms




Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




Diode Recovery Test Circuit & Waveforms