AO6804A

20V Dual P-Channel MOSFET

General Description

The AO6804A uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch applications.

Product Summary

V_{DS} = 20V

I_D = 5.0A (V_{GS} = 4.5V)

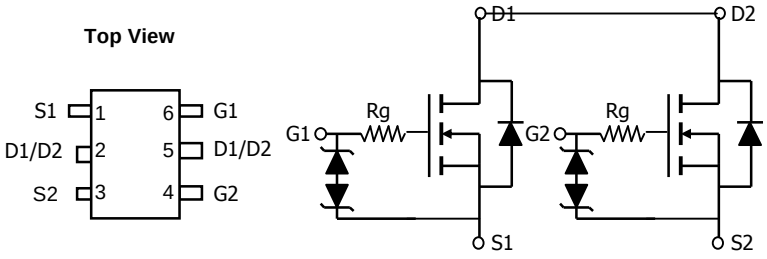
$R_{DS(ON)}$ < 28mΩ (V_{GS} = 4.5V)

$R_{DS(ON)}$ < 30mΩ (V_{GS} = 4.0V)

$R_{DS(ON)}$ < 34mΩ (V_{GS} = 3.1V)

$R_{DS(ON)}$ < 39mΩ (V_{GS} = 2.5V)

Green Product



Absolute Maximum Ratings T_A=25℃ unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current [A]	T_A=25℃	I_D	5	A
	T_A=70℃		4	
Pulsed Drain Current [B]		I_{DM}	25	
Power Dissipation [A]	T_A=25℃	P_D	1.3	W
	T_A=70℃		0.8	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	76	95	℃/W
Maximum Junction-to-Ambient [A]	Steady State		118	150	℃/W
Maximum Junction-to-Lead [C]	Steady State	$R_{\theta JL}$	54	68	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20V, V_{GS} = 0V			1	μA
		T_J = 55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS} = 0V, V_{GS} = ±10V			±10	υA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250μA	0.5	0.7	1	V
$I_{D(ON)}$	On state drain current	V_{GS} = 4.5V, V_{DS} = 5V	25			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5V, I_D = 5.0A	18	23	28	mΩ
		T_J=125℃	26	33	40	
		V_{GS} = 4.0V, I_D = 4.5A	19	24	30	mΩ
		V_{GS} = 3.1V, I_D = 4.5A	20	27	34	mΩ
		V_{GS} = 2.5V, I_D = 4.0A	21	30	39	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D = 5.0A		18		S
V_{SD}	Diode Forward Voltage	I_S = 1A,V_{GS} = 0V		0.65	1	V
I_S	Maximum Body-Diode Continuous Current				1.3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=10V, f=1MHz		180	225	pF
C_{oss}	Output Capacitance			95		pF
C_{rss}	Reverse Transfer Capacitance			18		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		2.7	4	kΩ
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}= 4.5V, V_{DS}= 10V, I_D= 5A		5.6	7.5	nC
Q_{gs}	Gate Source Charge			0.85		nC
Q_{gd}	Gate Drain Charge			1.7		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=10V, R_L=2.0Ω, R_{GEN}=3Ω		172		ns
t_r	Turn-On Rise Time			368		ns
$t_{D(off)}$	Turn-Off DelayTime			2.94		υs
t_f	Turn-Off Fall Time			2.5		υs
t_{rr}	Body Diode Reverse Recovery Time	I_F=5A, dI/dt=100A/μs		32	43	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=5A, dI/dt=100A/μs		3.2		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25℃. in any given application depends on the user's specific board design. The current rating is based on the t ≤10s thermal resistance rating.
B: Repetitive rating, pulse width limited by junction temperature.
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
D. The static characteristics in Figures 1 to 6 are obtained using < 300μs pulses, duty cycle 0.5% max.
E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃. The SOA curve provides a single pulse rating.

Rev2: Nov. 2010

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

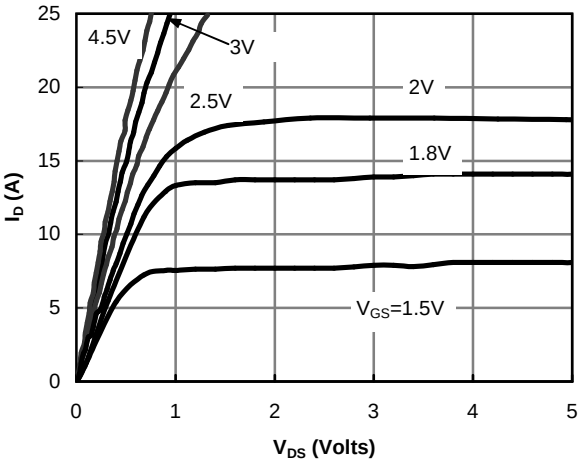


Figure 1: On-Region Characteristics

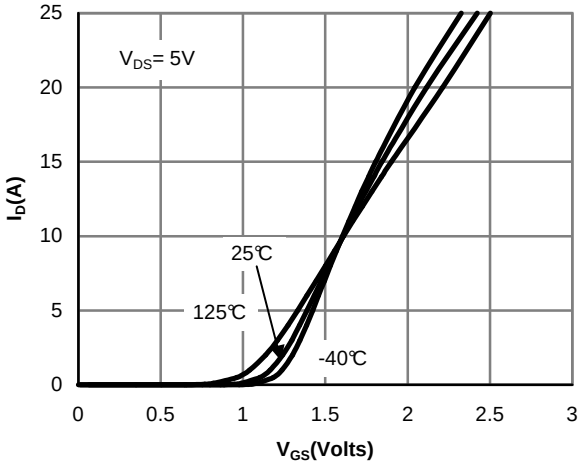


Figure 2: Transfer Characteristics

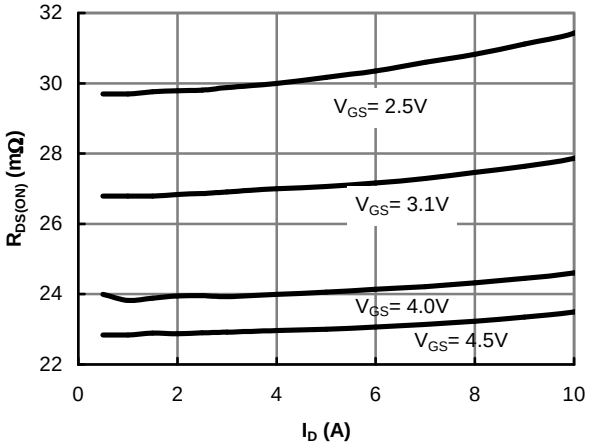


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

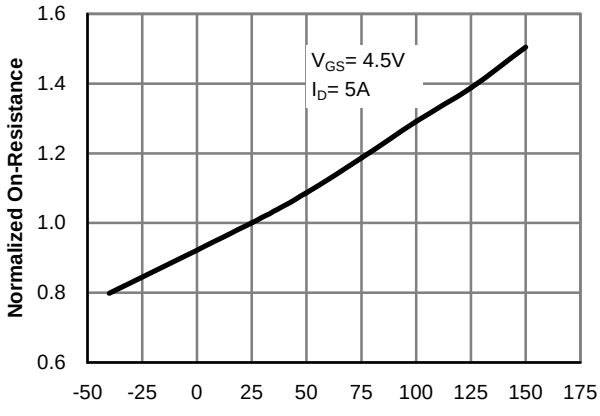


Figure 4: On-Resistance vs. Junction Temperature

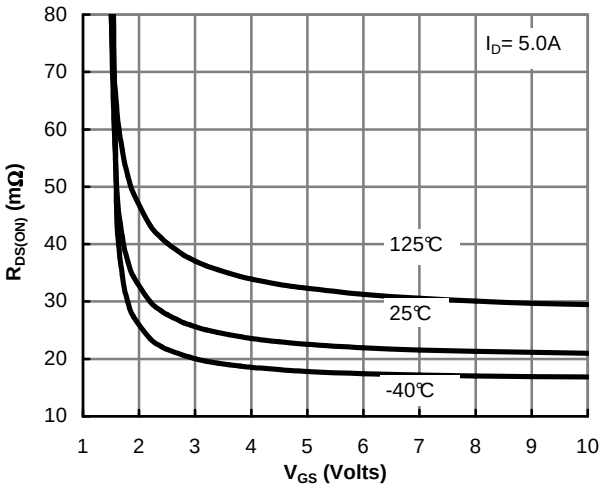


Figure 5: On-Resistance vs. Gate-Source Voltage

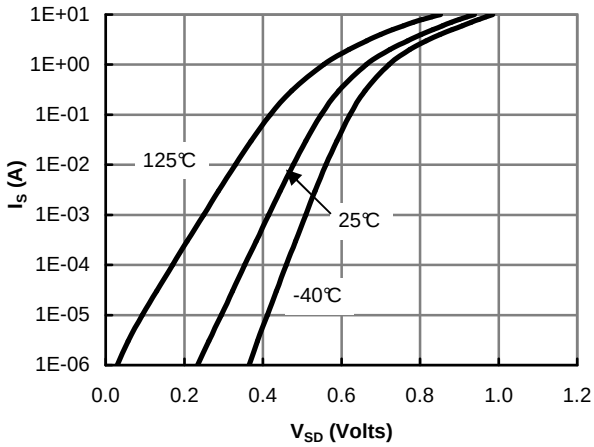


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

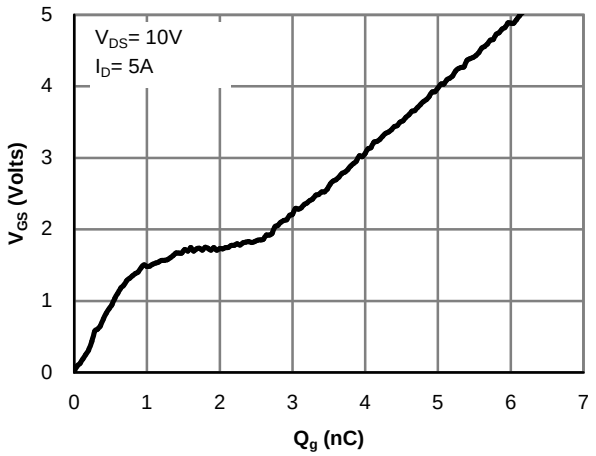


Figure 7: Gate-Charge Characteristics

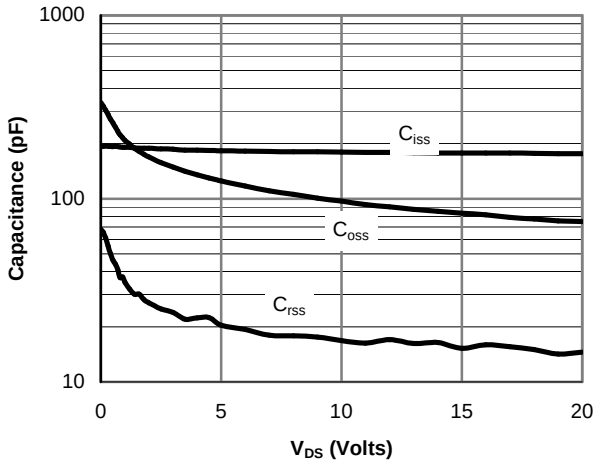


Figure 8: Capacitance Characteristics

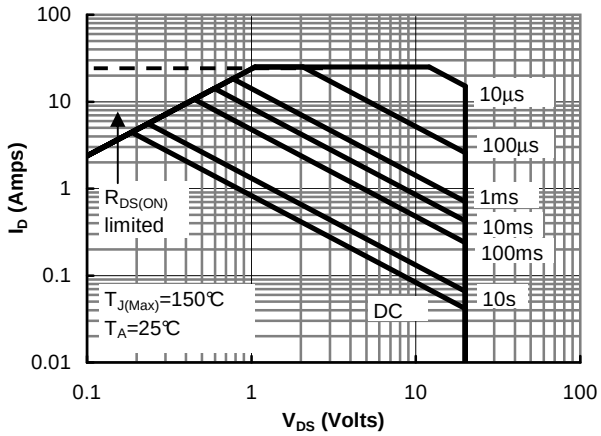


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

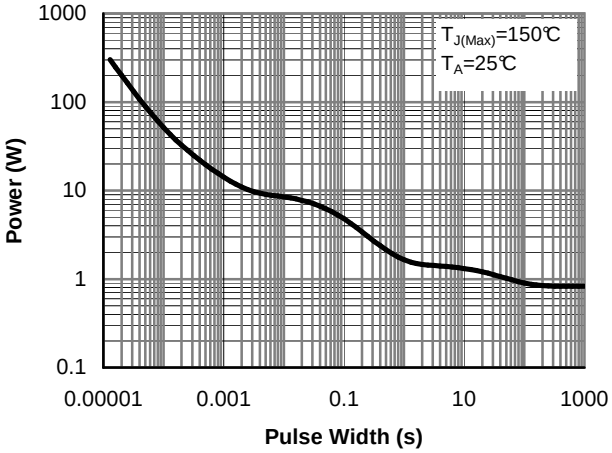


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

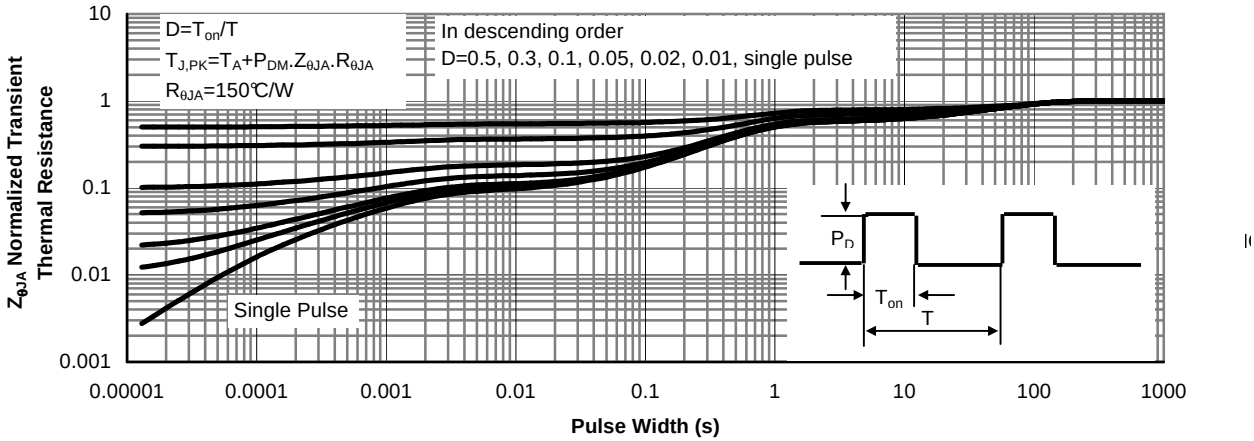
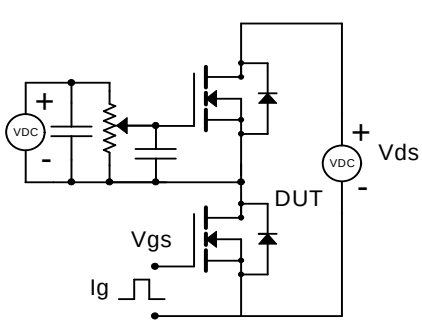
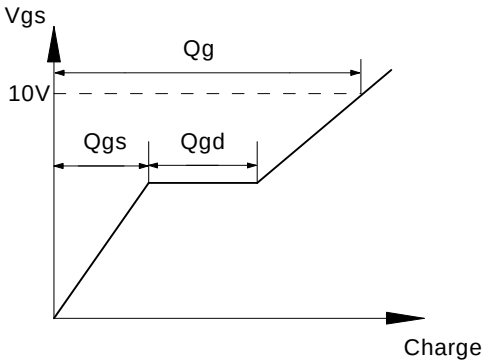


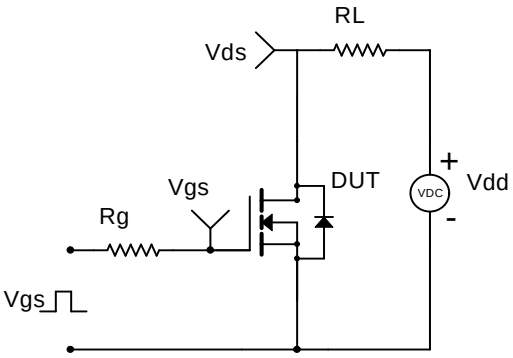
Figure 11: Normalized Maximum Transient Thermal Impedance(Note E)

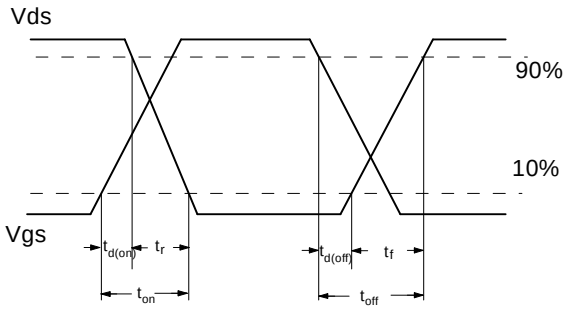
Gate Charge Test Circuit & Waveform





Resistive Switching Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms