freescale
飞思卡尔(深圳)功率半导体有限公司

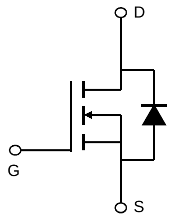
AOT240L/AOB240L/AOTF240L
40V N-Channel MOSFET

General Description

The AOT240L & AOB240L & AOTF240L uses Trench MOSFET technology that is uniquely optimized to provide the most efficient high frequency switching performance. Power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Crss.

Features

V_{DS}	40V
I_D (at V_{GS}=10V)	105A/85A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 2.9mΩ (< 2.6mΩ*)
$R_{DS(ON)}$ (at V_{GS}=4.5V)	< 3.7mΩ (< 3.5mΩ*)



Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	AOT240L/AOB240L	AOTF240L	Units
Drain-Source Voltage		V_{DS}	40		V
Gate-Source Voltage		V_{GS}	±20		V
Continuous Drain Current [G]	T_C=25℃	I_D	105	85	A
	T_C=100℃		82	60	
Pulsed Drain Current [C]		I_{DM}	400		
Continuous Drain Current	T_A=25℃	I_{DSM}	20		A
	T_A=70℃		16		
Avalanche Current [C]		I_{AS}	68		A
Avalanche energy L=0.1mH [C]		E_{AS}	231		mJ
Power Dissipation [B]	T_C=25℃	P_D	176	41	W
	T_C=100℃		88	20	
Power Dissipation [A]	T_A=25℃	P_{DSM}	1.9		W
	T_A=70℃		1.2		
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175		℃

Thermal Characteristics

Parameter		Symbol	AOT240L/AOB240L	AOTF240L	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	15	15	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		65	65	℃/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	0.85	3.6	℃/W

* Surface mount package TO263

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V		40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V				1	µA
			T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V				±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250µA		1	1.7	2.2	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V		400			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A			2.4	2.9	mΩ
		TO220/TO220F	T_J=125℃		3.7	4.7	
		V_{GS}=4.5V, I_D=20A TO220/TO220F			3	3.7	mΩ
		V_{GS}=10V, I_D=20A TO263			2.1	2.6	mΩ
		V_{GS}=4.5V, I_D=20A TO263			2.7	3.5	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A			78		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V			0.65	1	V
I_S	Maximum Body-Diode Continuous Current [G]					105	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=20V, f=1MHz			3510		pF
C_{oss}	Output Capacitance				1070		pF
C_{rss}	Reverse Transfer Capacitance				68		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.5	1	1.5	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=20V, I_D=20A			49	72	nC
Q_g(4.5V)	Total Gate Charge				22	32	nC
Q_{gs}	Gate Source Charge				9		nC
Q_{gd}	Gate Drain Charge				7		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=20V, R_L=1Ω, R_{GEN}=3Ω			11		ns
t_r	Turn-On Rise Time				10		ns
$t_{D(off)}$	Turn-Off DelayTime				38		ns
t_f	Turn-Off Fall Time				11		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/µs			21		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/µs			58		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on R $_{\theta JA}$ and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.
B. The power dissipation P_D is based on $T_{J(MAX)}$=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175° C. Ratings are based on low frequency and duty cycles to keep initial T_J =25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175° C. The SOA curve provides a single pulse rating.
G. The maximum current limited by package.
H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

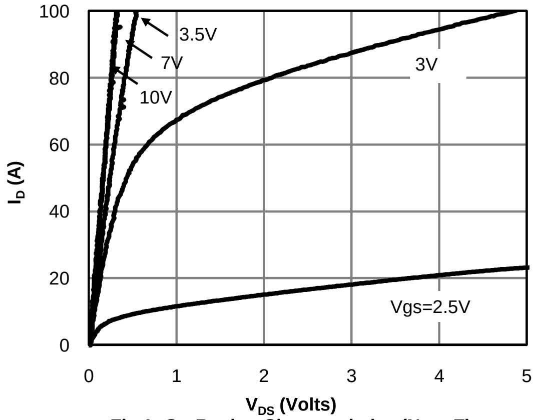


Fig 1: On-Region Characteristics (Note E)

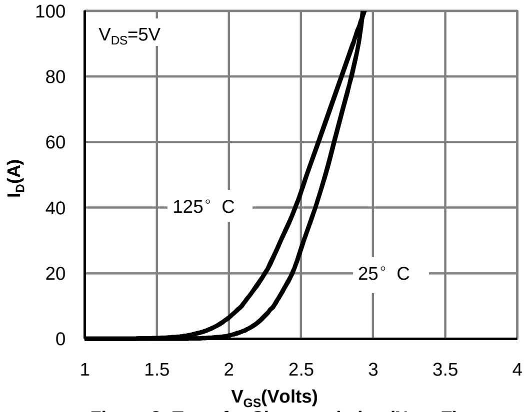


Figure 2: Transfer Characteristics (Note E)

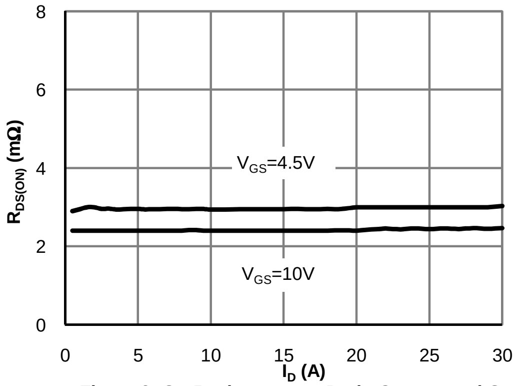


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

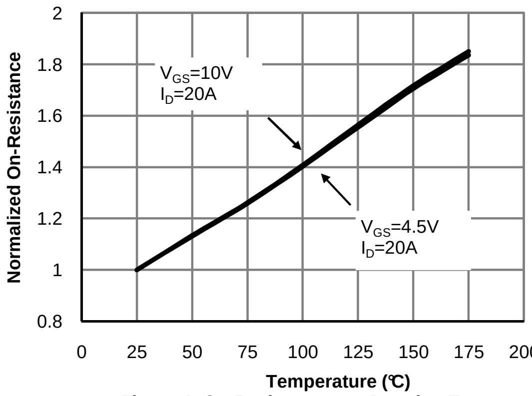


Figure 4: On-Resistance vs. Junction Temperature (Note E)

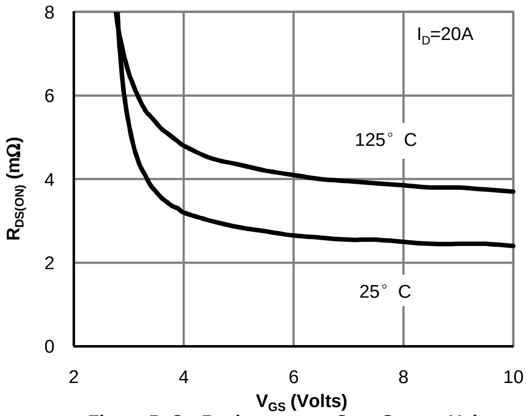


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

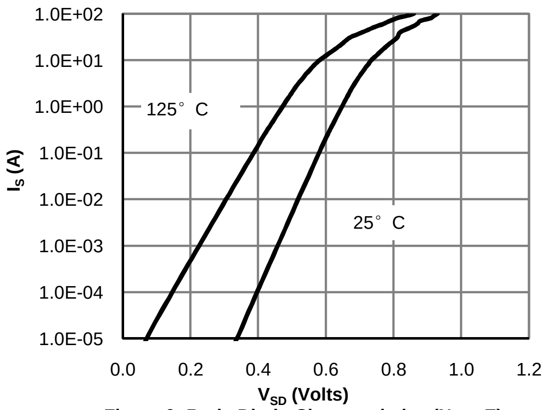


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

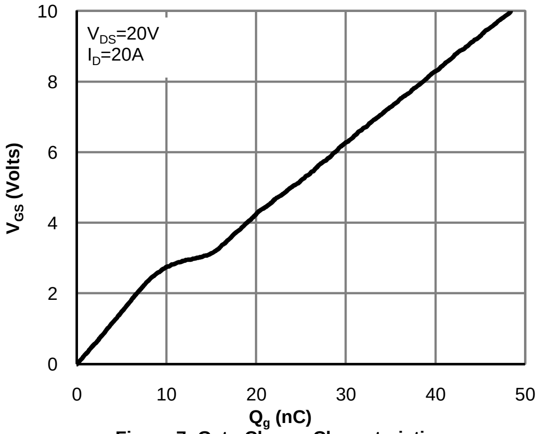


Figure 7: Gate-Charge Characteristics

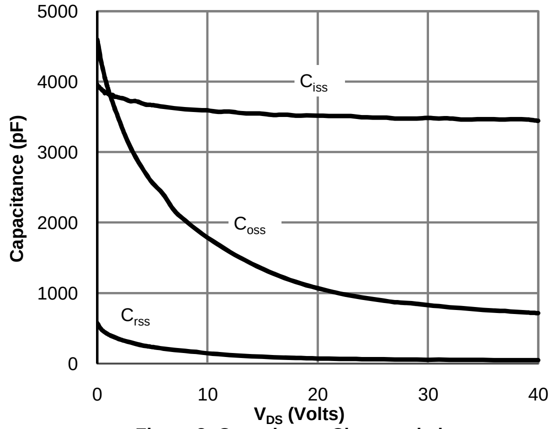


Figure 8: Capacitance Characteristics

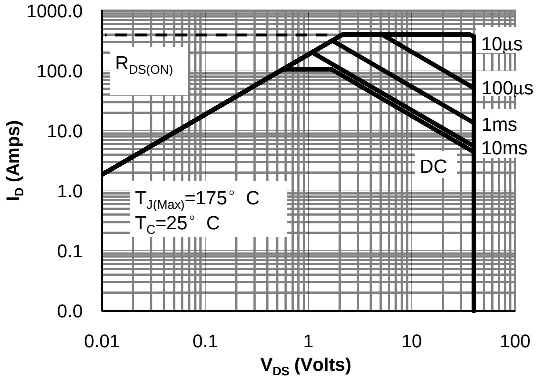


Figure 9: Maximum Forward Biased Safe Operating Area for AOT240L and AOB240L (Note F)

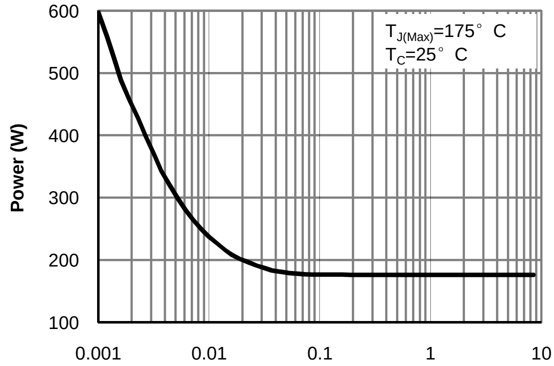


Figure 10: Single Pulse Power Rating Junction-to-Case for AOT240L and AOB240L (Note F)

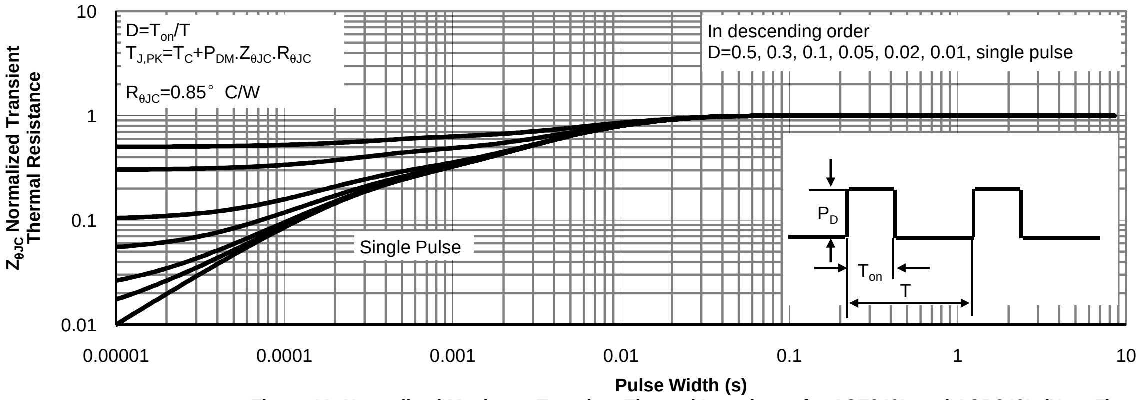


Figure 11: Normalized Maximum Transient Thermal Impedance for AOT240L and AOB240L (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

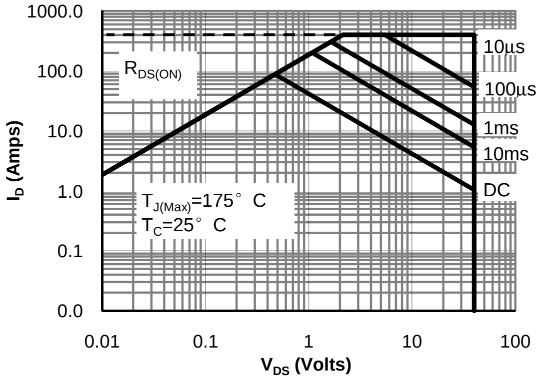


Figure 12: Maximum Forward Biased Safe Operating Area for AOTF240L

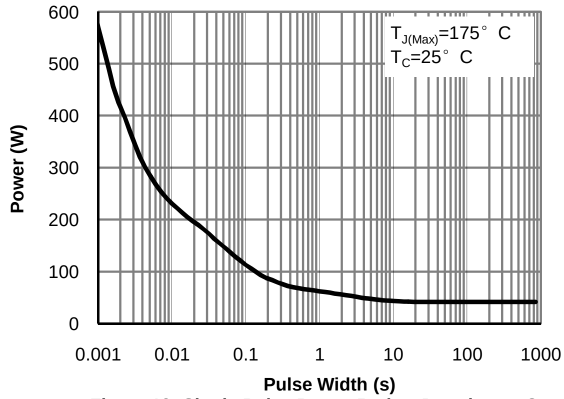


Figure 13: Single Pulse Power Rating Junction-to-Case for AOTF240L (Note F)

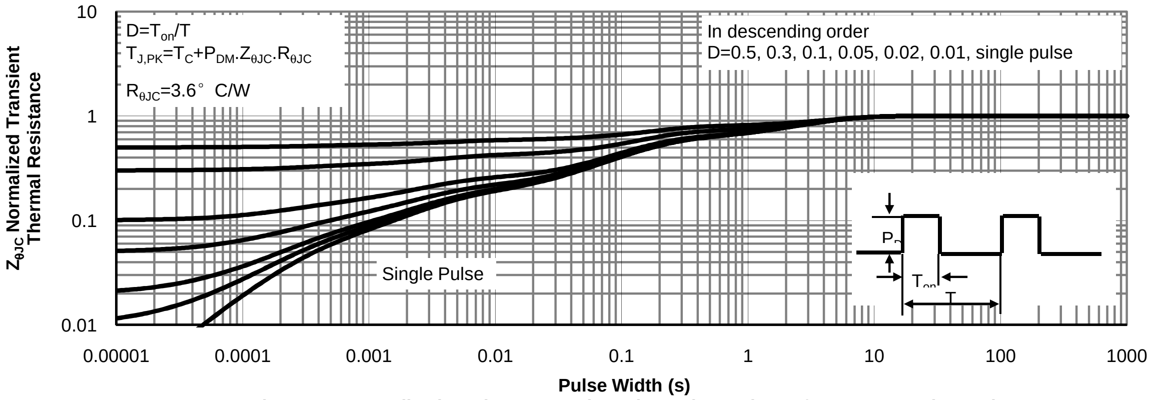


Figure 14: Normalized Maximum Transient Thermal Impedance for AOTF240L (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

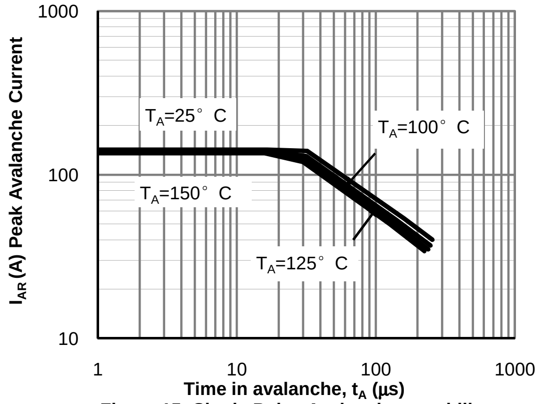


Figure 15: Single Pulse Avalanche capability (Note C)

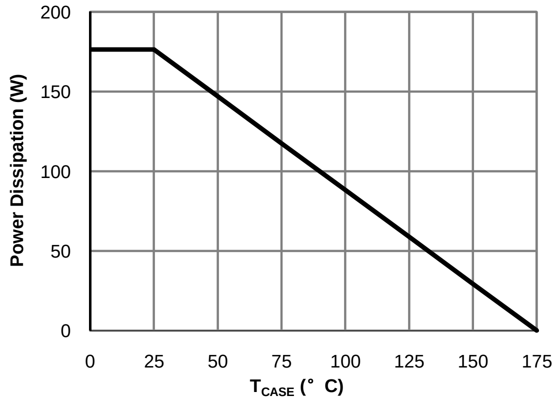


Figure 16: Power De-rating (Note F)

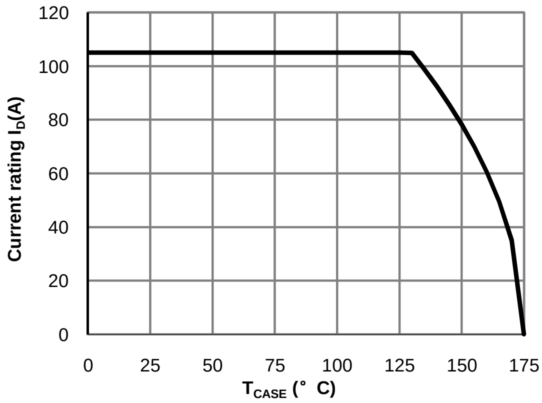


Figure 17: Current De-rating (Note F)

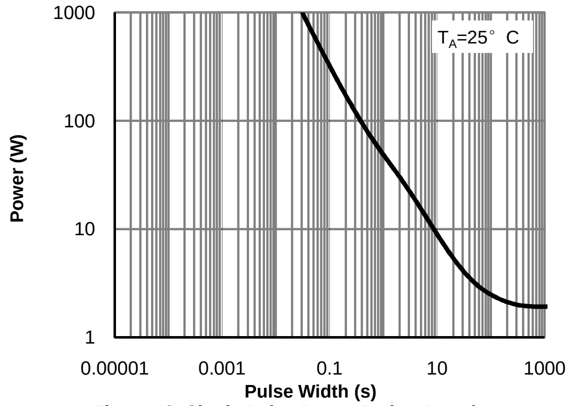


Figure 18: Single Pulse Power Rating Junction-to-Ambient (Note H)

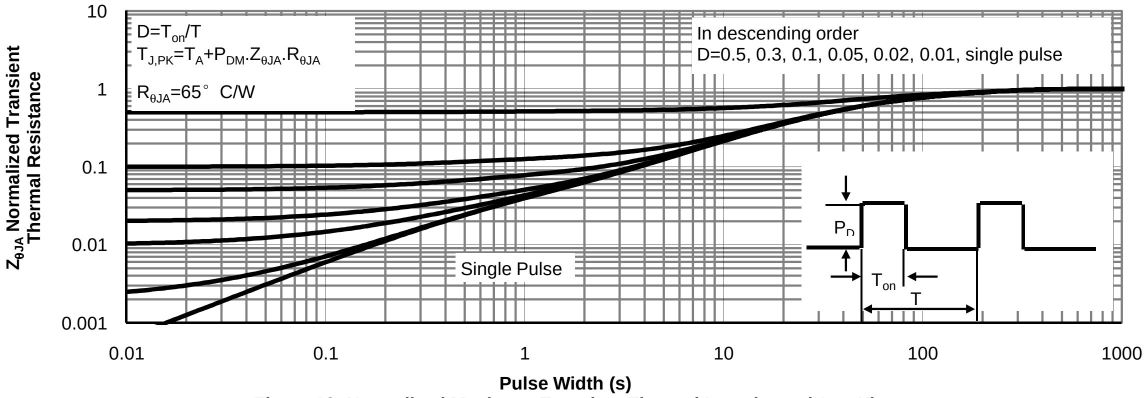
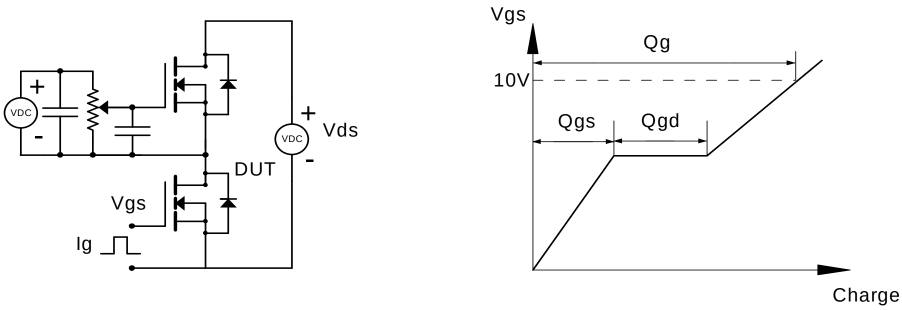
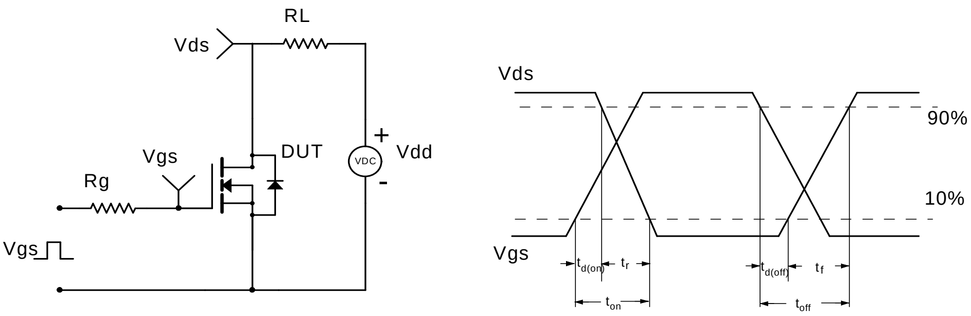


Figure 19: Normalized Maximum Transient Thermal Impedance (Note H)

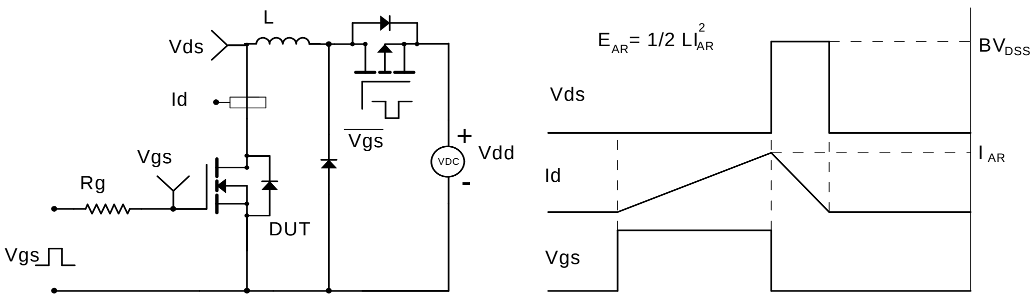
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms