

General Description

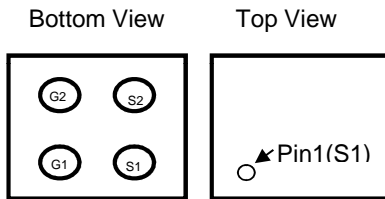
The AOC2800 uses advanced trench technology to provide excellent $R_{SS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V while retaining a 12V $V_{GS(MAX)}$ rating. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch, facilitated by its common-drain configuration.

Features

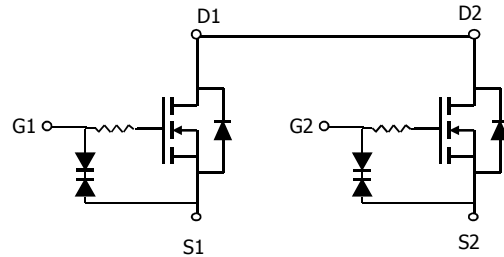
| | |
|----------------------------------|----------------|
| V_{SS} | 30V |
| I_D (at $V_{GS}=4.5V$) | 6A |
| $R_{SS(ON)}$ (at $V_{GS}=4.5V$) | < 42m Ω |
| $R_{SS(ON)}$ (at $V_{GS}=4.0V$) | < 44m Ω |
| $R_{SS(ON)}$ (at $V_{GS}=3.1V$) | < 49m Ω |
| $R_{SS(ON)}$ (at $V_{GS}=2.5V$) | < 61m Ω |



WLCSP 1.57x1.57_4



Equivalent Circuit



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

| Parameter | Symbol | Maximum | Units |
|---|---------------------------|------------|------------|
| Source-Source Voltage | V_{SS} | 30 | V |
| Gate-Source Voltage | V_{GS} | ± 12 | V |
| Source Current (DC) ^{Note1} | $T_A=25^\circ C$ I_S | 6 | A |
| Source Current (Pulse) ^{Note2} | | 60 | |
| Power Dissipation ^{Note1} | $T_A=25^\circ C$ P_D | 1.3 | W |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to 150 | $^\circ C$ |

Note 1. Mounted on minimum pad PCB

Note 2. PW <300 μs pulses, duty cycle 0.5% max

Electrical Characteristics (T_J=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|---|--|-----|-----|------|-------|
| STATIC PARAMETERS | | | | | | |
| BV _{SSS} | Source-Source Breakdown Voltage | I _S =250μA, V _{GS} =0V, Test Circuit 6 | 30 | | | V |
| I _{SSS} | Zero Gate Voltage Source Current | V _{SS} =20V, V _{GS} =0V, Test Circuit 1 | | | 1 | μA |
| | | T _J =55°C | | | 5 | |
| I _{GSS} | Gate leakage current | V _{SS} =0V, V _{GS} = ±10V, Test Circuit 2 | | 1 | 10 | |
| BV _{GSO} | Gate-Source Breakdown Voltage | V _{SS} =0V, I _G =±250μA, Test Circuit 7 | ±12 | | | V |
| V _{GS(th)} | Gate Threshold Voltage | V _{SS} =V _{GS} I _S =250μA, Test Circuit 3 | 0.5 | 1 | 1.5 | V |
| R _{SS(ON)} | Static Source to Source On-Resistance ^{Note} | V _{GS} =4.5V, I _S =3A, Test Circuit 4 | | 35 | 42 | mΩ |
| | | T _J =125°C | | 53 | 63 | |
| | | V _{GS} =4.0V, I _S =3A, Test Circuit 4 | | 37 | 44 | |
| | | V _{GS} =3.1V, I _S =3A, Test Circuit 4 | | 41 | 49 | |
| | | V _{GS} =2.5V, I _S =3A, Test Circuit 4 | | 49 | 61 | |
| g _{FS} | Forward Transconductance ^{Note} | V _{SS} =5V, I _S =3A, Test Circuit 3 | | 21 | | S |
| V _{FSS} | Diode Forward Voltage ^{Note} | I _S =1A, V _{GS} =0V, Test Circuit 5 | | 0.7 | 1 | V |
| DYNAMIC PARAMETERS | | | | | | |
| C _{iss} | Input Capacitance | V _{GS} =0V, V _{SS} =15V, f=1MHz, | | 984 | 1180 | pF |
| C _{oss} | Output Capacitance | | | 93 | | pF |
| C _{rss} | Reverse Transfer Capacitance | | | 57 | | pF |
| R _g | Gate resistance | V _{GS} =0V, V _{SS} =0V, f=1MHz | | 1.5 | | kΩ |
| SWITCHING PARAMETERS | | | | | | |
| t _{D(on)} | Turn-On DelayTime | V _{GS} =10V, V _{SS} =15V, R _L =2.4Ω, R _{GEN} =6Ω , | | 320 | | ns |
| t _r | Turn-On Rise Time | | | 800 | | ns |
| t _{D(off)} | Turn-Off DelayTime | | | 3.8 | | μs |
| t _f | Turn-Off Fall Time | | | 3.6 | | μs |
| Q _g | Total Gate Charge | V _{G1S1} =4.5V, V _{SS} =15V, I _S =6A | | 9.1 | | nC |

Note: Pulsed

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

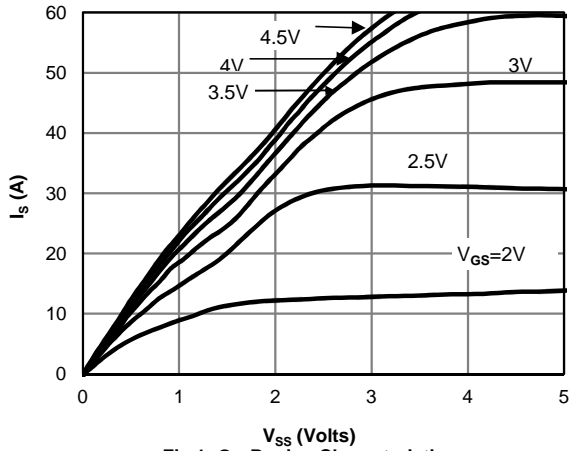


Fig 1: On-Region Characteristics

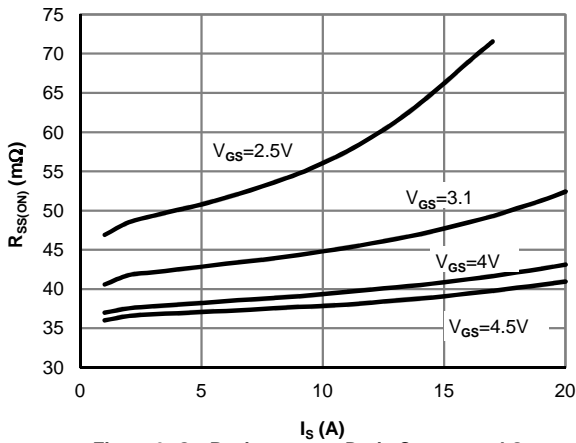
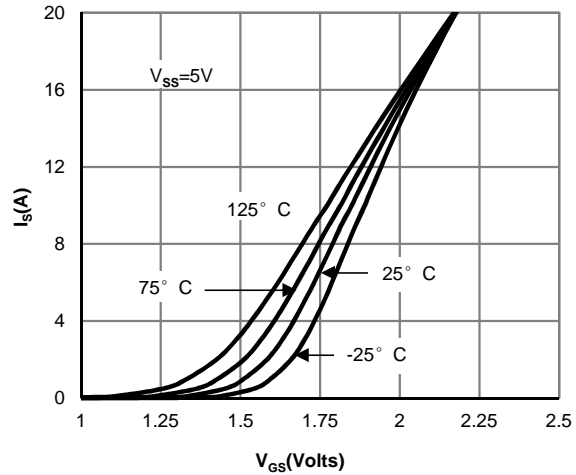


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

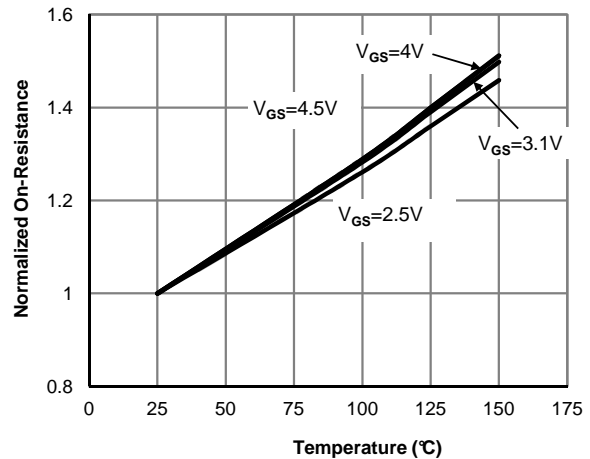


Figure 4: On-Resistance vs. Junction Temperature

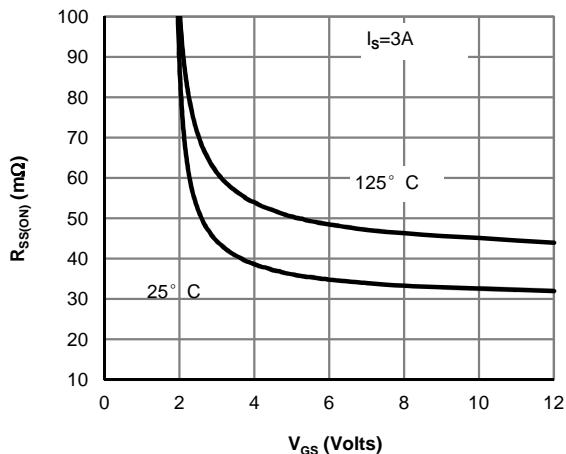


Figure 5: On-Resistance vs. Gate-Source Voltage

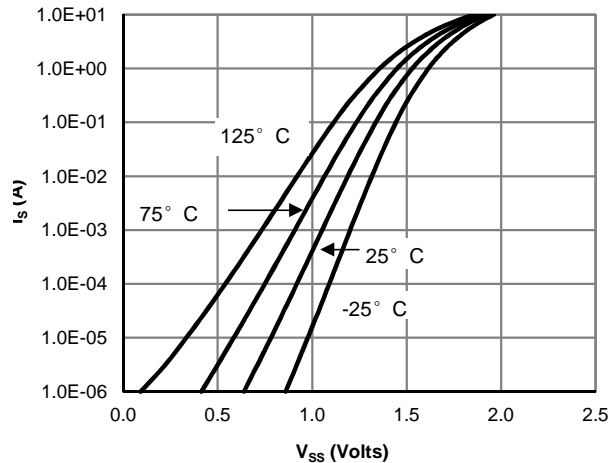


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

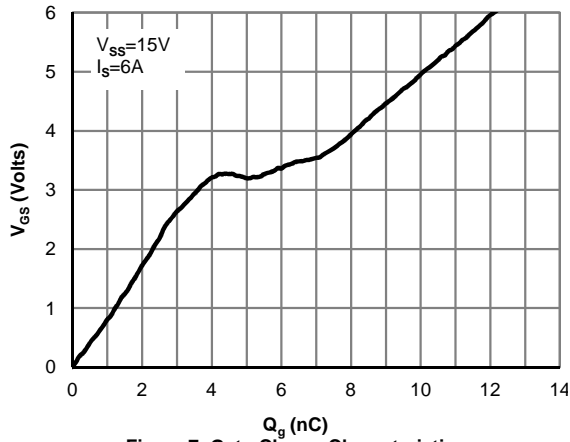


Figure 7: Gate-Charge Characteristics

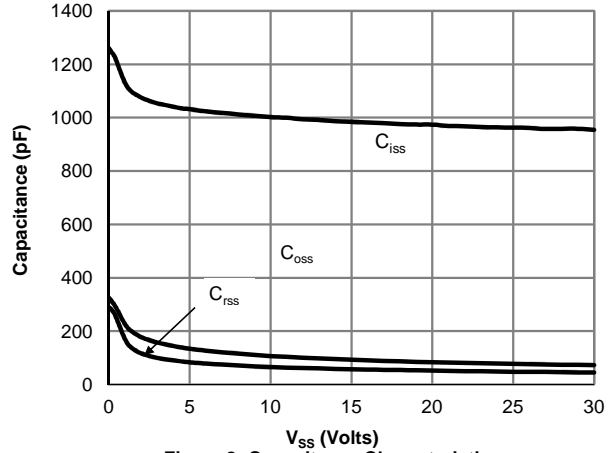


Figure 8: Capacitance Characteristics

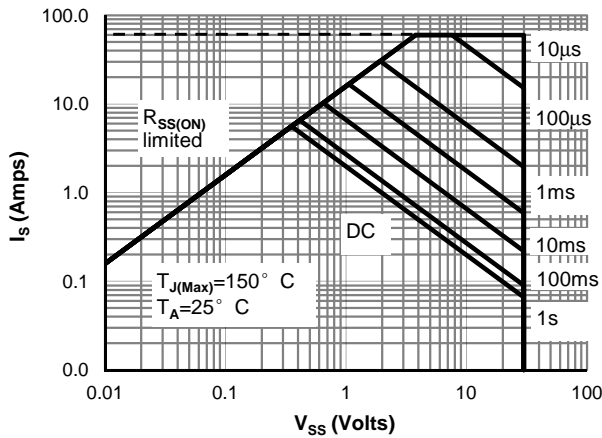


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

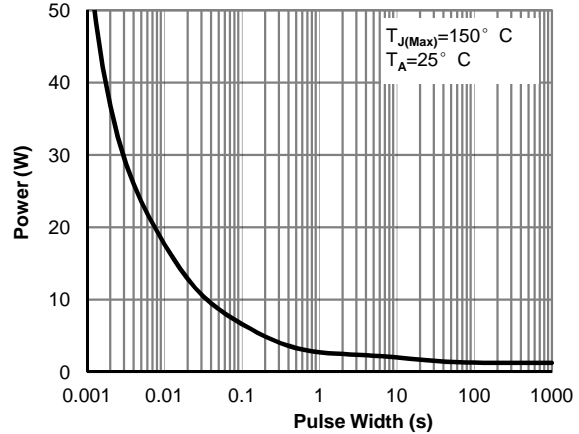


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

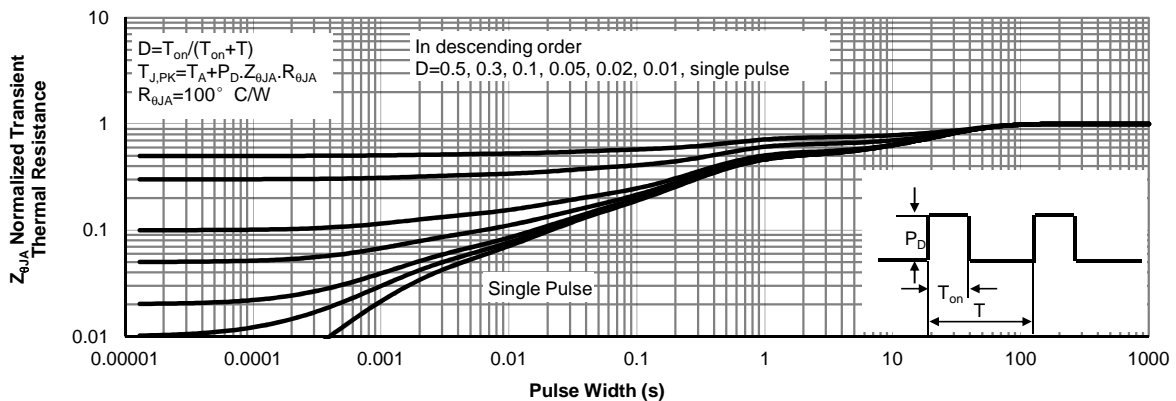
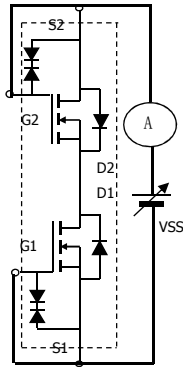


Figure 11: Normalized Maximum Transient Thermal Impedance

TEST CIRCUIT 1 I_{SSS}

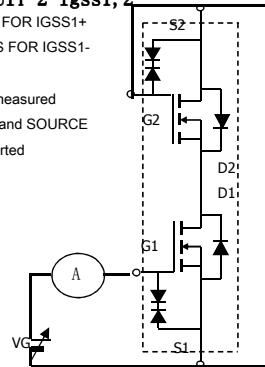
POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-



TEST CIRCUIT 2 $I_{GSS1, 2}$

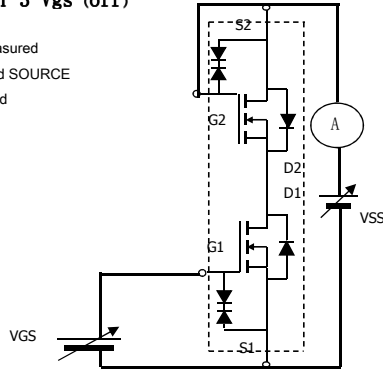
POSITIVE VGS FOR IGSS1+
NEGATIVE VGS FOR IGSS1-

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



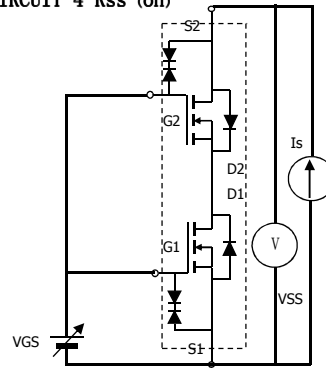
TEST CIRCUIT 3 V_{GS} (off)

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



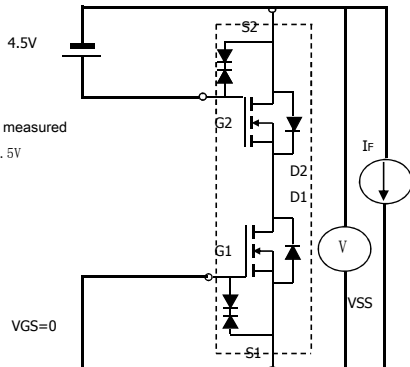
TEST CIRCUIT 4 R_{SS} (on)

VSS/Is



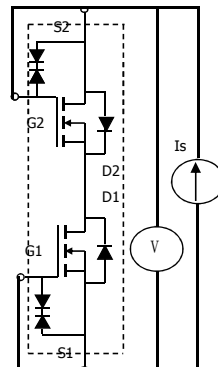
TEST CIRCUIT 5 $V_{F(SS)1, 2}$

When FET1 measured
FET2 $V_{GS}=4.5V$



TEST CIRCUIT 6 BV_{DSS}

POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-



TEST CIRCUIT 7 $BV_{GS01, 2}$

POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted

