AOD4136

N-Channel SDMOS™ POWER Transistor

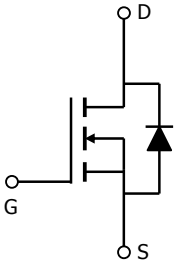
General Description

The AOD4136 is fabricated with SDMOS™ trench technology that combines excellent $R_{DS(ON)}$ with low gate charge. The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for both DC-DC and load switch applications.

Features

V_{DS} (V) = 25V
I_D = 25A (V_{GS} = 10V)
$R_{DS(ON)}$ < 11mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ <19mΩ (V_{GS} = 4.5V)

Green Product RoHS Compliant



Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	25	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [B,H]	T_C=25℃	I_D	25	A
	T_C=100℃		20	
Pulsed Drain Current [C]		I_{DM}	100	
Avalanche Current [C]		I_{AR}	17	
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	15	mJ
Power Dissipation [B]	T_C=25℃	P_D	30	W
	T_C=100℃		15	
Power Dissipation [A]	T_A=25℃	P_{DSM}	2.1	
	T_A=70℃		1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A,G]	t ≤ 10s	$R_{\theta JA}$	17.4	25	℃/W
Maximum Junction-to-Ambient [A,G]	Steady-State		50	60	℃/W
Maximum Junction-to-Case [F]	Steady-State	$R_{\theta JC}$	4	5	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	25			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=25V, V_{GS}=0V			10	µA
		T_J=55℃			100	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.5	1.9	2.5	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	100			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		9	11	mΩ
		T_J=125℃		13	16	
		V_{GS}=4.5V, I_D=15A		15	19	
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		32		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.71	1	V
I_S	Maximum Body-Diode Continuous Current				20	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=12.5V, f=1MHz		734		pF
C_{oss}	Output Capacitance			174		pF
C_{rss}	Reverse Transfer Capacitance			97		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	2.4	3.6	5.4	Ω
SWITCHING PARAMETERS						
Q_g (10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=12.5V, I_D=20A		12.9	16.8	nC
Q_g (4.5V)	Total Gate Charge			6.2	8.1	nC
Q_{gs}	Gate Source Charge			2.2		nC
Q_{gd}	Gate Drain Charge			4		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=12.5V, R_L=0.5Ω, R_{GEN}=3Ω		6		ns
t_r	Turn-On Rise Time			11.2		ns
$t_{D(off)}$	Turn-Off DelayTime			19.6		ns
t_f	Turn-Off Fall Time			9.6		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=300A/µs		12	16	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=300A/µs		11		nC

A: The value of $R_{\theta JA}$ is measured with the device in a still air environment with T_A =25℃. The power dissipation P_{DSM} and current rating I_{DSM} are based on $T_{J(MAX)}$=150℃, using t ≤ 10s junction-to-ambient thermal resistance.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175℃, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175℃.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175℃. The SOA curve provides a single pulse ratin g.

G. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃.

H. The maximum current rating is limited by bond-wires.

*This device is guaranteed green after data code 8X11 (Sep 1^{ST} 2008).

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

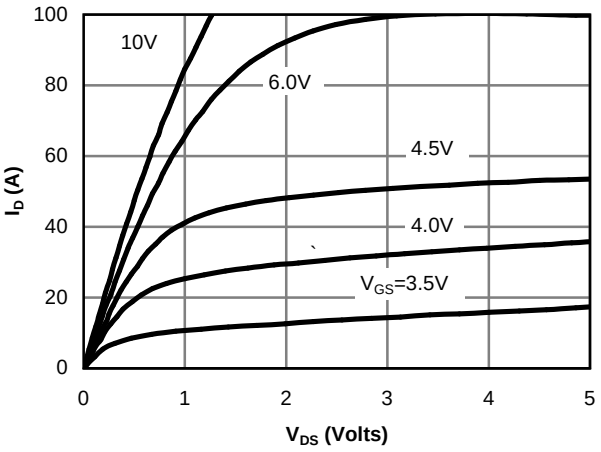


Figure 1: On-Region Characteristics

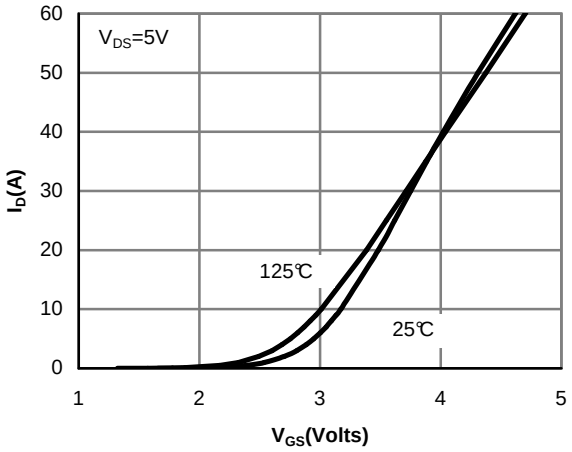


Figure 2: Transfer Characteristics

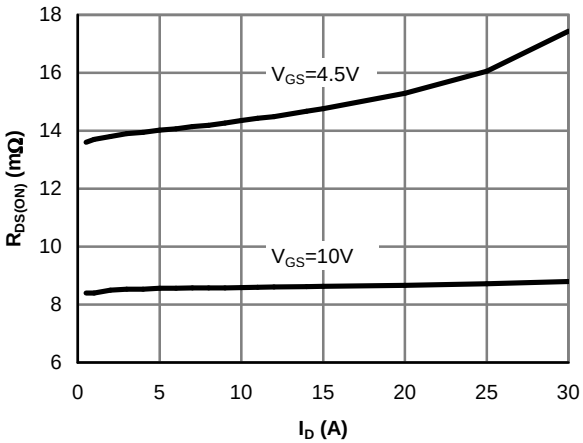


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

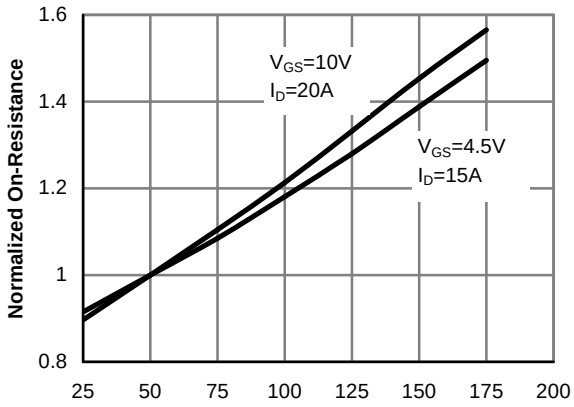


Figure 4: On-Resistance vs. Junction Temperature

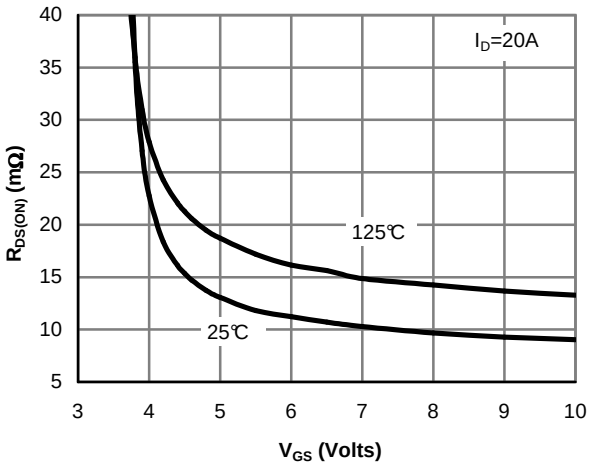


Figure 5: On-Resistance vs. Gate-Source Voltage

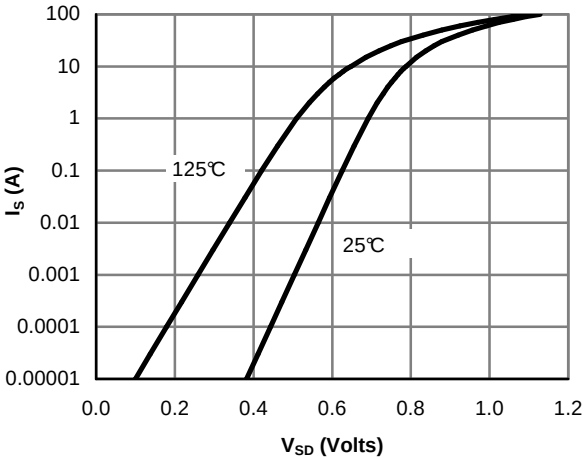


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

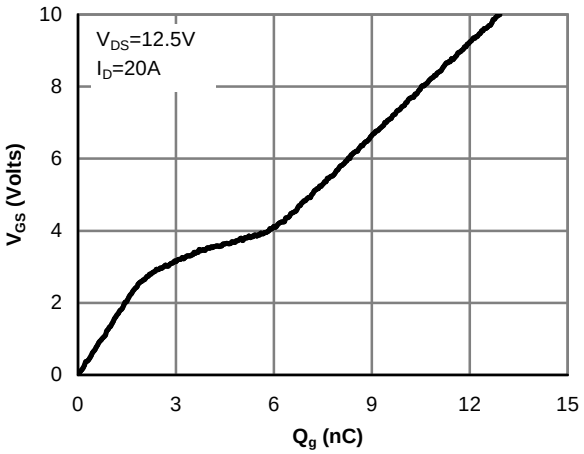


Figure 7: Gate-Charge Characteristics

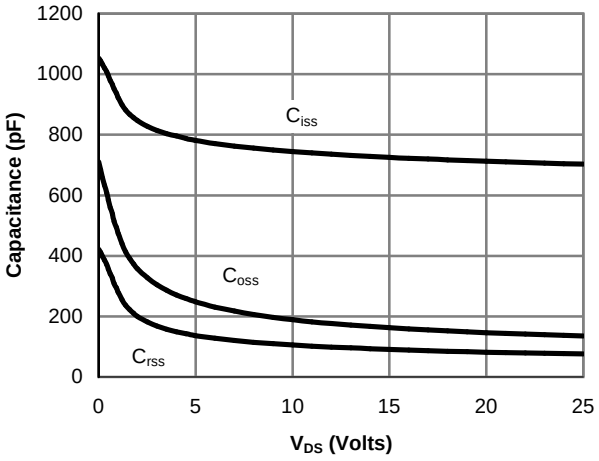


Figure 8: Capacitance Characteristics

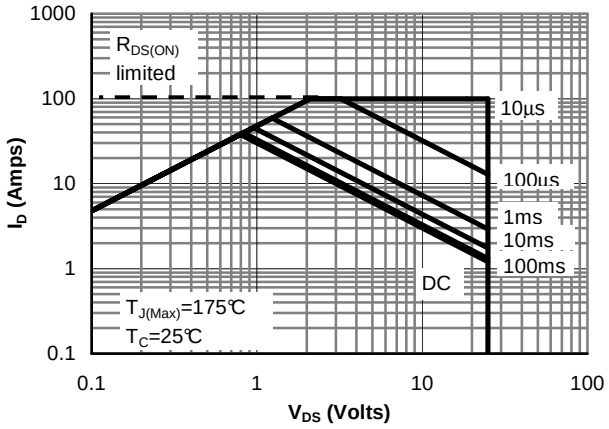


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

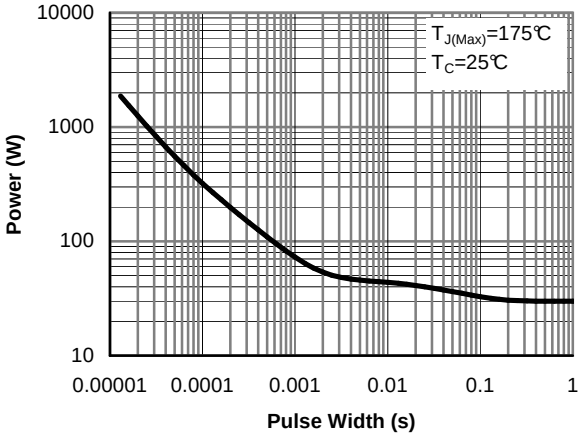


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

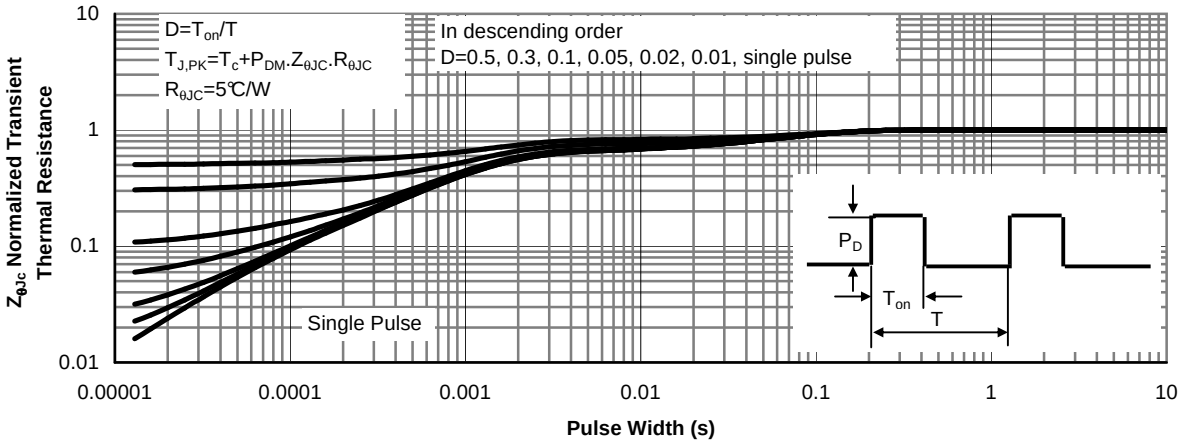


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

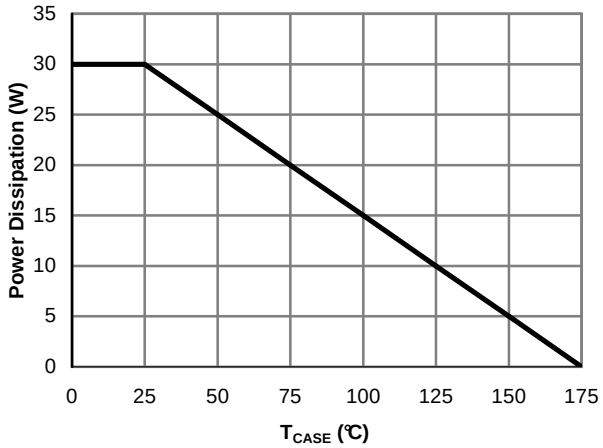


Figure 12: Power De-rating (Note B)

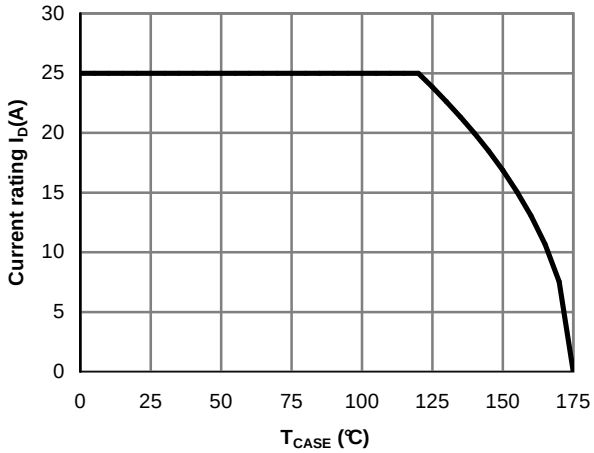


Figure 13: Current De-rating (Note B)

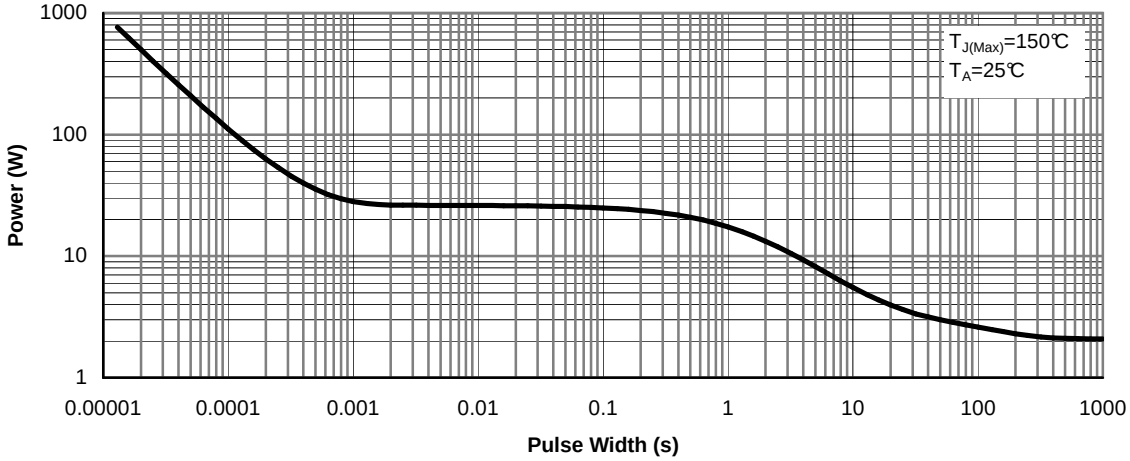


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

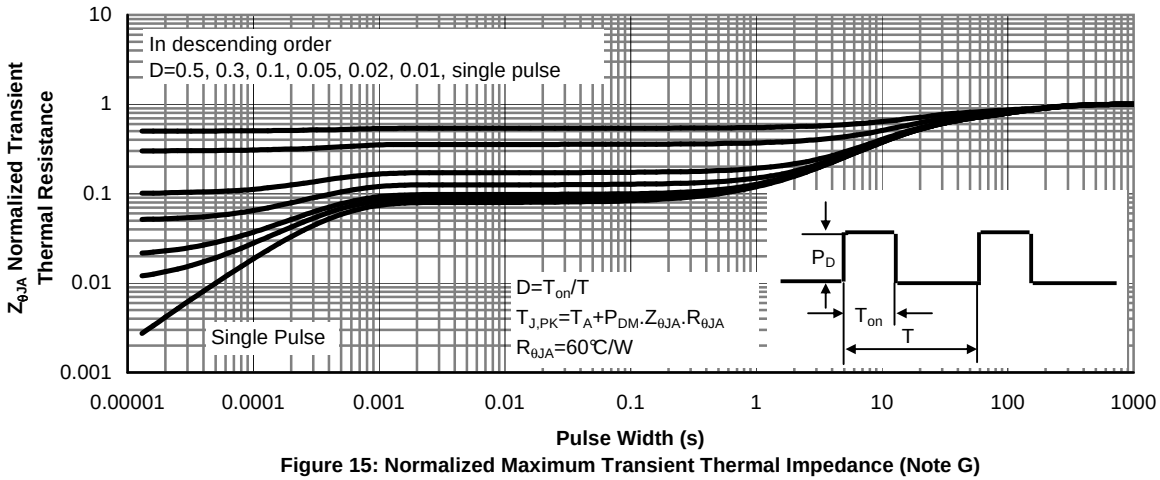
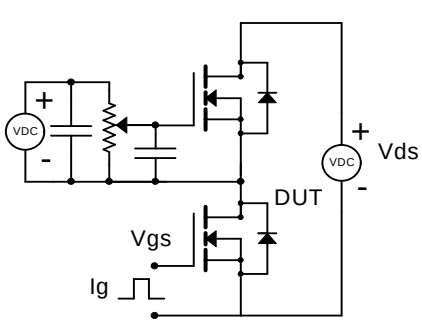
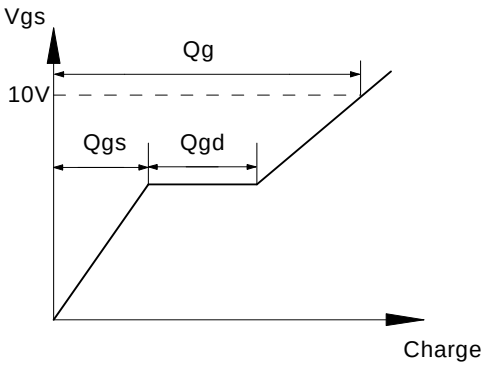


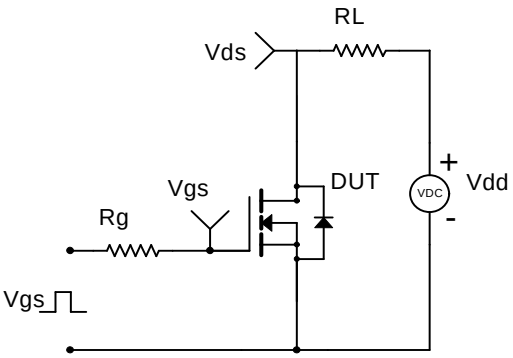
Figure 15: Normalized Maximum Transient Thermal Impedance (Note G)

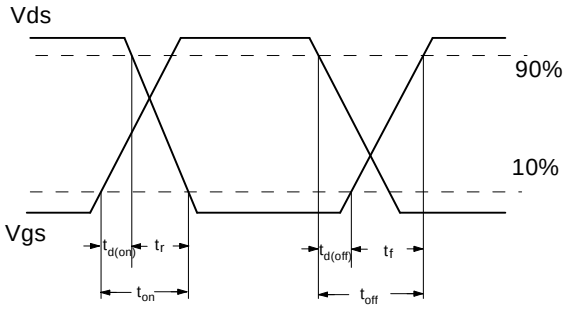
Gate Charge Test Circuit & Waveform



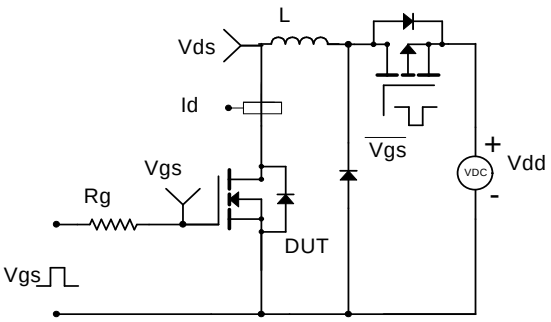


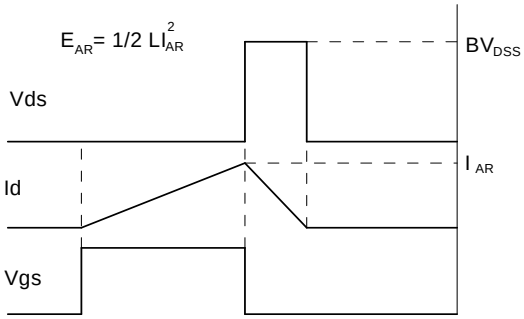
Resistive Switching Test Circuit & Waveforms





Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms