AOD417
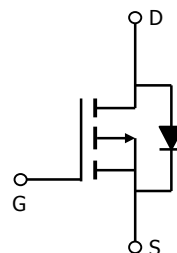P-Channel Enhancement Mode Field Effect Transistor

General Description

The AOD417 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance. With the excellent thermal resistance of the DPAK package, this device is well suited for high current load applications.

Features

V_{DS} (V) = -30V
I_D = -25A   (V_{GS} = -10V)
$R_{DS(ON)}$ < 34mΩ (V_{GS} = -10V)
$R_{DS(ON)}$ < 55mΩ (V_{GS} = -4.5V)

Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [B,G]	T_A=25℃ [G]	I_D	-25	A
	T_A=100℃		-20	
Pulsed Drain Current [C]		I_{DM}	-60	
Avalanche Current [C]		I_{AR}	-14	A
Repetitive avalanche energy L=0.3mH [C]		E_{AR}	30	mJ
Power Dissipation [B]	T_C=25℃	P_D	50	W
	T_C=100℃		25	
Power Dissipation [A]	T_A=25℃	P_{DSM}	2.5	W
	T_A=70℃		1.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{θJA}$	16.7	25	℃/W
Maximum Junction-to-Ambient [A]	Steady-State		40	50	℃/W
Maximum Junction-to-Case [D]	Steady-State	$R_{θJC}$	2.5	3	℃/W

Electrical Characteristics (T$_J$=25℃ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV$_{DSS}$	Drain-Source Breakdown Voltage	I$_D$=-250µA, V$_{GS}$=0V		-30			V
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$=-24V, V$_{GS}$=0V				-1	µA
			T$_J$=55℃			-5	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$=±20V				±100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=V$_{GS}$ I$_D$=-250µA		-1	-1.9	-3	V
I$_{D(ON)}$	On state drain current	V$_{GS}$=-10V, V$_{DS}$=-5V		-60			A
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$=-10V, I$_D$=-20A			27	34	mΩ
			T$_J$=125℃		36		
		V$_{GS}$=-4.5V, I$_D$=-7A			40	55	mΩ
g$_{FS}$	Forward Transconductance	V$_{DS}$=-5V, I$_D$=-20A			18		S
V$_{SD}$	Diode Forward Voltage	I$_S$=-1A,V$_{GS}$=0V			-0.75	-1	V
I$_S$	Maximum Body-Diode Continuous Current					-6	A
DYNAMIC PARAMETERS							
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$=-15V, f=1MHz			920		pF
C$_{oss}$	Output Capacitance				140		pF
C$_{rss}$	Reverse Transfer Capacitance				90		pF
R$_g$	Gate resistance	V$_{GS}$=0V, V$_{DS}$=0V, f=1MHz			6	9	Ω
SWITCHING PARAMETERS							
Q$_g$(10V)	Total Gate Charge (10V)	V$_{GS}$=-10V, V$_{DS}$=-15V, I$_D$=-20A			16.2		nC
Q$_g$(4.5V)	Total Gate Charge (4.5V)				8.2		nC
Q$_{gs}$	Gate Source Charge				2.9		nC
Q$_{gd}$	Gate Drain Charge				3.6		nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$=-10V, V$_{DS}$=-15V, R$_L$=0.75Ω, R$_{GEN}$=0.75Ω			8		ns
t$_r$	Turn-On Rise Time				30		ns
t$_{D(off)}$	Turn-Off DelayTime				22		ns
t$_f$	Turn-Off Fall Time				26		ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$=-20A, dI/dt=100A/µs			23		ns
Q$_{rr}$	Body Diode Reverse Recovery Charge	I$_F$=-20A, dI/dt=100A/µs			14		nC

A: The value of R$_{θ}$JA is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T$_A$ =25℃. The Power dissipation P$_{DSM}$ is based on R$_{θJA}$ (<10s) and the maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design, and the maximum temperature of 175℃ may be u sed if the PCB allows it.

B. The power dissipation P$_D$ is based on T$_{J(MAX)}$=175℃, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T$_{J(MAX)}$=175℃.

D. The R$_{θJA}$ is the sum of the thermal impedance from junction to case R$_{θJC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T$_{J(MAX)}$=175℃.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T$_A$=25℃. The SOA curve provides a single pulse rating.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev1: Sep. 2008

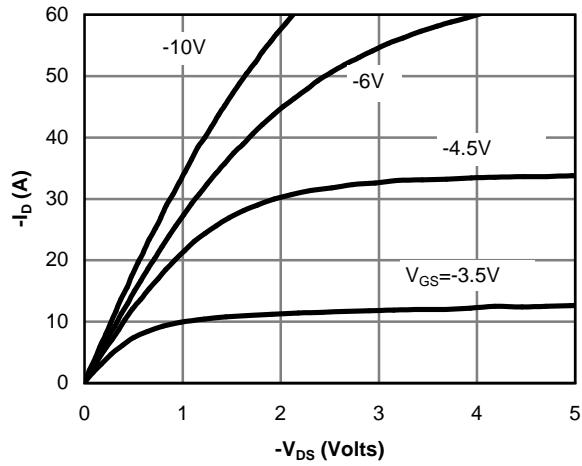## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

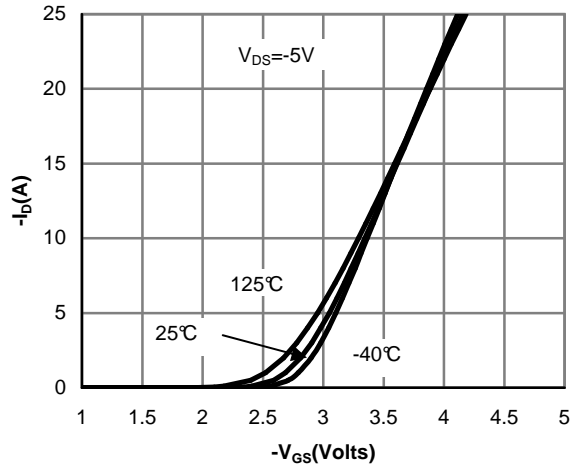Figure 1: On-Region Characteristics

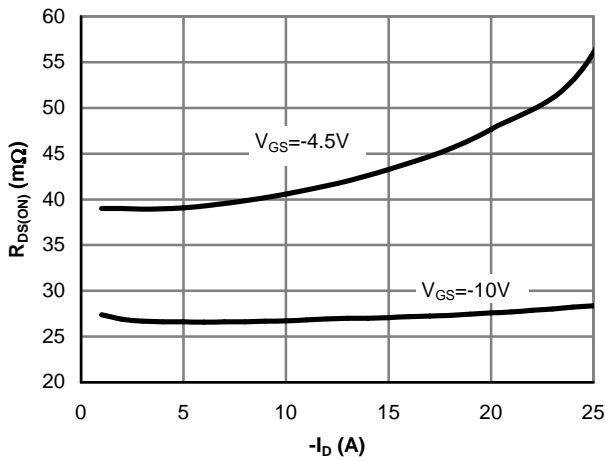Figure 2: Transfer Characteristics

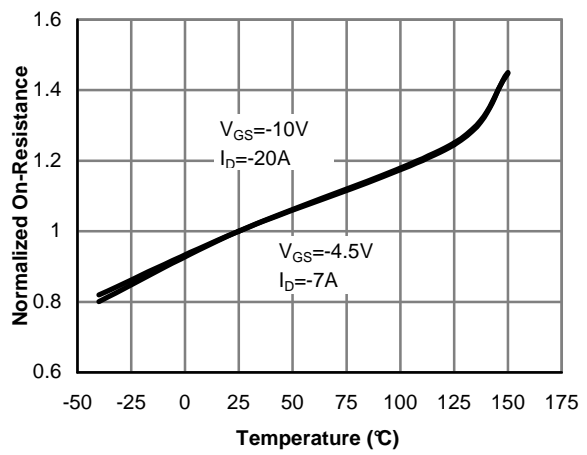Figure 3: On-Resistance vs. Drain Current and Gate Voltage

Figure 4: On-Resistance vs. Junction Temperature
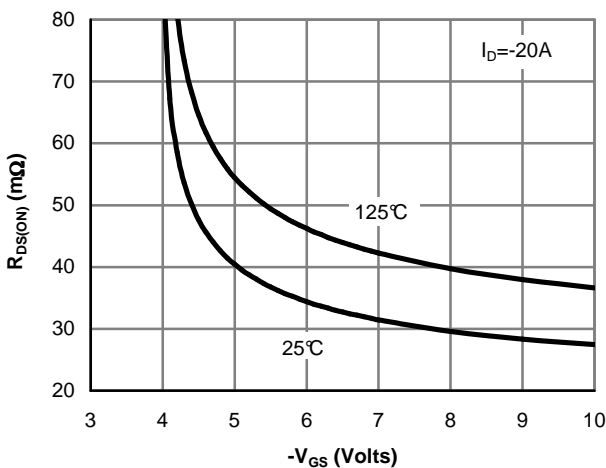

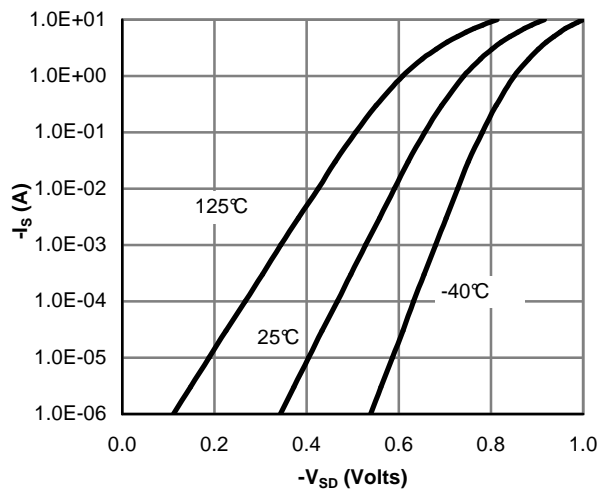Figure 5: On-Resistance vs. Gate-Source Voltage

Figure 6: Body-Diode Characteristics

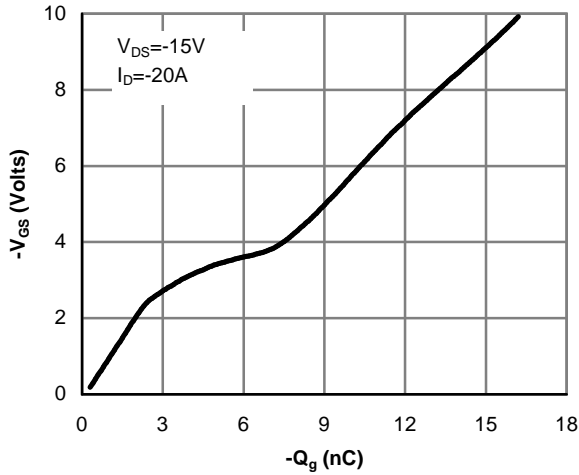## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
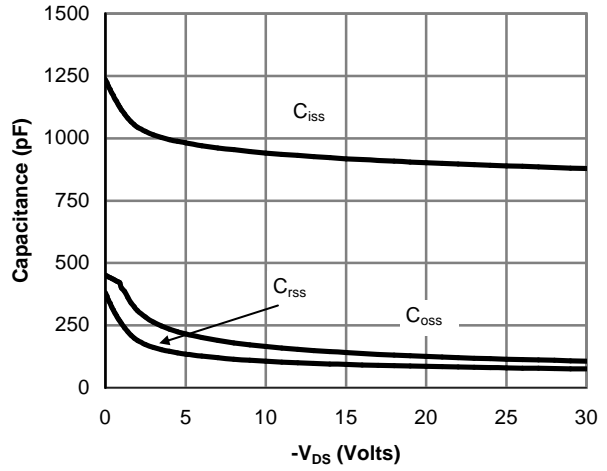

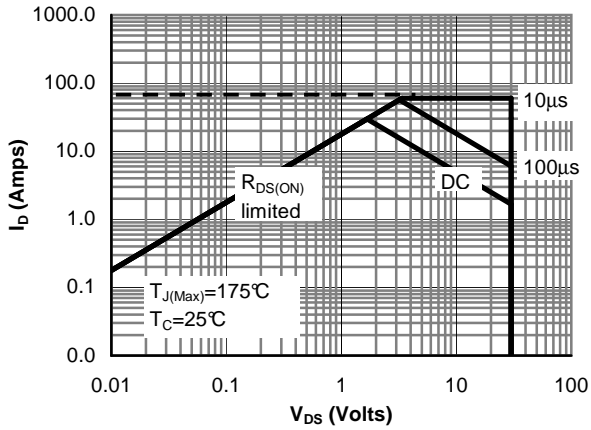Figure 7: Gate-Charge Characteristics

Figure 8: Capacitance Characteristics

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
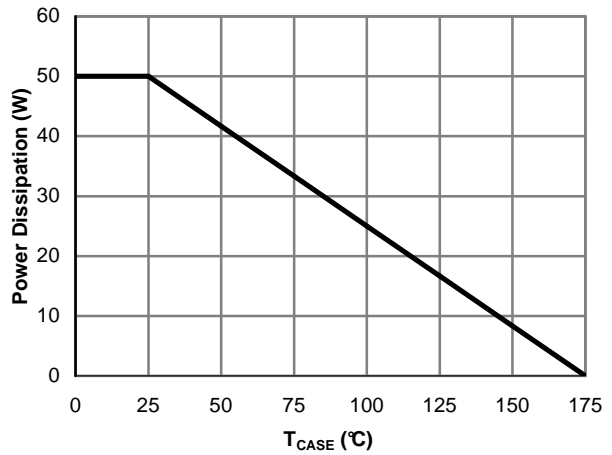

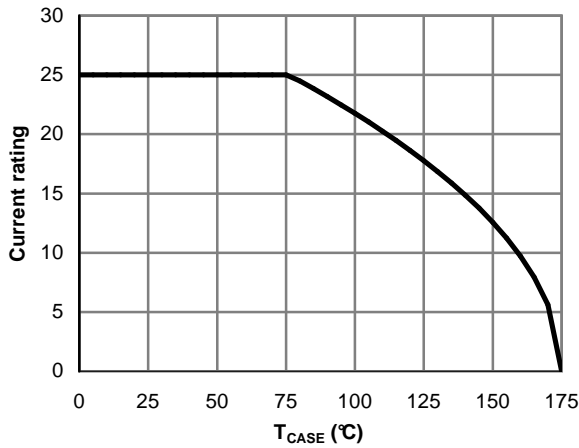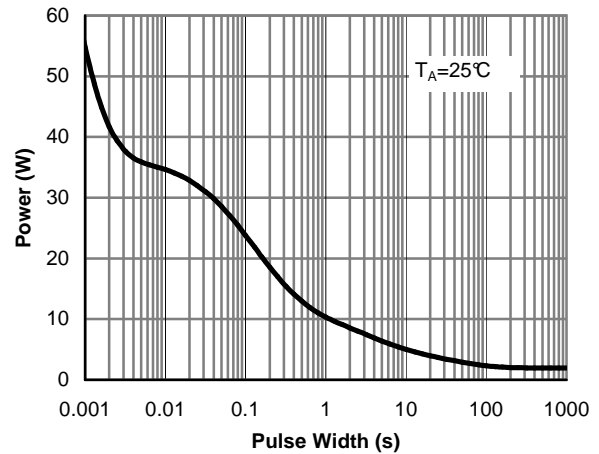**Figure 12: Single Pulse Avalanche capability**

Figure 13: Power De-rating (Note B)

Figure 14: Current De-rating (Note B)

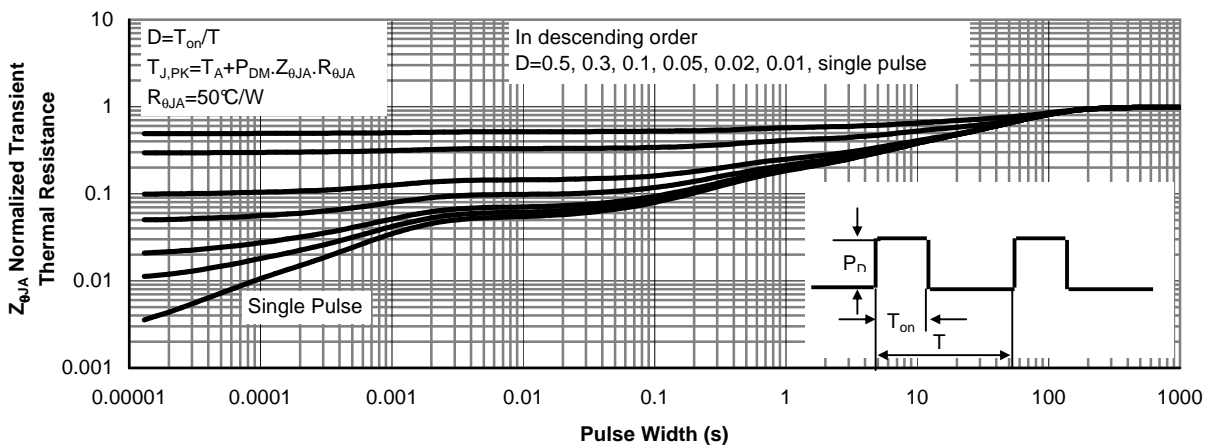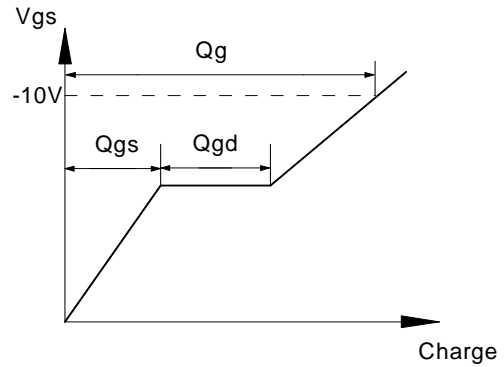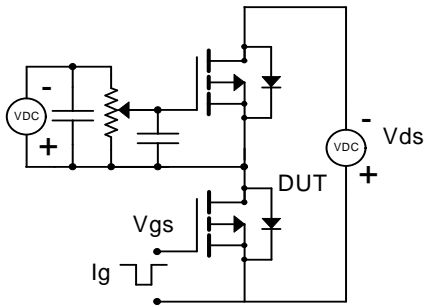**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)**

$D=T_{on}/T$

$T_{J,PK}=T_A+P_{DM}\cdot Z_{\theta JA}\cdot R_{\theta JA}$

$R_{\theta JA}=50℃/W$

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse
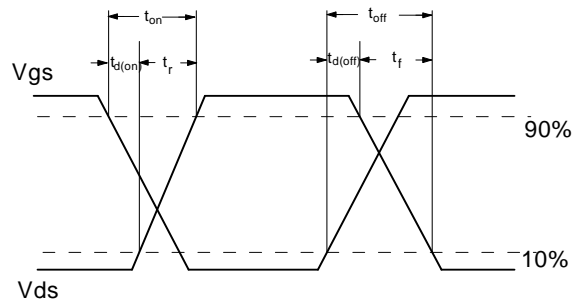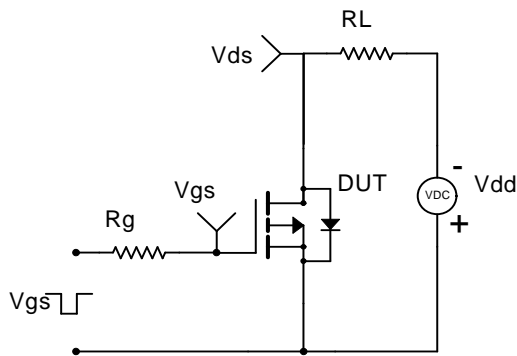
Single Pulse

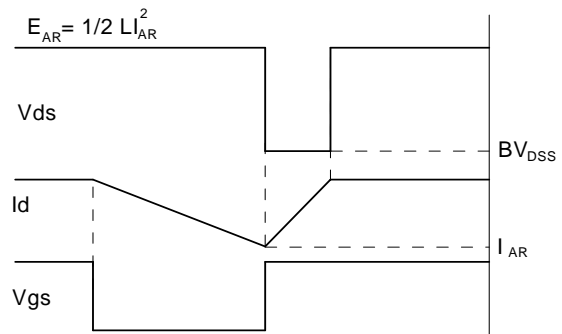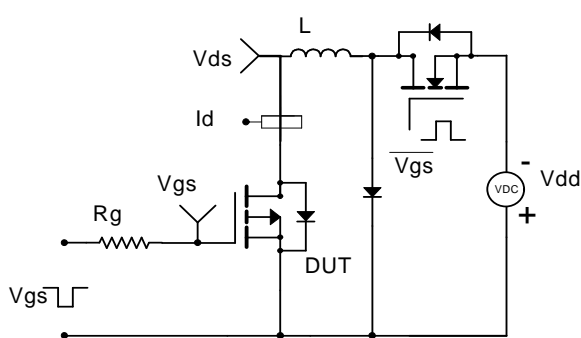**Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)**

Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

$$E_{AR} = 1/2\ LI_{AR}^2$$

Diode Recovery Test Circuit & Waveforms

$$Q_{rr} = -\int Idt$$