

General Description

The AON7405 uses advanced trench technology to provide excellent $R_{DS(ON)}$ with low gate charge.

This device is ideal for load switch and battery protection applications.

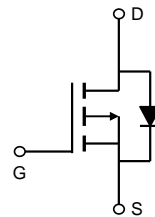
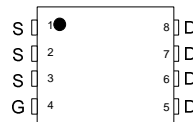
Product Summary

V_{DS}	-30V
I_D (at $V_{GS} = -10V$)	-50A
$R_{DS(ON)}$ (at $V_{GS} = -10V$)	< 6.2m Ω
$R_{DS(ON)}$ (at $V_{GS} = -6V$)	< 8.9m Ω

100% UIS Tested
100% R_g Tested



Top View



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted					
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V_{DS}	-30	V	
Gate-Source Voltage		V_{GS}	± 25	V	
Continuous Drain Current ^G	$T_C=25^\circ\text{C}$	I_D	-50	A	
	$T_C=100^\circ\text{C}$		-39		
Pulsed Drain Current ^C		I_{DM}	-210		
Continuous Drain Current	$T_A=25^\circ\text{C}$	I_{DSM}	-25	A	
	$T_A=70^\circ\text{C}$		-20		
Avalanche Current ^C		I_{AR}, I_{AS}	-44	A	
Repetitive avalanche energy $L=0.1\text{mH}$ ^C		E_{AR}, E_{AS}	97	mJ	
Power Dissipation ^B	$T_C=25^\circ\text{C}$	P_D	83	W	
	$T_C=100^\circ\text{C}$		33		
Power Dissipation ^A	$T_A=25^\circ\text{C}$	P_{DSM}	6.25	W	
	$T_A=70^\circ\text{C}$		4		
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$	
Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10\text{s}$	$R_{\theta JA}$	16	20	$^\circ\text{C/W}$
	Steady-State		45	55	$^\circ\text{C/W}$
Maximum Junction-to-Case		$R_{\theta JC}$	1.1	1.5	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±25V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =-250μA	-1.7	-2.2	-2.8	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	-210			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-20A T _J =125°C		5.1 7.6	6.2 9.2	mΩ
		V _{GS} =-6V, I _D =-20A		7.1	8.9	mΩ
		V _{GS} =-4.5V, I _D =-10A		10.7		mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-20A		46		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.7	-1	V
I _S	Maximum Body-Diode Continuous Current ^G				-50	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz	1960	2450	2940	pF
C _{oss}	Output Capacitance		380	550	720	pF
C _{rss}	Reverse Transfer Capacitance		220	370	520	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	7	14	28	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =-10V, V _{DS} =-15V, I _D =-20A	33	42	51	nC
Q _{g(4.5V)}	Total Gate Charge		16	21	26	nC
Q _{gs}	Gate Source Charge		5.5	7	8.5	nC
Q _{gd}	Gate Drain Charge		7	12	17	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-15V, R _L =0.75Ω, R _{GEN} =3Ω		9.5		ns
t _r	Turn-On Rise Time			10		ns
t _{D(off)}	Turn-Off DelayTime			104		ns
t _f	Turn-Off Fall Time			78		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-20A, dI/dt=500A/μs	20	25	30	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-20A, dI/dt=500A/μs	37	47	57	nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} t ≤ 10s value and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by package.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

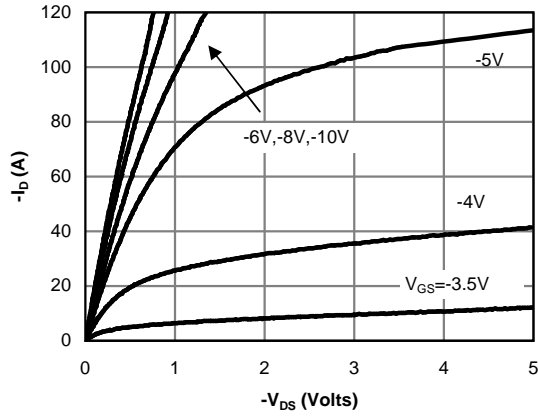


Fig 1: On-Region Characteristics (Note E)

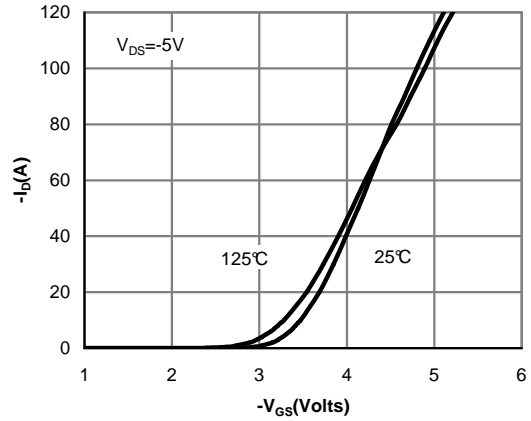


Figure 2: Transfer Characteristics (Note E)

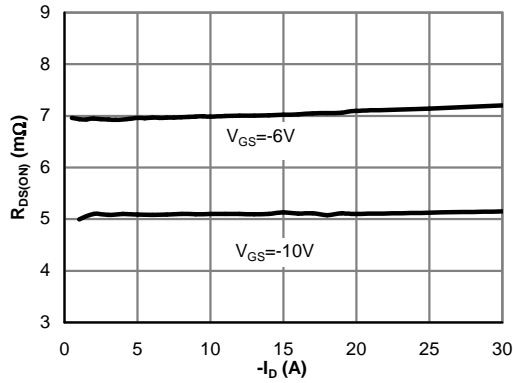


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

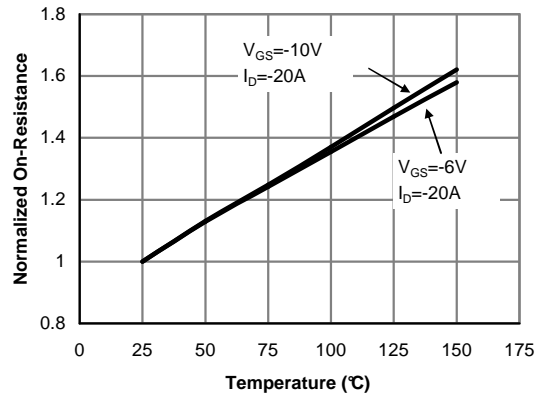


Figure 4: On-Resistance vs. Junction Temperature (Note E)

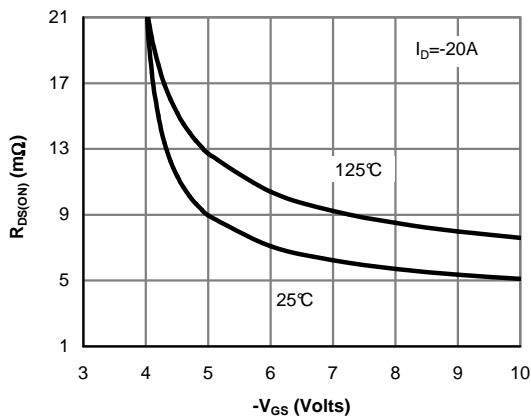


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

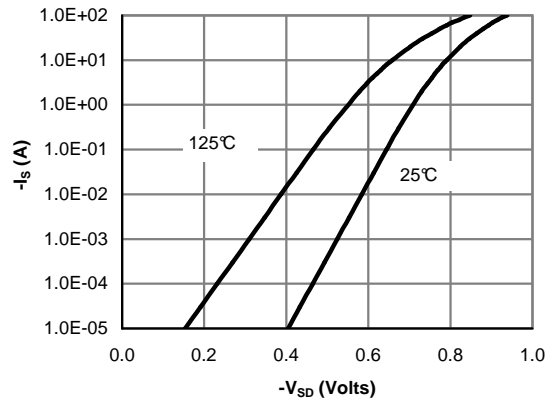


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

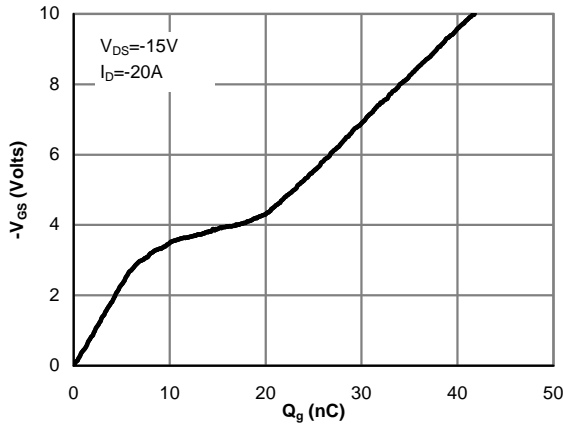


Figure 7: Gate-Charge Characteristics

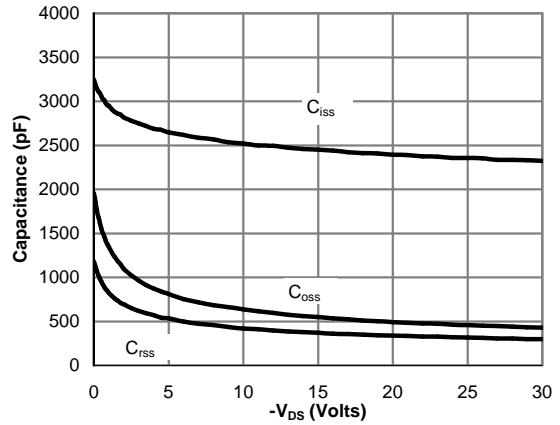


Figure 8: Capacitance Characteristics

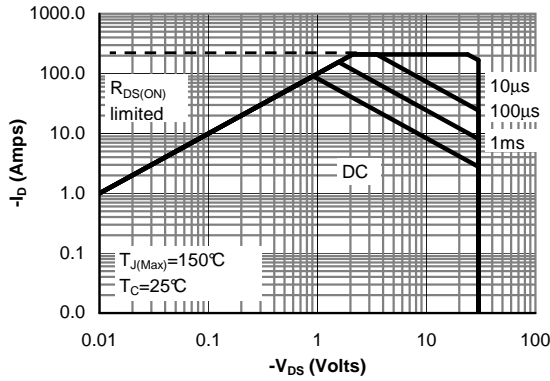


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

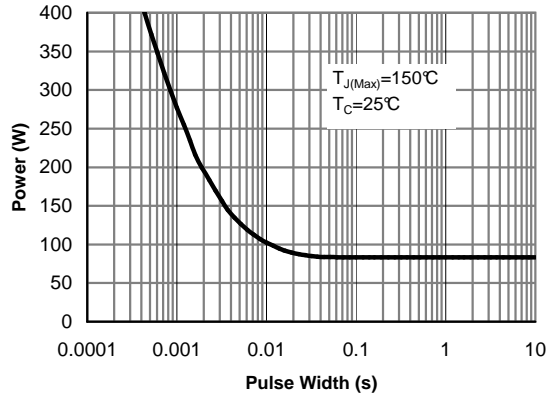


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

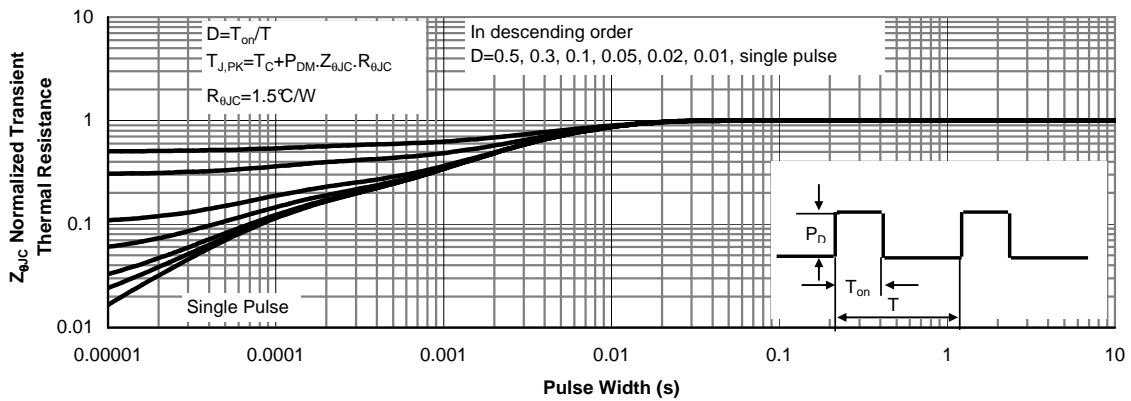


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

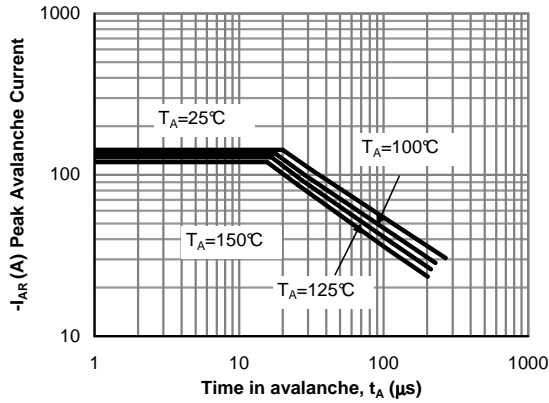


Figure 12: Single Pulse Avalanche capability (Note C)

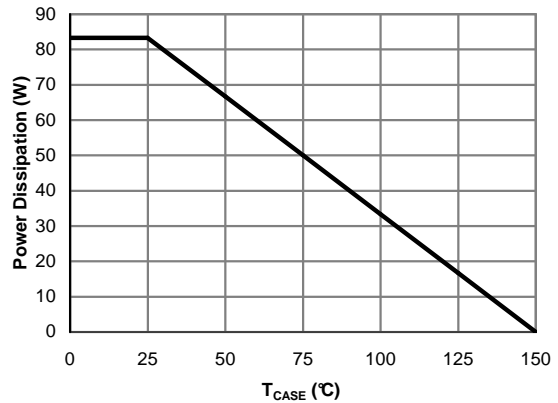


Figure 13: Power De-rating (Note F)

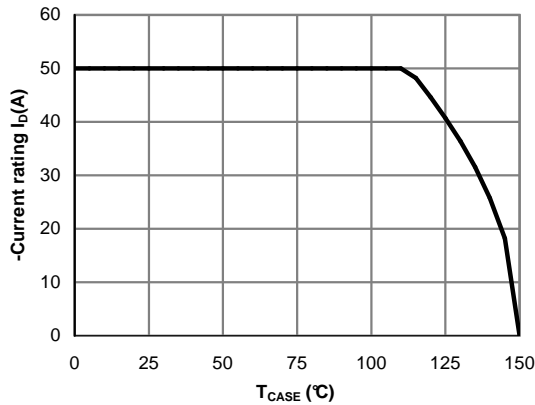


Figure 14: Current De-rating (Note F)

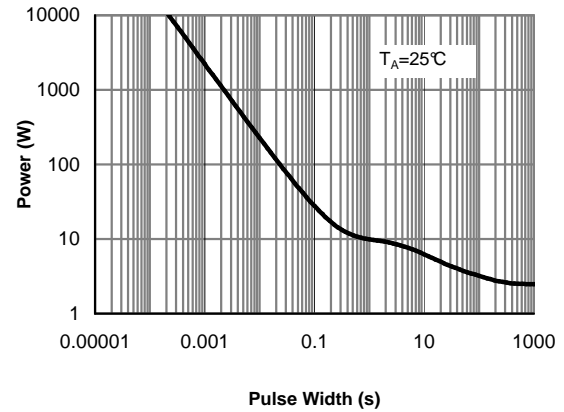


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

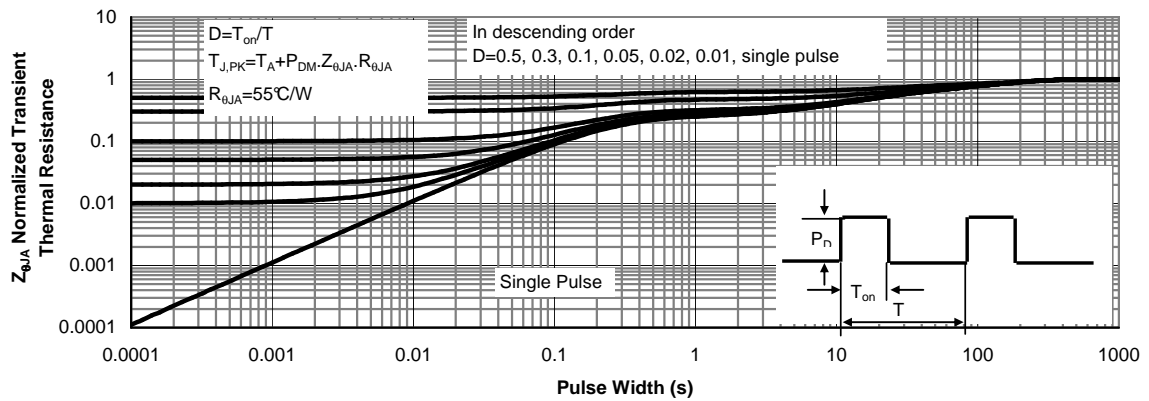
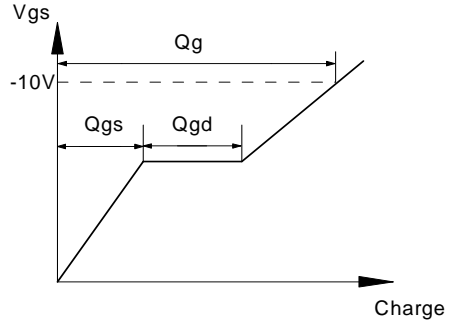
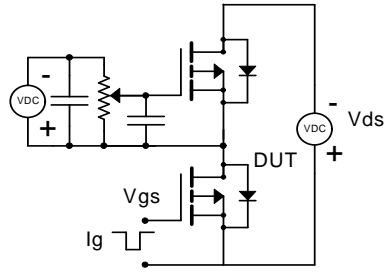
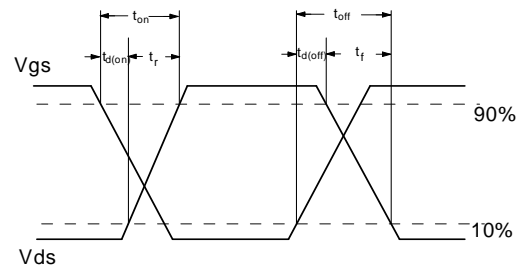
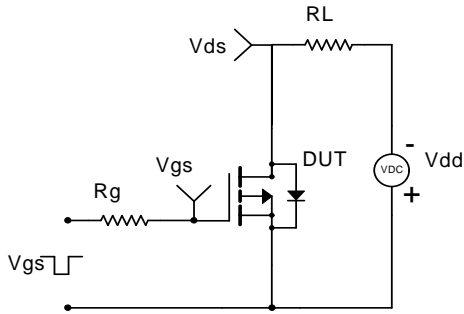


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

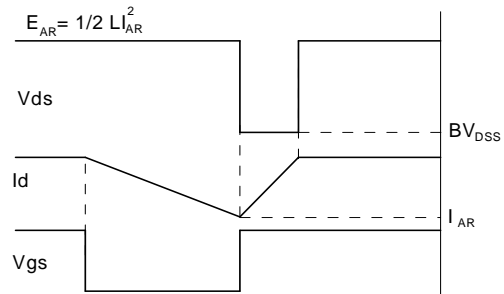
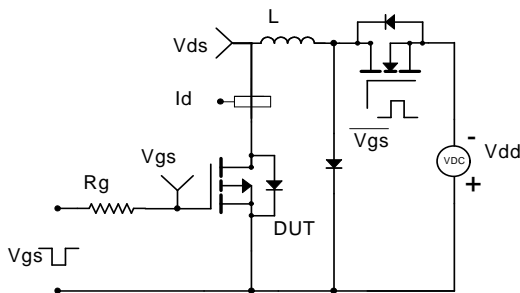
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

