

General Description

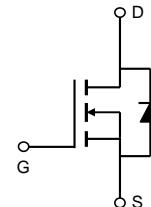
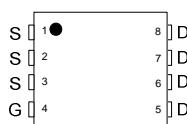
The AON7450 is fabricated with SDMOS™ trench technology that combines excellent $R_{DS(ON)}$ with low gate charge and low Qrr. The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

Features

V_{DS}	100V
I_D (at $V_{GS}=10V$)	21A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 48mΩ
$R_{DS(ON)}$ (at $V_{GS} = 8V$)	< 57mΩ



Top View



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current ^{T_C=25°C}	I_D	21	A
Continuous Drain Current ^{T_C=100°C}		13	
Pulsed Drain Current ^C	I_{DM}	60	
Continuous Drain Current ^{T_A=25°C}	I_{DSM}	5.6	A
Continuous Drain Current ^{T_A=70°C}		4.5	
Avalanche Current ^C	I_{AS}, I_{AR}	18	A
Avalanche energy L=0.1mH ^C	E_{AS}, E_{AR}	16	mJ
Power Dissipation ^B ^{T_C=25°C}	P_D	43	W
Power Dissipation ^B ^{T_C=100°C}		17	
Power Dissipation ^A ^{T_A=25°C}	P_{DSM}	3.1	W
Power Dissipation ^A ^{T_A=70°C}		2	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A ^{t ≤ 10s}	$R_{θJA}$	30	40	°C/W
Maximum Junction-to-Ambient ^{A D} Steady-State		60	75	°C/W
Maximum Junction-to-Case	Steady-State	$R_{θJC}$	2.4	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	100			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=100\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			10 50	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 25\text{V}$			100	nA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.9	3.5	4.1	V
$I_{\text{D(ON)}}$	On state drain current	$V_{GS}=10\text{V}, V_{DS}=5\text{V}$	60			A
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=7.8\text{A}$ $T_J=125^\circ\text{C}$		40 73	48 87	$\text{m}\Omega$
		$V_{GS}=8\text{V}, I_D=7.8\text{A}$		45	57	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=7.8\text{A}$		20		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.7	1	V
I_S	Maximum Body-Diode Continuous Current ^G				40	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=50\text{V}, f=1\text{MHz}$	725	910	1090	pF
C_{oss}	Output Capacitance		65	95	125	pF
C_{rss}	Reverse Transfer Capacitance		20	35	50	pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$	0.4	0.8	1.2	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=50\text{V}, I_D=7.8\text{A}$	12	16	20	nC
Q_{gs}	Gate Source Charge		4.2	5.3	6.4	nC
Q_{gd}	Gate Drain Charge		2.8	4.7	6.6	nC
$t_{\text{D(on)}}$	Turn-On DelayTime	$V_{GS}=10\text{V}, V_{DS}=50\text{V}, R_L=6.4\Omega, R_{\text{GEN}}=3\Omega$		18		ns
t_r	Turn-On Rise Time			6.5		ns
$t_{\text{D(off)}}$	Turn-Off DelayTime			35		ns
t_f	Turn-Off Fall Time			7		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=7.8\text{A}, dI/dt=500\text{A}/\mu\text{s}$	12	17	22	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=7.8\text{A}, dI/dt=500\text{A}/\mu\text{s}$	42	60	78	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ $t \leq 10\text{s}$ value and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(\text{MAX})}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})}=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(\text{MAX})}=150^\circ\text{C}$. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

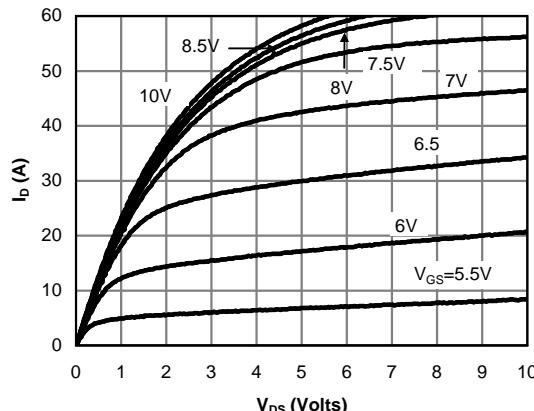


Fig 1: On-Region Characteristics (Note E)

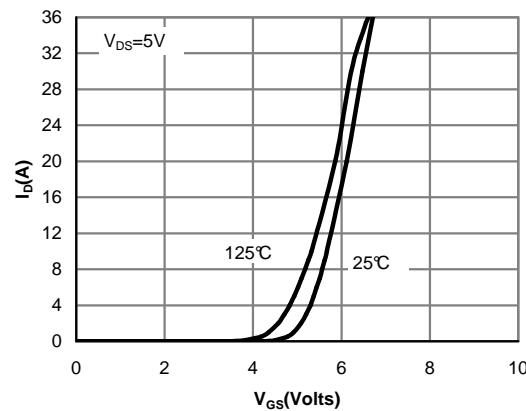


Figure 2: Transfer Characteristics (Note E)

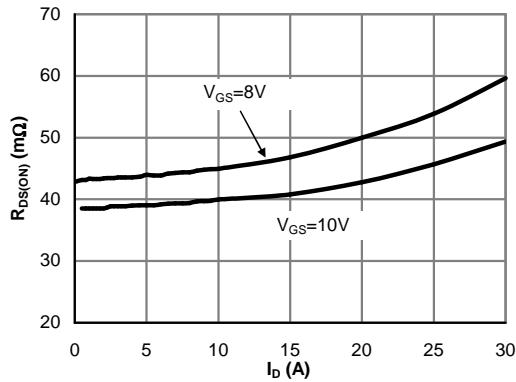


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

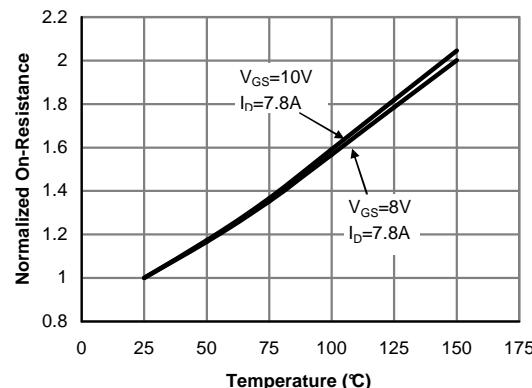


Figure 4: On-Resistance vs. Junction Temperature (Note E)

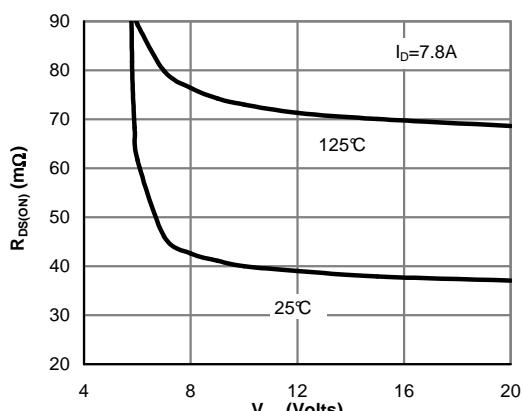


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

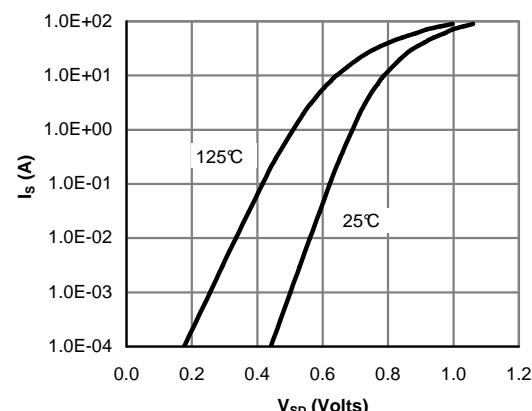
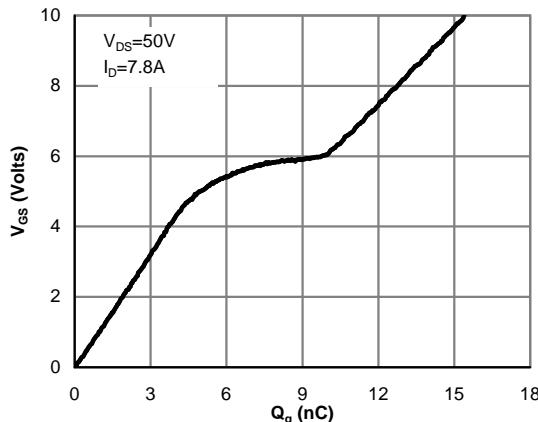
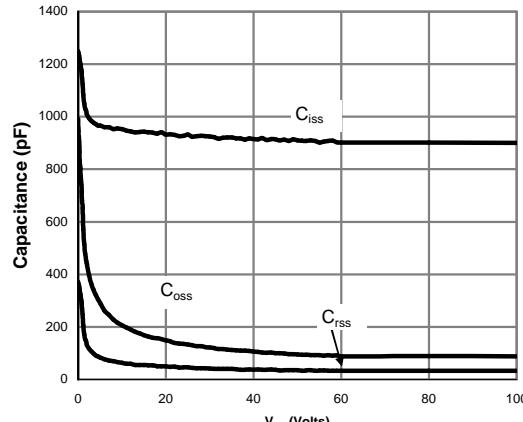
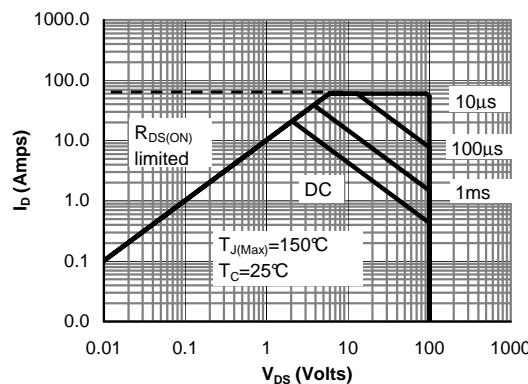
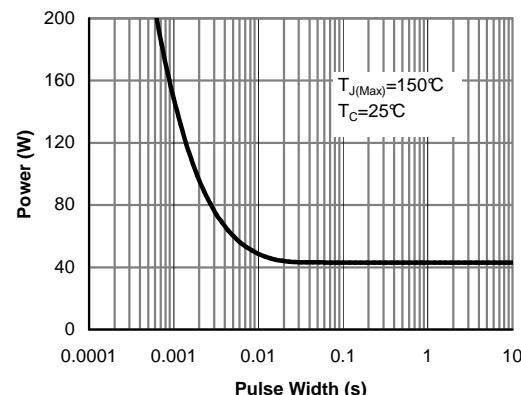
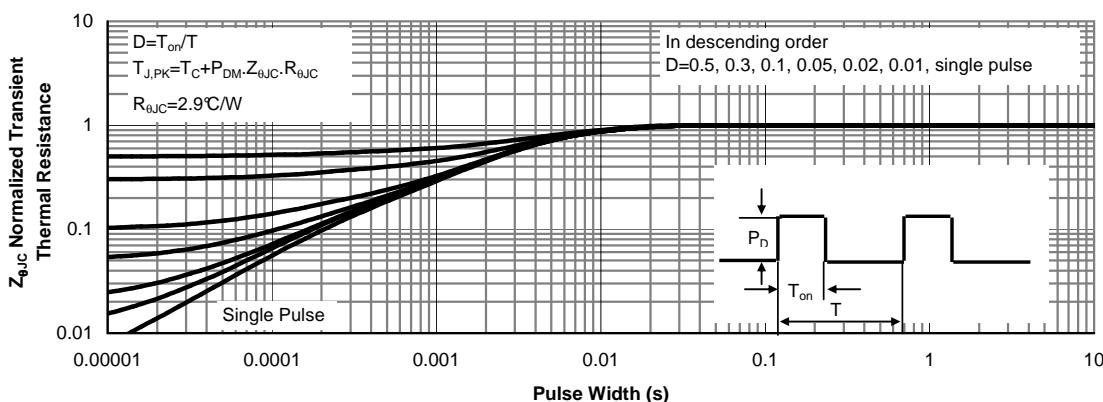


Figure 6: Body-Diode Characteristics (Note E)

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Figure 7: Gate-Charge Characteristics

Figure 8: Capacitance Characteristics

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

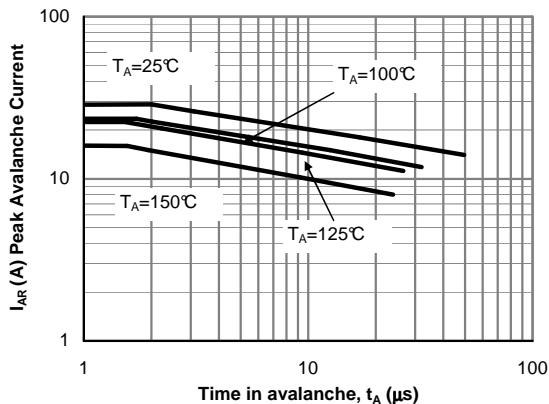
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Figure 12: Single Pulse Avalanche capability (Note C)

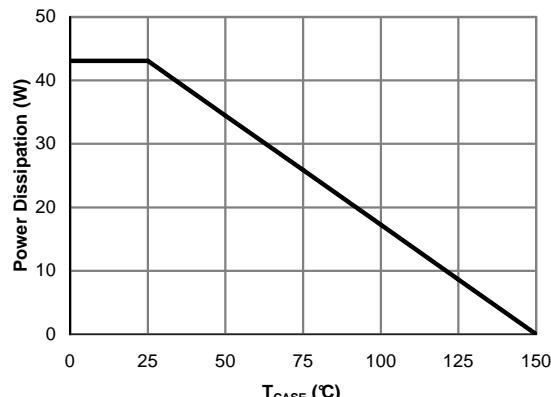


Figure 13: Power De-rating (Note F)

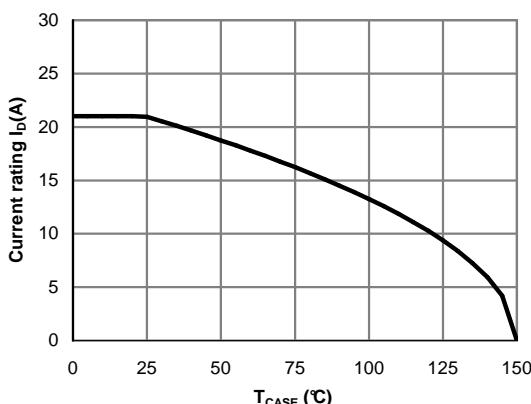


Figure 14: Current De-rating (Note F)

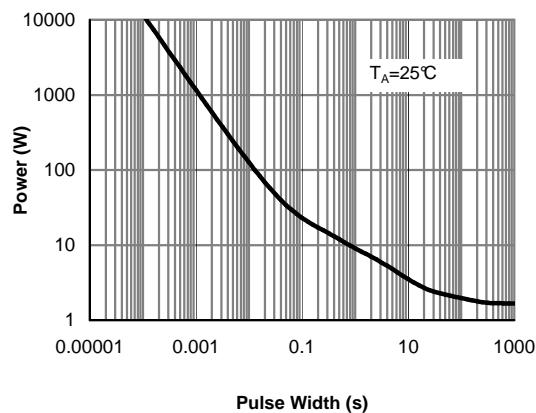


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

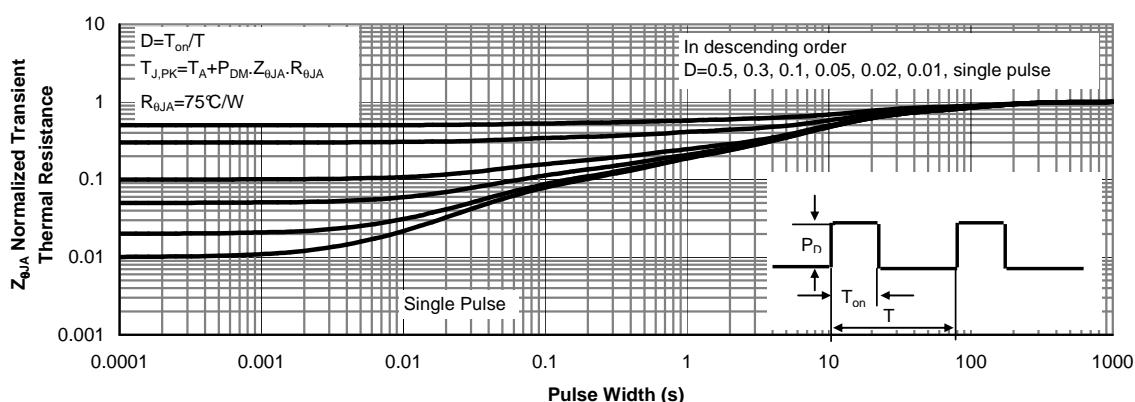


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

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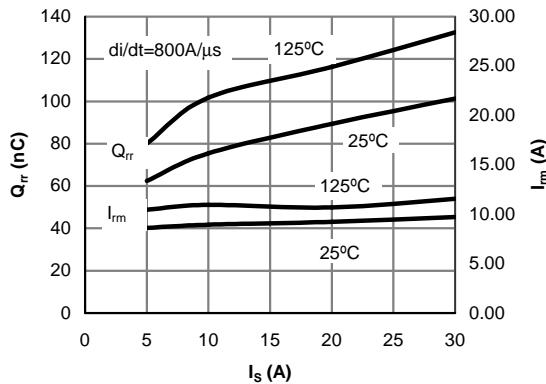


Figure 17: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

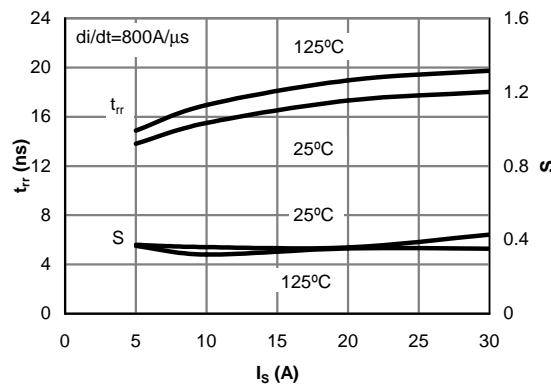


Figure 18: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

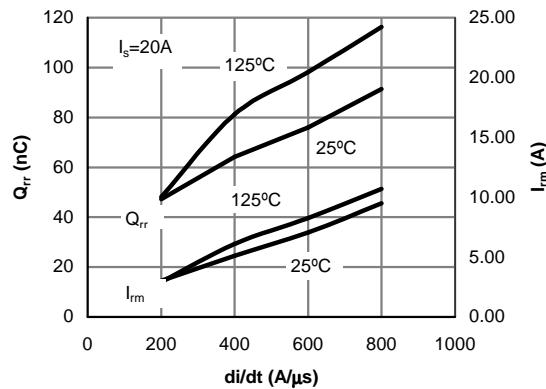


Figure 19: Diode Reverse Recovery Charge and Peak Current vs. di/dt

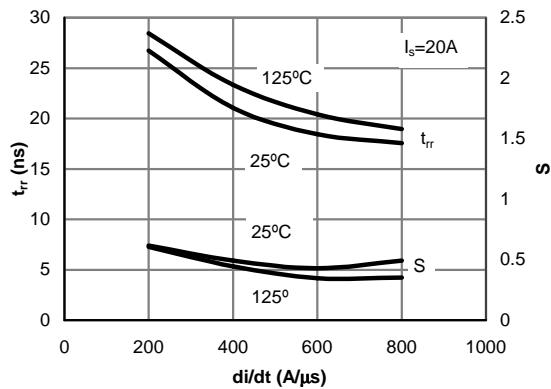
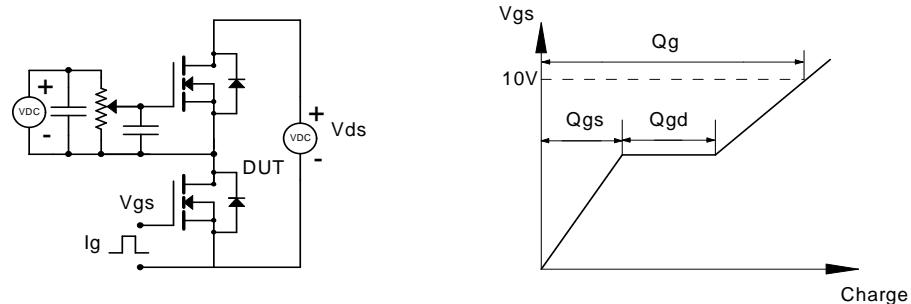
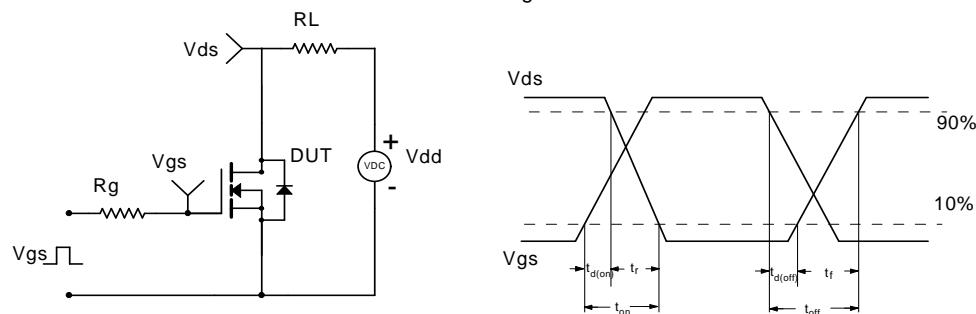


Figure 20: Diode Reverse Recovery Time and Softness Factor vs. di/dt

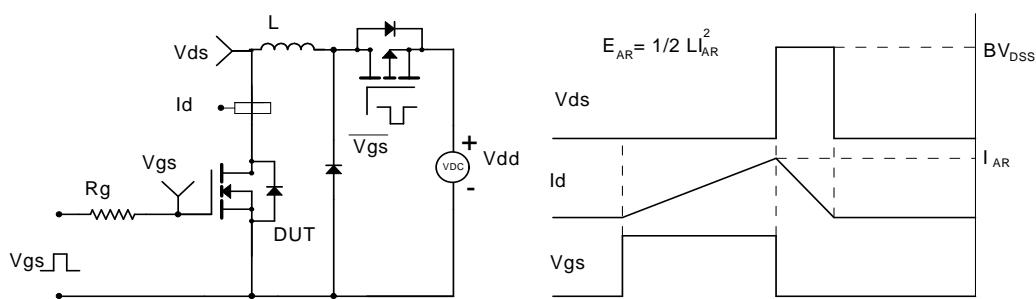
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

