AO5401E

P-Channel Enhancement Mode Field Effect Transistor

General Description

The AO5401E/L uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications.AO5401E and AO5401EL are electrically identical. -RoHS compliant

-AO5401EL is Halogen Free

Features

V_{DS} (V) = -20V

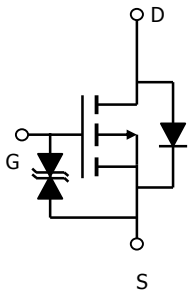
I_D = -0.5 A (V_{GS} = -4.5V)

$R_{DS(ON)}$ < 0.8Ω (V_{GS} = -4.5V)

$R_{DS(ON)}$ < 1Ω (V_{GS} = -2.5V)

$R_{DS(ON)}$ < 1.3Ω (V_{GS} = -1.8V)

ESD PROTECTED!



Absolute Maximum Ratings T_A=25°C unless otherwise noted					
Parameter		**Symbol**	**10 Sec**	**Steady State**	**Units**
Drain-Source Voltage		V_{DS}	-20		V
Gate-Source Voltage		V_{GS}	±8		V
Continuous Drain Current [AF]	T_A=25°C	I_D	-0.5	-0.5	A
	T_A=70°C		-0.45	-0.40	
Pulsed Drain Current [B]		I_{DM}	-1		
Power Dissipation [A]	T_A=25°C	P_D	0.38	0.28	W
	T_A=70°C		0.24	0.18	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	275	330	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		360	450	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	300	350	°C/W

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Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-20V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=10V, V_{GS}=±4.5V			±1	µA
		V_{DS}=10V, V_{GS}=±8V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-0.4	-0.5	-0.9	V
$I_{D(ON)}$	On state drain current	V_{GS}=-4.5V, V_{DS}=-5V	-1			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-4.5V, I_D=-0.5A		0.53	0.8	Ω
		T_J=125°C		0.75	0.95	
		V_{GS}=-2.5V, I_D=-0.5A		0.72	1	Ω
		V_{GS}=-1.8V, I_D=-0.3A		0.95	1.3	Ω
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-0.5A		0.9		S
V_{SD}	Diode Forward Voltage	I_S=-0.1A,V_{GS}=0V		-0.66	-1	V
I_S	Maximum Body-Diode Continuous Current				-0.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-10V, f=1MHz		72	100	pF
C_{oss}	Output Capacitance			17		pF
C_{rss}	Reverse Transfer Capacitance			9		pF
SWITCHING PARAMETERS						
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-4.5V, V_{DS}=-10V, R_L=50Ω, R_{GEN}=3Ω		60.5		ns
t_r	Turn-On Rise Time			150		ns
$t_{D(off)}$	Turn-Off DelayTime			612		ns
t_f	Turn-Off Fall Time			436		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-0.5A, dI/dt=100A/µs		27	35	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-0.5A, dI/dt=100A/µs		8.3		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using <300 µs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

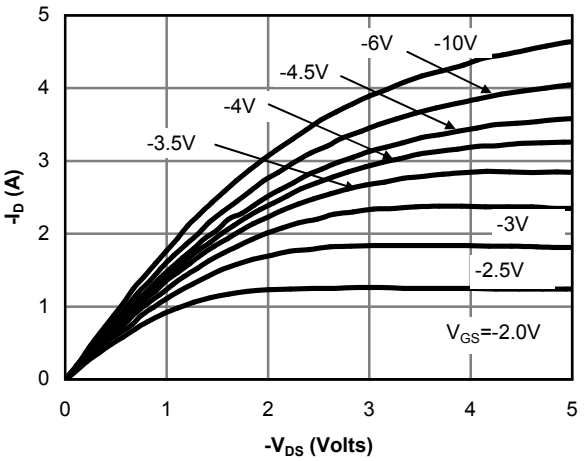


Figure 1: On-Region Characteristics

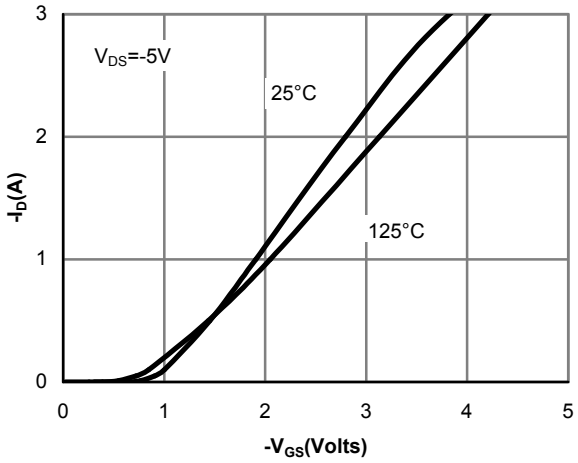


Figure 2: Transfer Characteristics

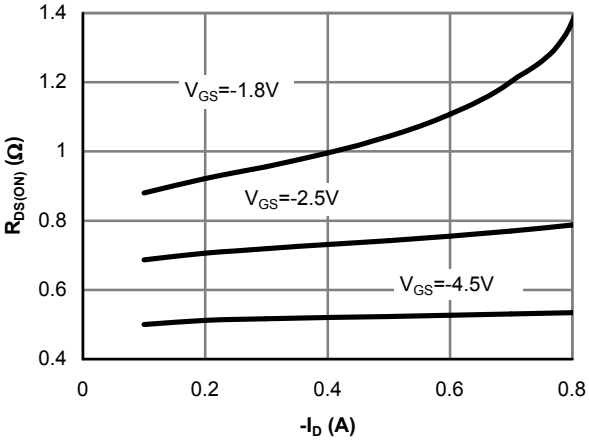


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

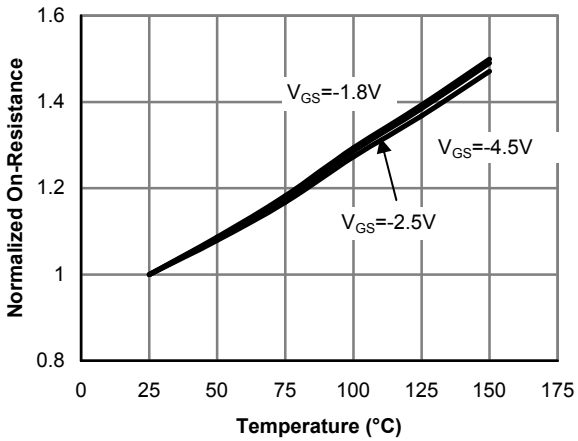


Figure 4: On-Resistance vs. Junction Temperature

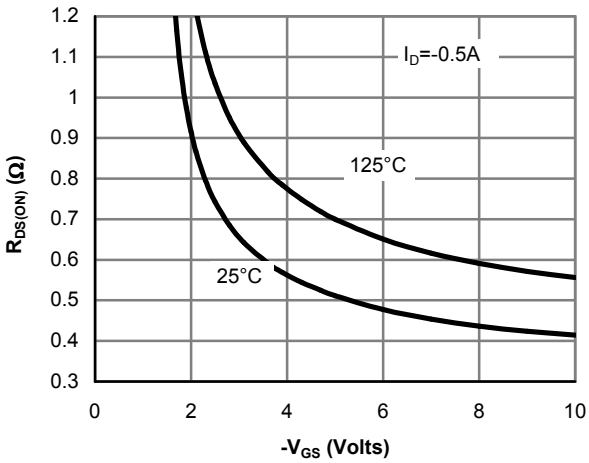


Figure 5: On-Resistance vs. Gate-Source Voltage

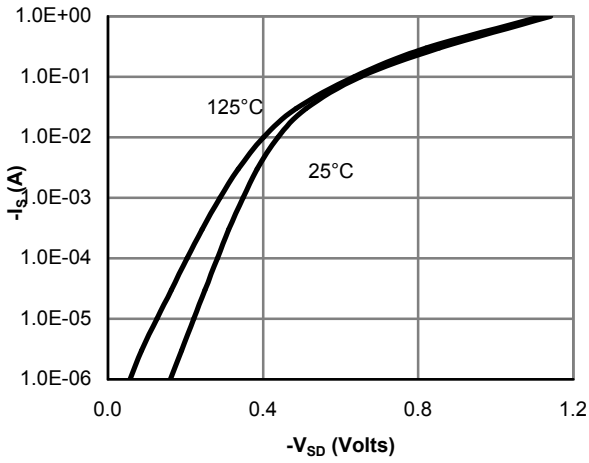


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

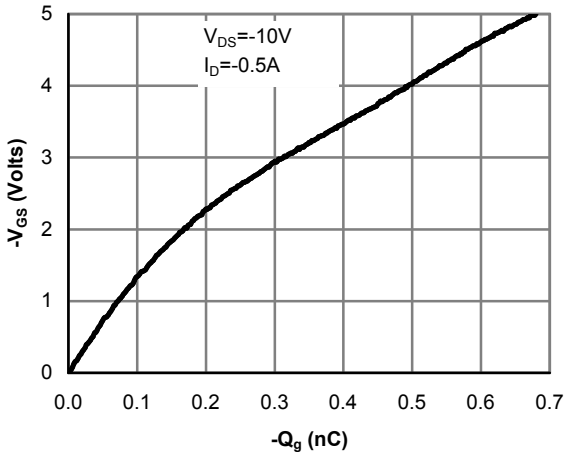


Figure 7: Gate-Charge Characteristics

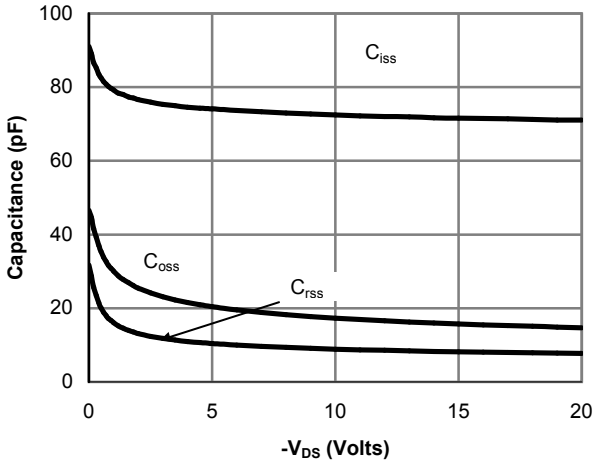


Figure 8: Capacitance Characteristics

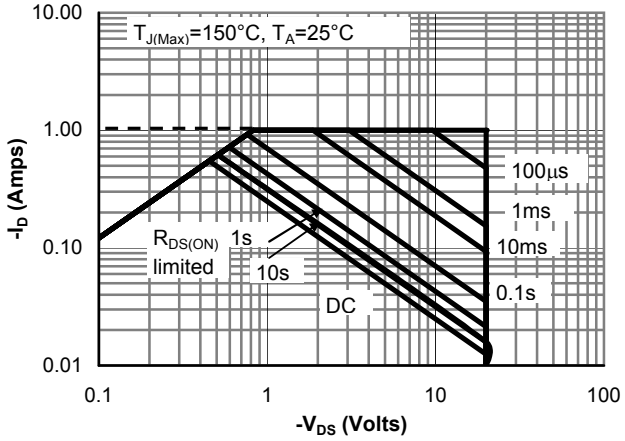


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

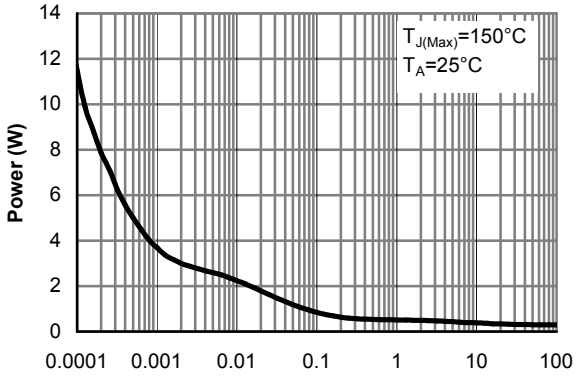


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

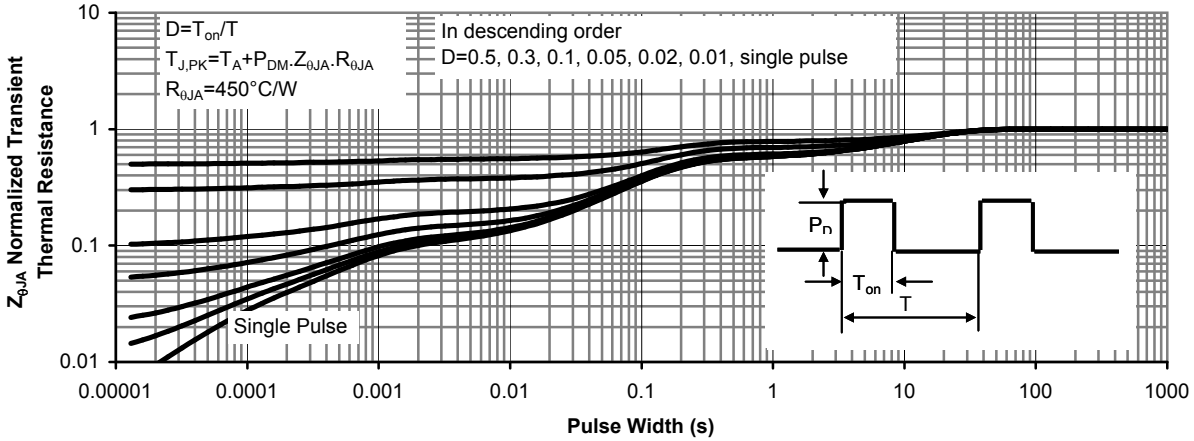
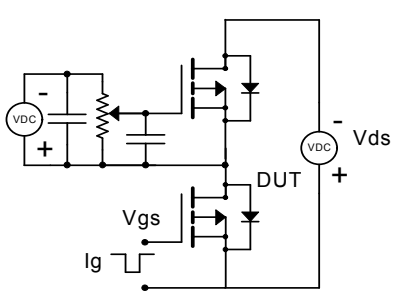
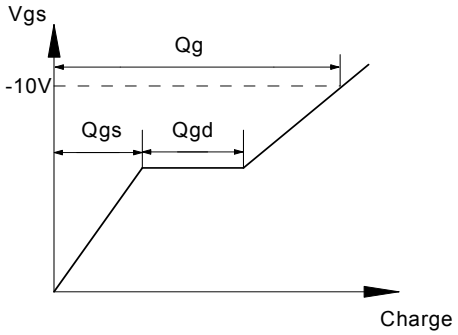


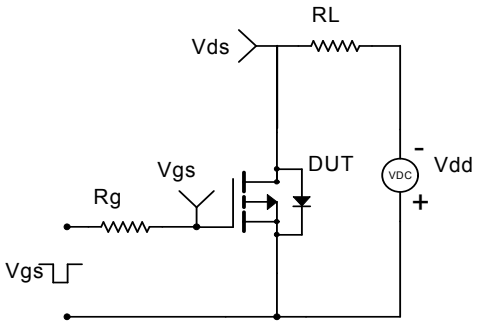
Figure 11: Normalized Maximum Transient Thermal Impedance

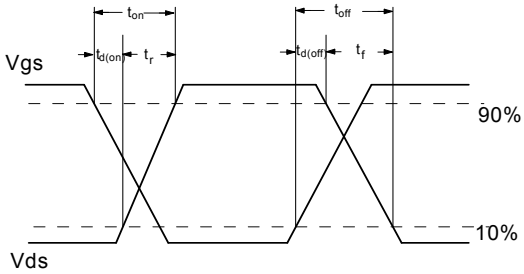
Gate Charge Test Circuit & Waveform





Resistive Switching Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms