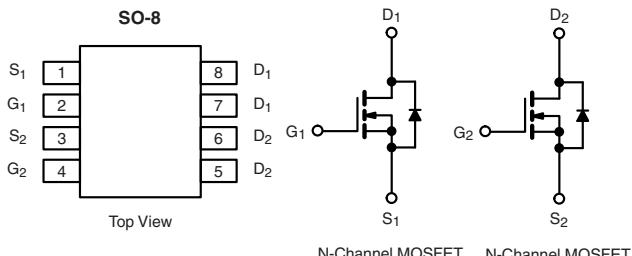


PRODUCT SUMMARY	
V_{DS} (V)	30
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.0145
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.0175
I_D (A) per leg	8
Configuration	Dual


FEATURES

- TrenchFET® Power MOSFET
- AEC-Q101 Qualified^d
- 100 % R_g and UIS Tested
- Material categorization:
 For definitions of compliance please see
www.freescale.net.cn


RoHS
 COMPLIANT
HALOGEN
FREE
ORDERING INFORMATION

Package	SO-8
Lead (Pb)-free and Halogen-free	SQ4920EY-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	I_D	8	A
		7.2	
Continuous Source Current (Diode Conduction) ^a	I_S	4	
Pulsed Drain Current ^b	I_{DM}	32	
Single Pulse Avalanche Current	I_{AS}	25	mJ
Single Pulse Avalanche Energy	E_{AS}	31	
Maximum Power Dissipation ^b	P_D	4.4	W
		1.4	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	110	°C/W
Junction-to-Foot (Drain)		34	

Notes

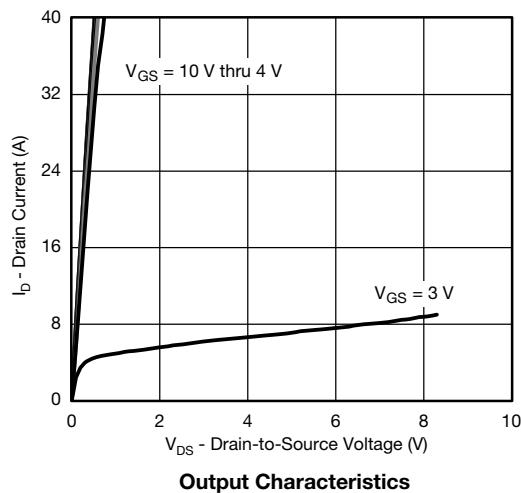
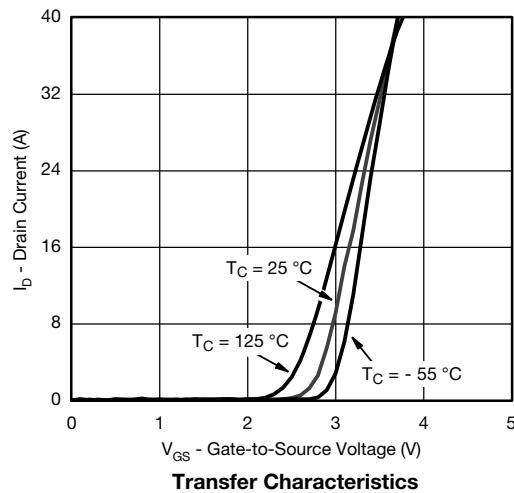
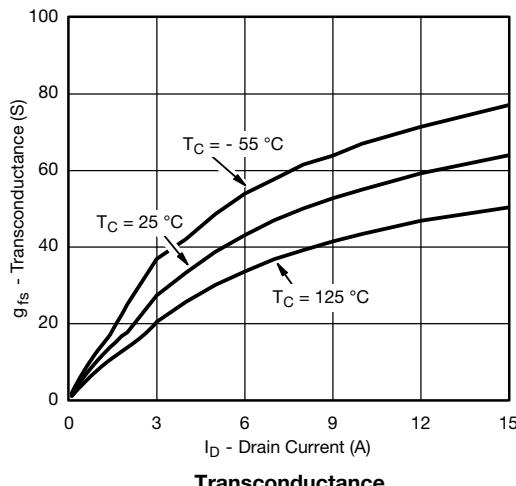
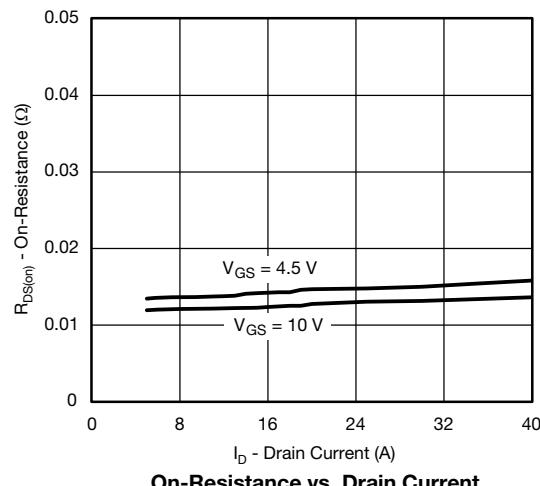
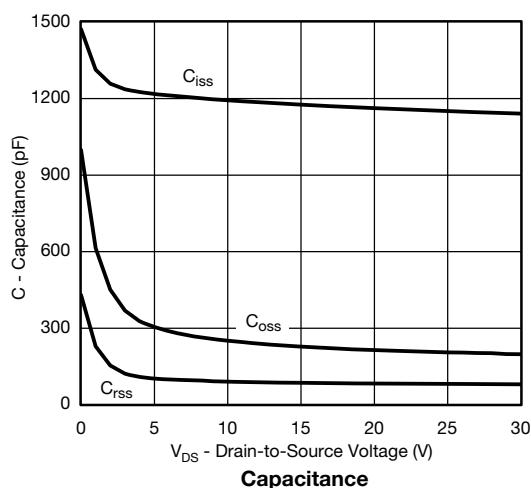
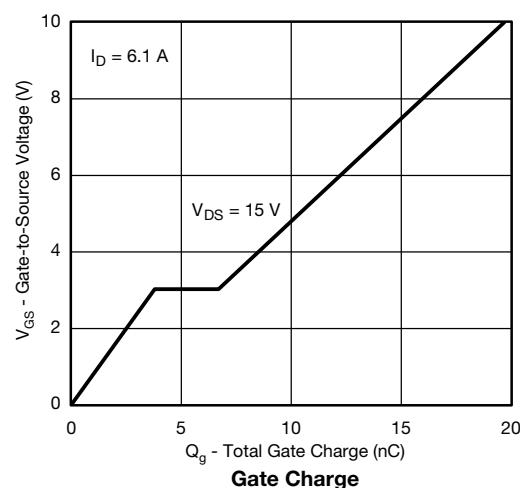
- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.

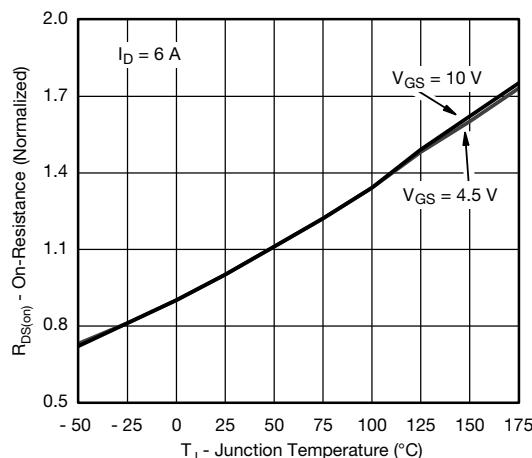
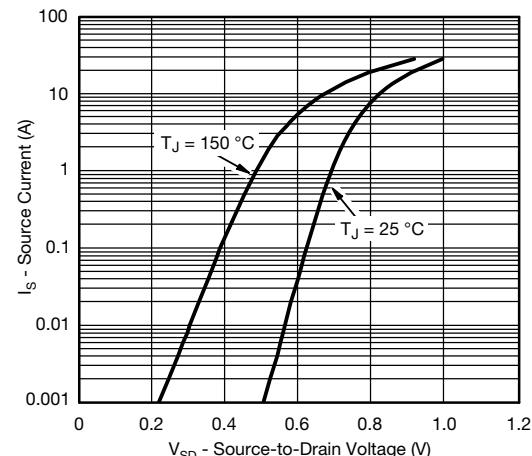
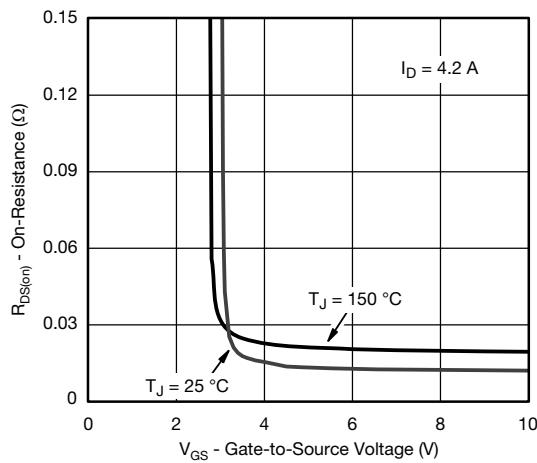
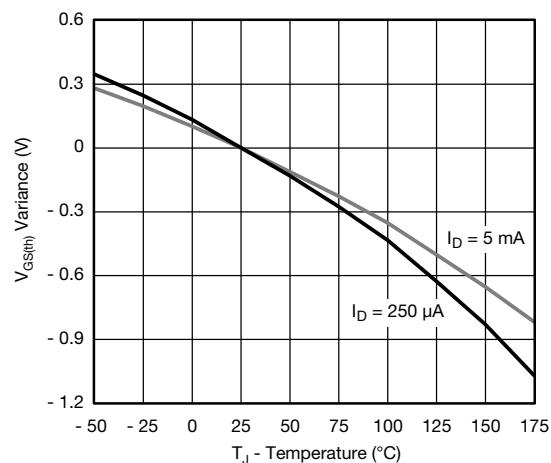
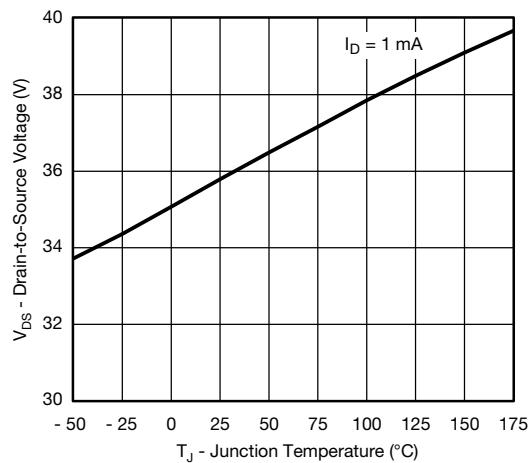
SPECIFICATIONS ($T_C = 25^\circ\text{C}$, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$, $I_D = 250 \mu\text{A}$		30	-	-	V	
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		1.5	2.0	2.5		
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0 \text{ V}$	$V_{DS} = 30 \text{ V}$	-	-	1.0	μA	
		$V_{GS} = 0 \text{ V}$	$V_{DS} = 30 \text{ V}$, $T_J = 125^\circ\text{C}$	-	-	50		
		$V_{GS} = 0 \text{ V}$	$V_{DS} = 30 \text{ V}$, $T_J = 175^\circ\text{C}$	-	-	150		
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{GS} = 10 \text{ V}$	$V_{DS} \geq 5 \text{ V}$	30	-	-	A	
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 4.5 \text{ V}$	$I_D = 5 \text{ A}$	-	0.016	0.0175	Ω	
		$V_{GS} = 10 \text{ V}$	$I_D = 6 \text{ A}$	-	0.013	0.0145		
		$V_{GS} = 10 \text{ V}$	$I_D = 6 \text{ A}$, $T_J = 125^\circ\text{C}$	-	-	0.024		
		$V_{GS} = 10 \text{ V}$	$I_D = 6 \text{ A}$, $T_J = 175^\circ\text{C}$	-	-	0.028		
Forward Transconductance ^f	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 6 \text{ A}$		-	43	-	S	
Dynamic^b								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$	$V_{DS} = 15 \text{ V}$, $f = 1 \text{ MHz}$	-	1175	1465	pF	
Output Capacitance	C_{oss}			-	225	280		
Reverse Transfer Capacitance	C_{rss}			-	85	105		
Total Gate Charge ^c	Q_g	$V_{GS} = 10 \text{ V}$	$V_{DS} = 15 \text{ V}$, $I_D = 6.1 \text{ A}$	-	19.7	30	nC	
Gate-Source Charge ^c	Q_{gs}			-	3.8	-		
Gate-Drain Charge ^c	Q_{gd}			-	2.9	-		
Gate Resistance	R_g	$f = 1 \text{ MHz}$		2.5	-	7.5	Ω	
Turn-On Delay Time ^c	$t_{d(\text{on})}$	$V_{DD} = 15 \text{ V}$, $R_L = 15 \Omega$ $I_D \geq 1 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 1 \Omega$		-	7	10	ns	
Rise Time ^c	t_r			-	10	15		
Turn-Off Delay Time ^c	$t_{d(\text{off})}$			-	25	37		
Fall Time ^c	t_f			-	8	12		
Source-Drain Diode Ratings and Characteristics^b								
Pulsed Current ^a	I_{SM}			-	-	32	A	
Forward Voltage	V_{SD}	$I_F = 1.8 \text{ A}$, $V_{GS} = 0$		-	0.75	1.1	V	

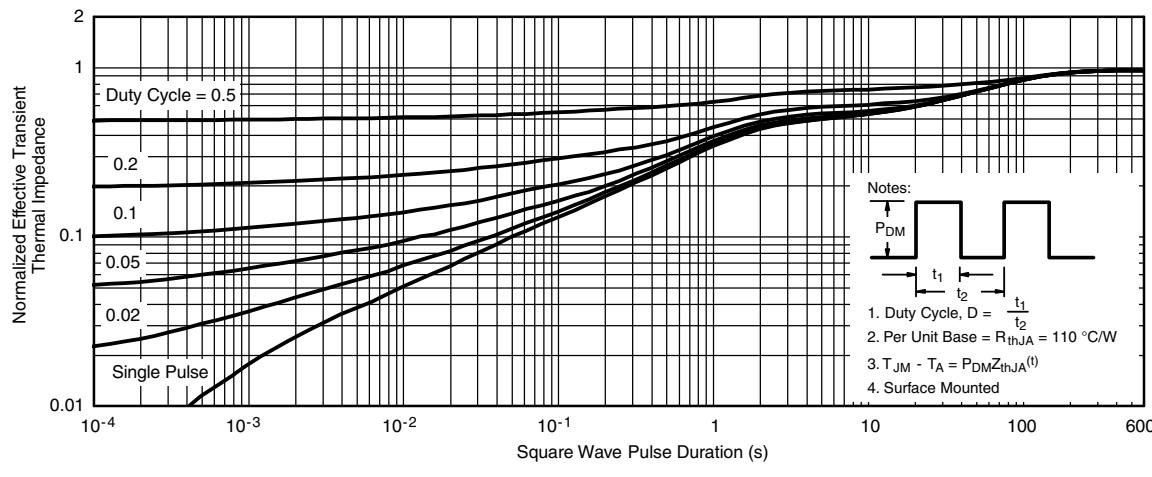
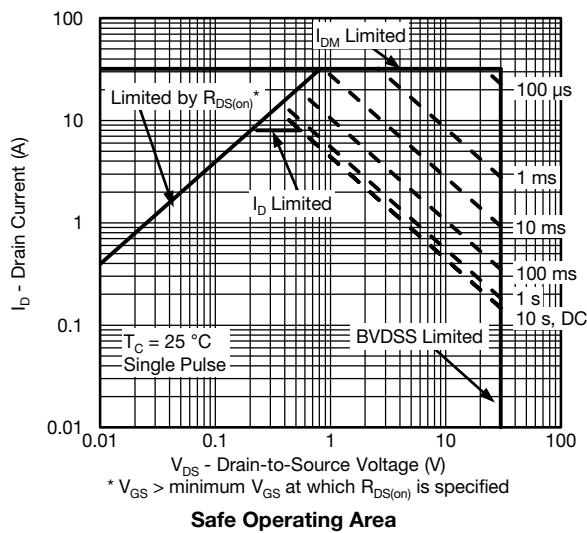
Notes

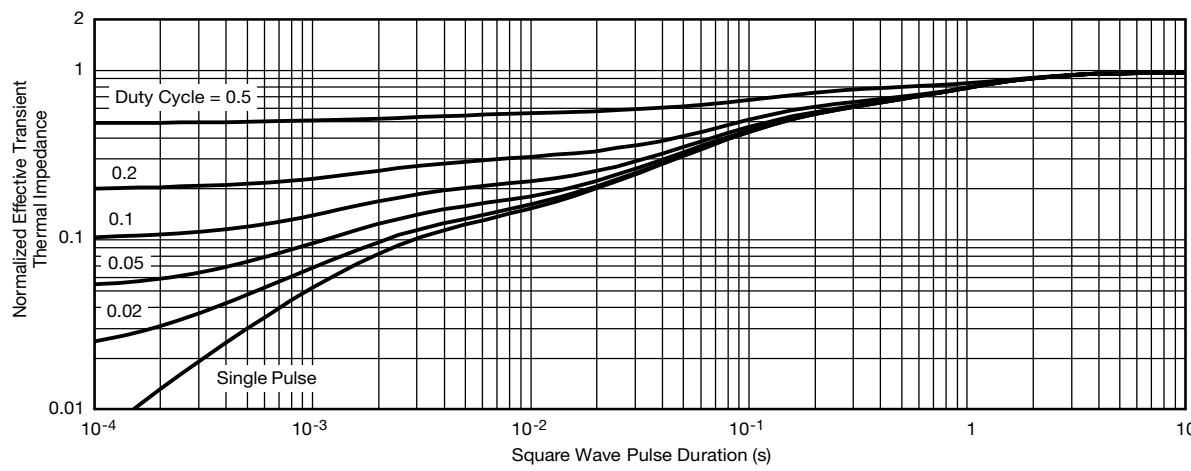
- Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge

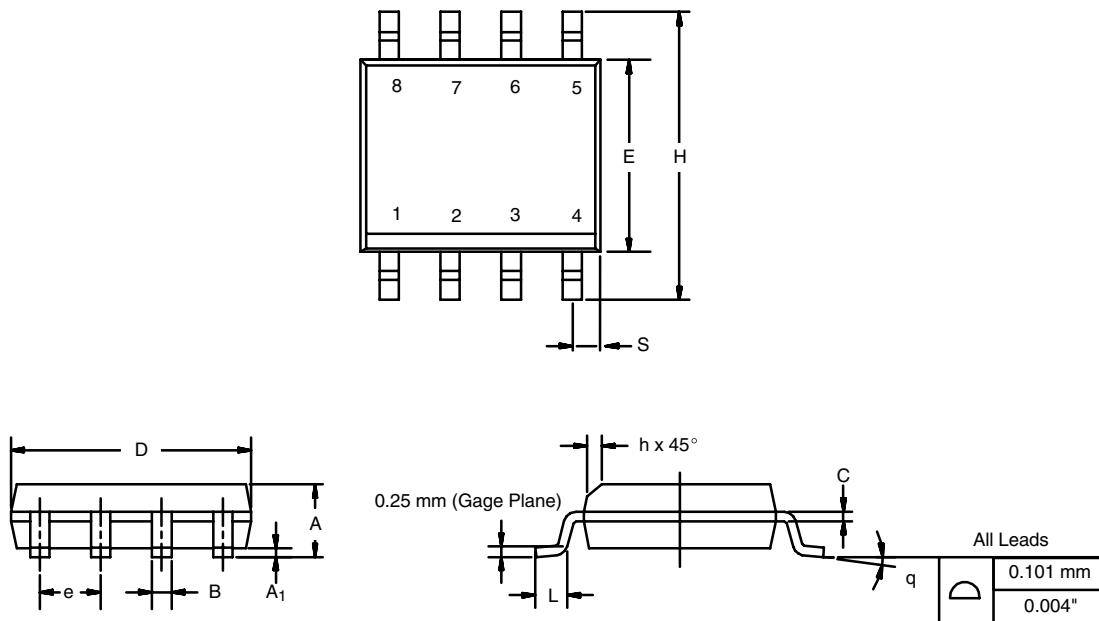
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

On-Resistance vs. Junction Temperature

Drain Source Breakdown vs. Junction Temperature

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)


THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Foot
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

SOIC (NARROW): 8-LEAD
 JEDEC Part Number: MS-012


DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

ECN: C-06527-Rev. I, 11-Sep-06
 DWG: 5498

Mounting LITTLE FOOT®, SO-8 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (www.freescale.net.cn), for the basis of the pad design for a LITTLE FOOT SO-8 power MOSFET. In converting this recommended minimum pad to the pad set for a power MOSFET, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

In the case of the SO-8 package, the thermal connections are very simple. Pins 5, 6, 7, and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In a dual package, pins 5 and 6 are one drain, and pins 7 and 8 are the other drain. For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

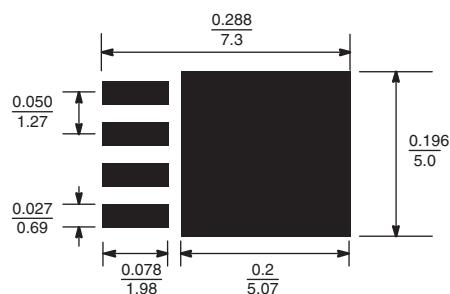


Figure 1. Single MOSFET SO-8 Pad Pattern With Copper Spreading

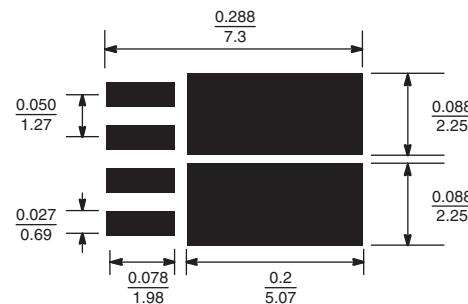


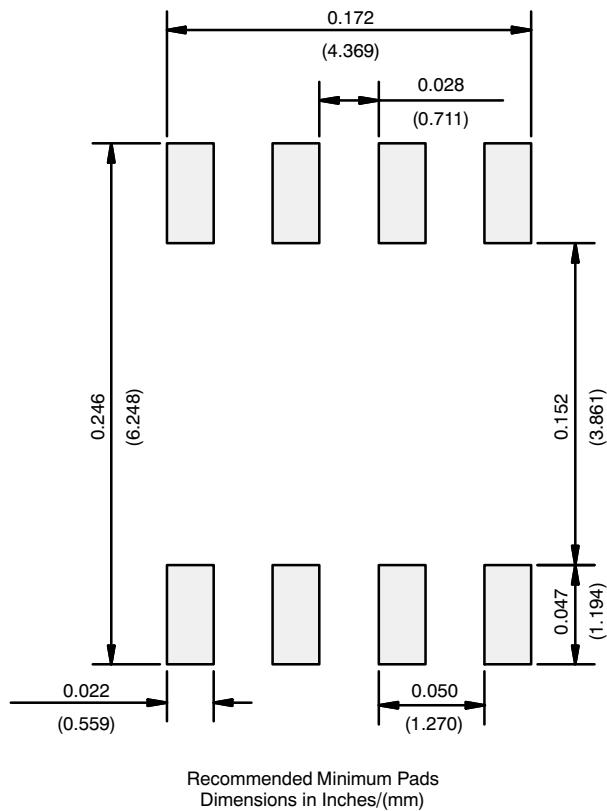
Figure 2. Dual MOSFET SO-8 Pad Pattern With Copper Spreading

The minimum recommended pad patterns for the single-MOSFET SO-8 with copper spreading (Figure 1) and dual-MOSFET SO-8 with copper spreading (Figure 2) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. These patterns use all the available area underneath the body for this purpose.

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

RECOMMENDED MINIMUM PADS FOR SO-8



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