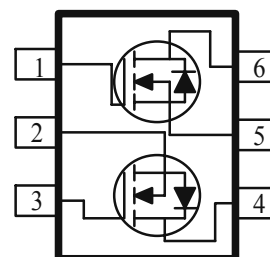
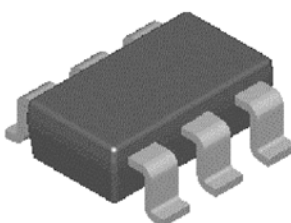


## N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low  $r_{DS(on)}$  assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low  $r_{DS(on)}$  Provides Higher Efficiency and Extends Battery Life
- Miniature TSOP-6 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications



PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ m( $\Omega$ )	$I_D$ (A)
30	58 @ $V_{GS} = 10V$	3.5
	82 @ $V_{GS} = 4.5V$	3.0

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		$V_{DS}$	30	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>a</sup>	$T_A = 25^\circ\text{C}$	$I_D$	3.5	A
	$T_A = 70^\circ\text{C}$		2.8	
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	16	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	1.25	A
Power Dissipation <sup>a</sup>	$T_A = 25^\circ\text{C}$	$P_D$	1.3	W
	$T_A = 70^\circ\text{C}$		0.8	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	100	$^\circ\text{C/W}$
	Steady-State		166	$^\circ\text{C/W}$

### Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

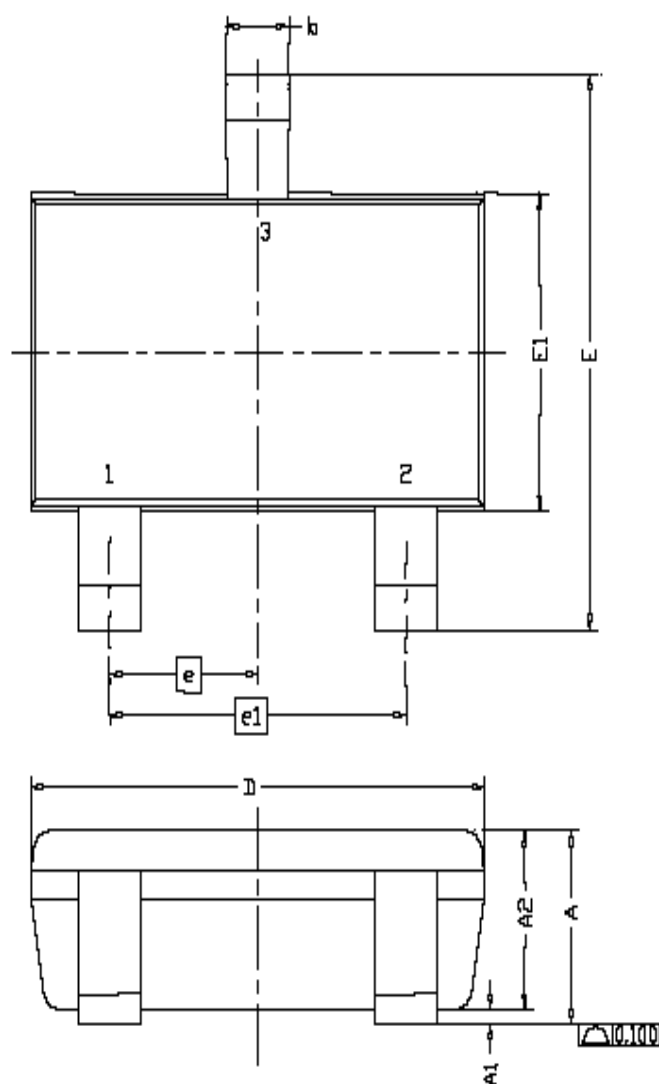
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 uA	1			V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			1	uA
		V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C			25	
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	6			A
Drain-Source On-Resistance <sup>A</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.5 A			58	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3 A			82	
Forward Tranconductance <sup>A</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3.5 A		6.9		S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 2.3 A, V <sub>GS</sub> = 0 V		0.8	1.2	V
Dynamic <sup>b</sup>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.5 A		2.2		nC
Gate-Source Charge	Q <sub>gs</sub>			0.5		
Gate-Drain Charge	Q <sub>gd</sub>			0.8		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 25 V, R <sub>L</sub> = 25 Ω , I <sub>D</sub> = 1 A, V <sub>GEN</sub> = 10 V		16		nS
Rise Time	t <sub>r</sub>			5		
Turn-Off Delay Time	t <sub>d(off)</sub>			23		
Fall-Time	t <sub>f</sub>			3		

## Notes

- Pulse test:  $PW \leq 300\mu\text{s}$  duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

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# Package Information



DIM.	MILLIMETERS		
	MIN	NOM	MAX
A	0.935	0.95	1.10
A1	0.01	---	0.10
A2	0.85	0.90	0.925
b	0.30	0.40	0.50
c	0.10	0.15	0.25
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.40	0.60
L1	0.60 REF		
L2	0.25 BSC		
R	0.10	---	---
$\theta$	0°	4°	8°
$\theta_1$	7° NOM		

