Triple Output Regulator with Single Synchronous Buck and Dual LDO

The ISL6413 is a highly integrated triple output regulator which provides a single chip solution for wireless chipset power management. The device integrates high efficiency synchronous buck regulator with two ultra low noise LDO regulators. The IC accepts an input voltage range of 3.0V to 3.6V and provides three regulated output voltages: 1.8V (PWM), 2.84V (LDO1), and another ultra-clean 2.84V (LDO2).

The Synchronous current mode PWM regulator with integrated N- and P-channel power MOSFET provides pre-set 1.8V for BBP/MAC core supply. Synchronous rectification with internal MOSFETs is used to achieve higher efficiency and reduced number of external components. Operating frequency is typically 750kHz allowing the use of smaller inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 500kHz to 1MHz. The PG_PWM output indicates loss of regulation on PWM output.

The ISL6413 also has two LDO regulators which use an internal PMOS transistor as the pass device. LDO2 features ultra low noise that does not typically exceed 30µV RMS to aid VCO stability. The EN_LDO pin controls LDO1 and LDO2 outputs. The ISL6413 also integrates a RESET function, which eliminates the need for additional RESET IC required in WLAN applications. The IC asserts a RESET signal whenever the V_{IN} supply voltage drops below a preset threshold, keeping it asserted for at least 25ms after V_{IN} has risen above the reset threshold. The PG_LDO output indicates loss of regulation on either of the two LDO outputs. Other features include over current protection for all three outputs and thermal shutdown.

High integration and the thin Quad Flat No-lead (QFN) package makes ISL6413 an ideal choice to power many of today's small form factor industry standard wireless cards such as PCMCIA, mini-PCI and Cardbus-32.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. DWG. #
ISL6413IR	-40 to 85	24 Ld QFN	L24.4x4B

Features

- Fully Integrated Synchronous Buck Regulator + Dual LDO
- High Output Current (For QFN package)
  - PWM, 1.8V 400mA
  - LDO1, 2.84V 300mA
  - LDO2, 2.84V 200mA
- Ultra-Compact DC-DC Converter Design
- Stable with Small Ceramic Output Capacitors
- High conversion efficiency
- Low Shutdown supply current
- Ultra-Low Dropout Voltage for LDOs
  - LDO1, 2.84V . . . . . 125mV (typ.) at 300mA
  - LDO2, 2.84V . . . . . 100mV (typ.) at 200mA
- Ultra-Low Output Voltage Noise
  - <30µV_{RMS} (typ.) for LDO2 (VCO Supply)
- PG_LDO, PG_PWM and $\overline{\text{PG\_PWM}}$ outputs
- Extensive circuit protection and monitoring features
  - Over voltage protection
  - Over current protection
  - Shutdown
  - Thermal Shutdown
- Integrated RESET output for microprocessor reset
- Proven Reference Design for Total WLAN System Solution
- QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - Near Chip-Scale Package Footprint Improves PCB Efficiency and Is Thinner in Profile

Applications

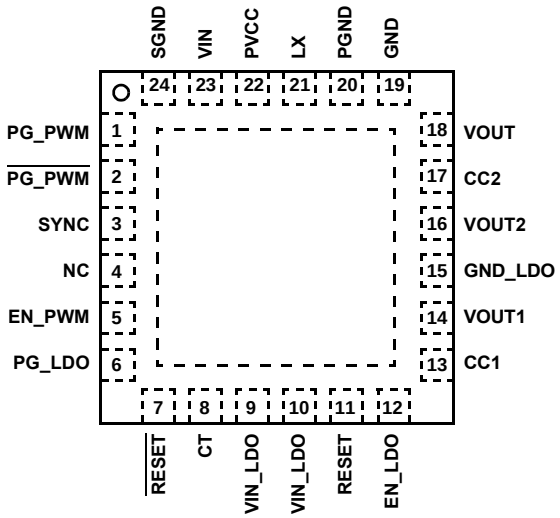
- WLAN Cards
  - PCMCIA, Cardbus32, MiniPCI Cards
  - Compact Flash Cards
- Liberty Chipset
- Hand-Held Instruments

Related Literature

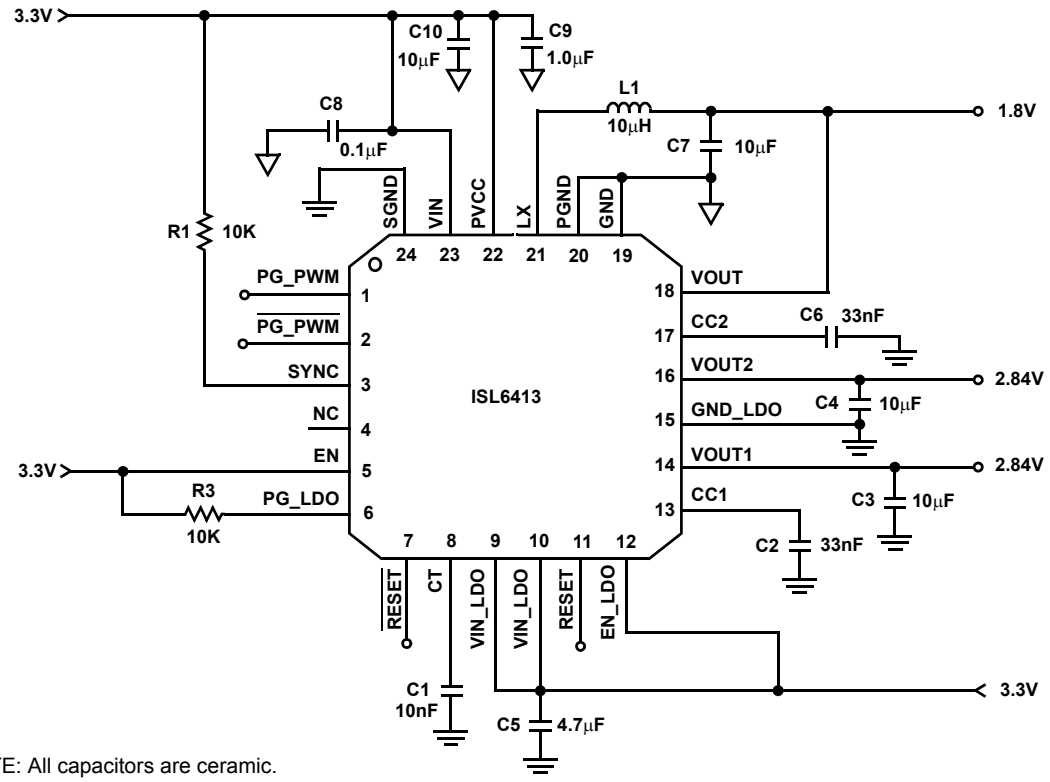
- TB363 - Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)
- TB389 - PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages

Pinout

ISL6413 (QFN)
TOP VIEW

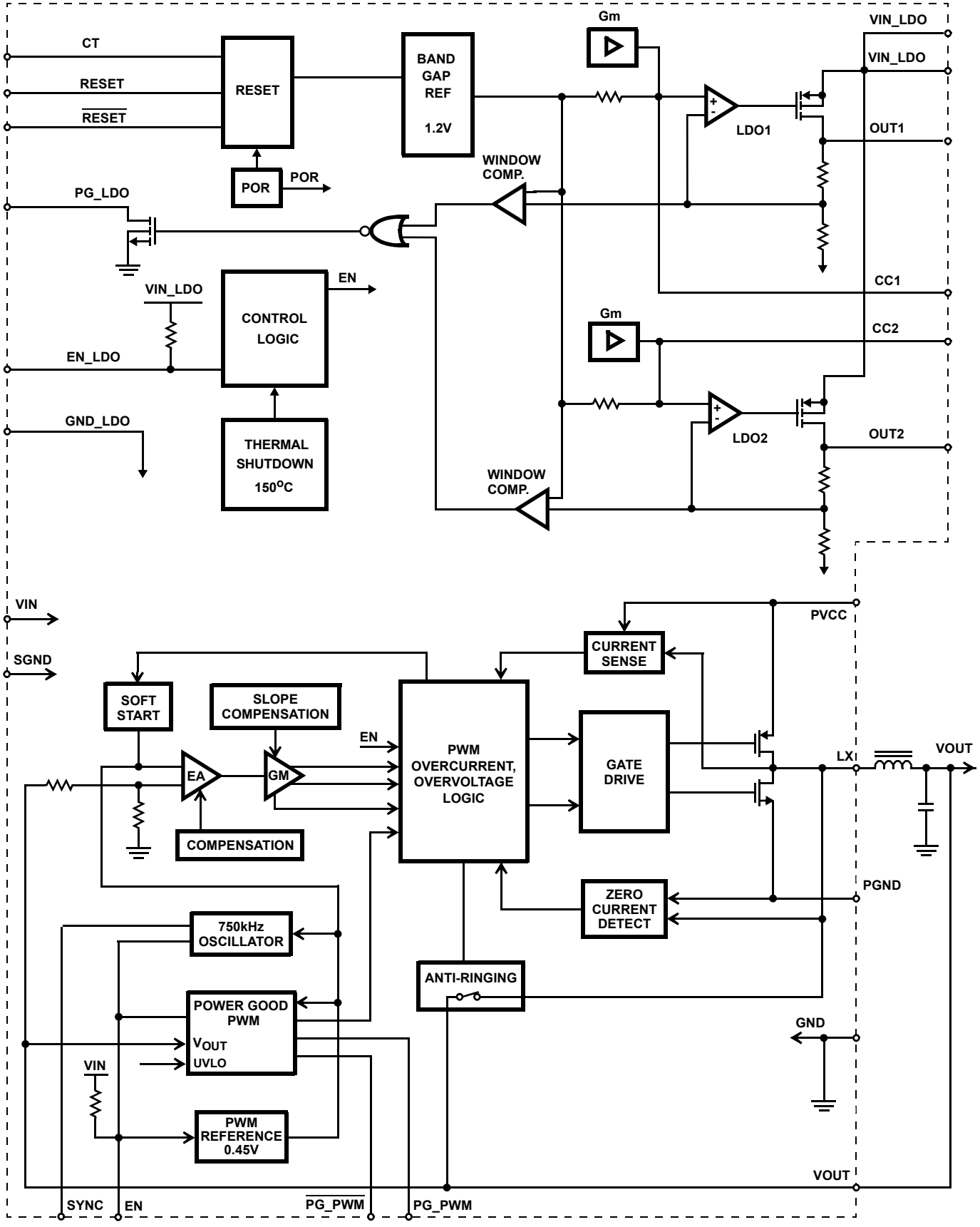


Typical Application Schematic



NOTE: All capacitors are ceramic.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage V_{IN}, PV_{CC}, V_{IN}_LDO . . . . . GND -0.3V to +5.0V
ESD Classification
Human Body Model 3kV
Machine Model . . . . . TBDV

Operating Conditions

Temperature Range
ISL6413I . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 1, 2)	40	5

Maximum Junction Temperature (Plastic Package) -55°C to 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . .300°C
(Lead Tips Only)
Operating Temperature Range
ISL6413IR . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379 for details.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside. See Tech Brief TB379 for details.

Electrical Specifications

Recommended operating conditions unless otherwise noted. V_{IN} = V_{IN}_LDO = PV_{CC} = 3.3V, Compensation Capacitors = 33nF for LDO1 and LDO2. T_A = 25°C. (Note 2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} SUPPLY					
Supply Voltage Range	V_{IN}, PV_{CC}, V_{IN}_LDO	3.0	3.3	3.6	V
Input UVLO Threshold	V_{TR}	2.55	2.62	2.66	V
	V_{TF}	2.5	2.55	2.59	V
Operating Supply Current (Note 3)	Device active, but not switching	-	0.9	1.1	mA
	V_{IN} = V_{IN}_LDO = PV_{CC} = 3.3V f_{SW} = 750kHz, C_{OUT} = 10µF, I_L = 0mA	-	1.9	2.5	mA
Shutdown Supply Current	EN_PWM = EN_LDO = GND, T_A = 25°C	-	15	20	µA
	EN_PWM = EN_LDO = GND, T_A = 85°C	-	20	25	µA
Input Bias Current	EN_PWM = EN_LDO = GND/V_{IN}, T_A = 25°C	-	1.0	1.5	µA
	EN_PWM = EN_LDO = GND/V_{IN}, T_A = 85°C	-	1.5	2.0	µA
Thermal Shutdown Temperature (Note 6)	Rising Threshold	-	150	-	°C
Thermal Shutdown Hysteresis (Note 6)		-	20	25	°C
SYNCHRONOUS BUCK PWM REGULATOR					
Output Voltage		-	1.8	-	V
Output Voltage Accuracy	I_{OUT} = 3mA to 400mA, T_A = -40°C to 85°C	-2.0	-	2.0	%
Line Regulation	I_O = 10mA, V_{IN} = V_{IN}_LDO = PV_{CC} = 3.0V to 3.6V	-0.5	-	0.5	%
Maximum Output Current		400	-	-	mA
Peak Output Current Limit		600	-	900	mA
PMOS $r_{DS(ON)}$	I_{OUT} = 200mA	-	300	-	mΩ
NMOS $r_{DS(ON)}$	I_{OUT} = 200mA	-	225	-	mΩ
Efficiency	I_{OUT} = 200mA, V_{IN} = 3.3V	-	93	-	%
Soft-Start Time	4096 Clock Cycles @ 750kHz	-	5.5	-	ms
OSCILLATOR					
Oscillator Frequency	T_A = -40°C to +85°C	620	750	860	kHz
Frequency Synchronization Range (f_{SYNC})	Clock signal on SYNC pin	500	-	1000	kHz
SYNC High Level Input Voltage		2.3	-	-	V
SYNC Low Level Input Voltage		-	-	1.0	V

Electrical Specifications Recommended operating conditions unless otherwise noted. V_{IN} = $V_{IN_}$LDO = PV_{CC} = 3.3V, Compensation Capacitors = 33nF for LDO1 and LDO2. T_A = 25°C. (Note 2) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Sync Input Leakage Current	SYNC = GND or V_{IN}	-	0.01	0.15	µA
Duty Cycle of External Clock Signal (Note 6)		20	-	80	%
PG_PWM					
Rising Threshold	1mA source/sink	+5.5	8.0	+13	%
Falling Threshold		-11.5	-8.0	-5.5	%
LDO1 SPECIFICATIONS					
Output Voltage		-	2.84	-	V
Output Voltage Accuracy	I_{OUT} = 10mA	-1.5	-	1.5	%
Maximum Output Current (Note 6)	V_{IN} = 3.6V	300	-	-	mA
Output Current Limit (Note 6)		330	770	-	mA
Dropout Voltage (Note 4)	I_{OUT} = 300mA	-	125	200	mV
Line Regulation	V_{IN} = 3.0V to 3.6V, I_{OUT} = 10mA	-0.15	0.0	0.15	%/V
Load Regulation	I_{OUT} = 10mA to 300mA	-0.5	0.2	1.0	%
Output Voltage Noise (Note 6)	10Hz < f < 100kHz, I_{OUT} = 10mA				
	C_{OUT} = 2.2µF	-	65	-	$µV_{RMS}$
	C_{OUT} = 10µF	-	60	-	$µV_{RMS}$
LDO2 SPECIFICATIONS					
Output Voltage		-	2.84	-	V
Output Voltage Accuracy	I_{OUT} = 10mA	-1.5	-	1.5	%
Maximum Output Current (Note 6)	V_{IN} = 3.6V	200	-	-	mA
Output Current Limit (Note 6)		250	400	-	mA
Dropout Voltage (Note 4)	I_{OUT} = 200mA	-	100	200	mV
Line Regulation	V_{IN} = 3.0V to 3.6V, I_{OUT} = 10mA	-0.15	0.0	0.15	%/V
Load Regulation	I_{OUT} = 10mA to 200mA	-	0.2	1.0	%
Output Voltage Noise (Note 6)	10Hz < f < 100kHz, I_{OUT} = 10mA				
	C_{OUT} = 2.2µF	-	30	-	$µV_{RMS}$
	C_{OUT} = 10µF	-	20	-	$µV_{RMS}$
ENABLE (EN_PWM and (EN_LDO)					
EN High Level Input Voltage		2.3	-	-	V
EN Low Level Input Voltage		-	-	1.0	V
RESET BLOCK SPECIFICATIONS					
RESET Rising Threshold		2.68	2.79	2.81	V
RESET Falling Threshold	Sink 1.0mA/Source 0.5mA at 0.4V from GND/V_{DD}	2.7	2.77	2.79	V
RESET Threshold Hysteresis		-	20	-	mV
RESET Current Source		0.4	0.54	0.7	µA
RESET/$\overline{\text{RESET}}$ Active Timeout Period (Note 5)	C_T = 0.01µF	25	-	-	ms
POWER GOOD (PG_LDO)					
PGOOD Threshold (Rising)		+11	+15	+18	%
PGOOD Threshold (Falling)		-17	-15	-11	%
PGOOD Output Voltage Low	I_{OL} = 1mA	-	-	0.5	V

Electrical Specifications Recommended operating conditions unless otherwise noted. V_{IN} = $V_{IN_}$LDO = PV_{CC} = 3.3V, Compensation Capacitors = 33nF for LDO1 and LDO2. T_A = 25°C. (Note 2) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PGOOD Output Leakage Current	V_{OUT} = 3.3V	-	0.01	0.1	µA
PWM OUTPUT OVER VOLTAGE					
Over Voltage Threshold		28	33	38	%

NOTE:

3. Specifications at -40°C and +85°C are guaranteed by design/characterization, not production tested.
4. This is the V_{IN} current consumed when the device is active but not switching. Does not include gate drive current.
5. The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} is 50mV below the value of V_{OUT} for V_{IN} = V_{OUT} + 0.5V.
6. The RESET timeout period is linear with CT at the slope of 2.5ms/nF. Thus, at 10nF (0.01µF) the RESET time is 25ms; at 1000nF (0.1µF) the RESET time would be 250ms.
7. Guaranteed by design, not production tested.

Typical Performance Curves

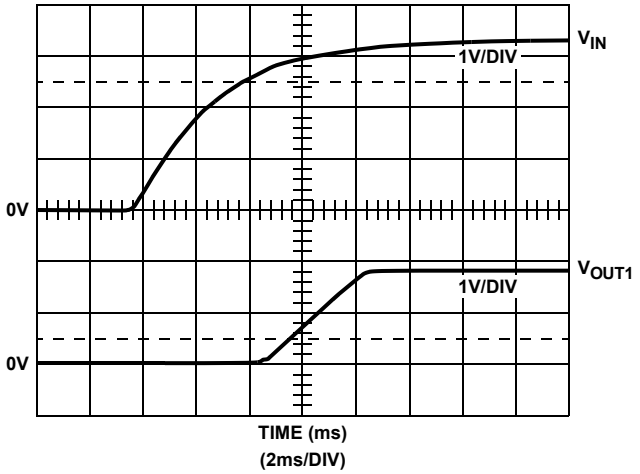


FIGURE 1. PWM SOFTSTART

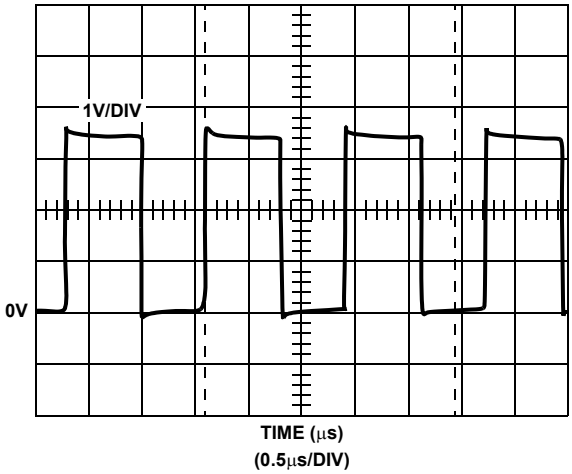


FIGURE 2. PWM PHASE NODE SWITCHING

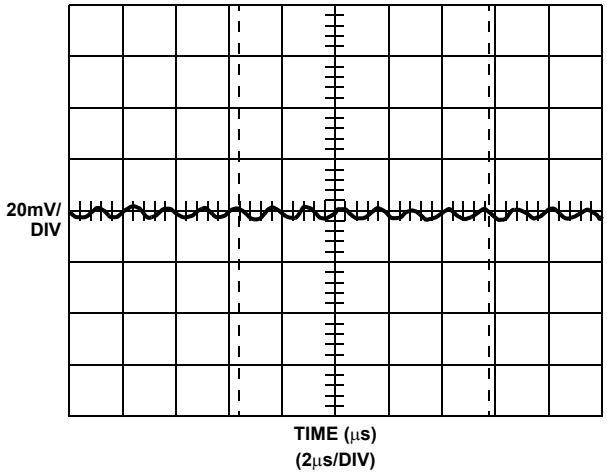


FIGURE 3. PWM OUTPUT RIPPLE WAVEFORMS

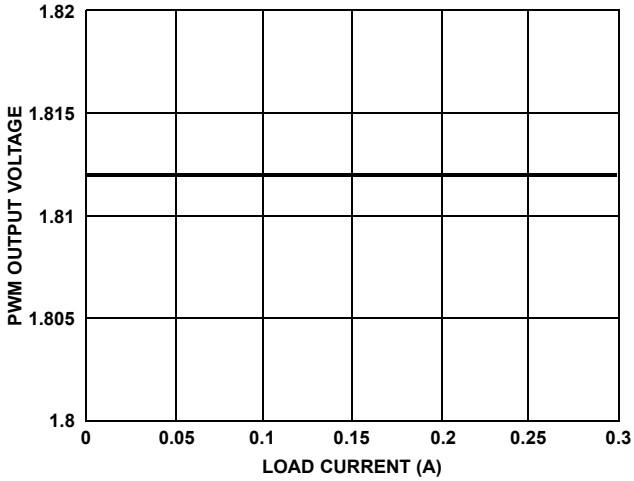


FIGURE 4. PWM LOAD REGULATION

Typical Performance Curves (Continued)

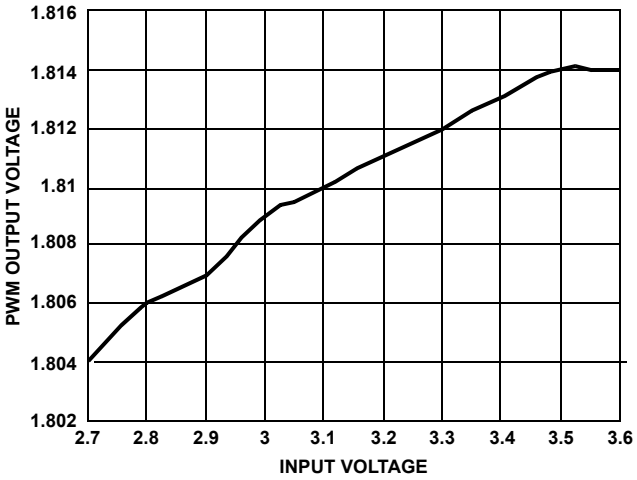


FIGURE 5. PWM LINE REGULATION

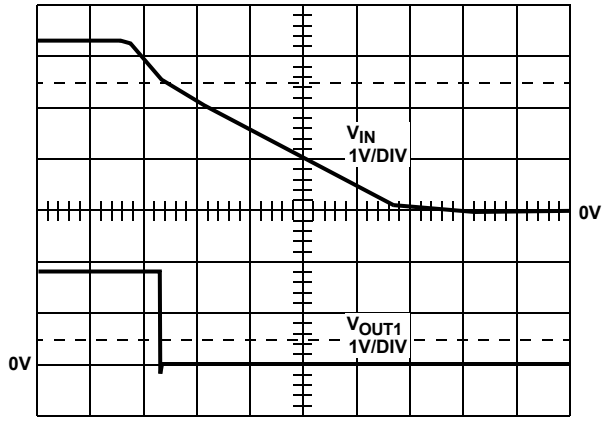


FIGURE 6. PWM SHUTDOWN WITH V_{IN}

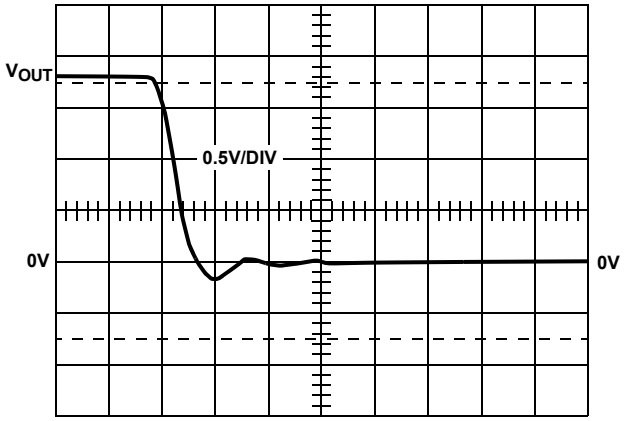


FIGURE 7. PWM SHUTDOWN WITH EN_PWM

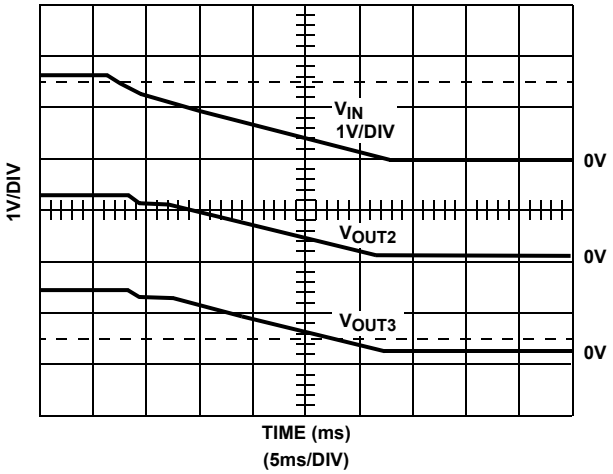


FIGURE 8. LDO SHUTDOWN WITH V_{IN}

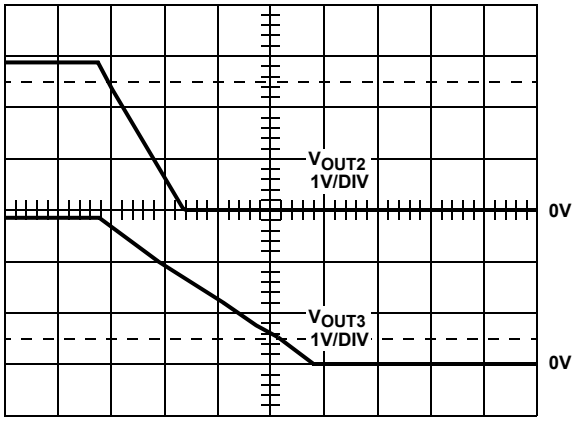


FIGURE 9. LDO SHUTDOWN WITH EN_LDO

Pin Descriptions

PVCC - Positive supply for the power (internal FET) stage of the PWM section.

SGND - Analog ground for the PWM. All internal control circuits are referenced to this pin.

EN _PWM- The PWM controller is enabled when this pin is HIGH, and held off when the pin is pulled LOW. It is a CMOS logic-level input (referenced to V_{IN}).

V_{IN}_LDO - This is the input voltage pin for LDO1 and LDO2.

EN_LDO - LDO1 and LDO2 are enabled when this pin is HIGH, and held off when the pin is pulled LOW. It is a CMOS logic-level input (referenced to V_{IN}).

CT - Timing capacitor connection to set the 25ms minimum pulse width for the RESET/$\overline{\text{RESET}}$ signal.

RESET, $\overline{\text{RESET}}$ - These complementary pins are the outputs of the reset supervisory circuit, which monitors V_{IN}. The IC asserts these RESET and $\overline{\text{RESET}}$ signals whenever the supply voltage drops below a preset threshold; keeping them asserted for at least 25ms after V_{CC} (V_{IN}) has risen above the reset threshold. These outputs are push-pull. $\overline{\text{RESET}}$ is LOW when re-setting the microprocessor. The device will continue to operate until V_{IN} drops below the UVLO threshold.

PG_LDO - This is a high impedance open drain output that provides the status of both LDOs. When either of the outputs are out of regulation, PG_LDO goes LOW.

CC1 - This is the compensation capacitor connection for LDO1. Connect a 0.033µF capacitor from CC1 to GND_LDO.

CC2 - This is the compensation capacitor connection for LDO2. Connect a 0.033µF capacitor from CC2 to GND_LDO.

V_{OUT2} - This pin is the output of LDO2. Bypass with a 2.2µF, low ESR capacitor to GND_LDO for stable operation.

GND_LDO - Ground pin for LDO1 and LDO2.

V_{OUT1} - This pin is the output of LDO1. Bypass with a 2.2µF, low ESR capacitor to GND_LDO for stable operation.

PGND - Power ground for the PWM controller stage.

V_{OUT} - This I/O pin senses the output voltage of the PWM converter stage. For fixed 1.8V operation, connect this pin directly to the output voltage.

PG_PWM - This pin is an active pull-up/pull-down able to source/sink 1mA (min.) at 0.4V from V_{IN}/SGND. This output is HIGH when V_{OUT} is within ±8% (typ.).

$\overline{\text{PG\_PWM}}$ - This pin provides an inverted PG_PWM output.

LX - The LX pin is the switching node of synchronous buck converter, connected internally at the junction point of the upper MOSFET source and lower MOSFET drain. Connect this pin to the output inductor.

V_{IN} - This pin is the power supply for the PWM controller stage and must be closely decoupled to ground.

SYNC - This is the external clock synchronization input. The device can be synchronized to 500kHz to 1MHz switching frequency.

GND - Tie this pin to the ground plane with a low impedance, shortest possible path.

Functional Description

The ISL6413 is a 3-in-1 multi-output regulator designed for wireless chipset power applications. The device integrates a single synchronous buck regulator with dual LDOs. It supplies three fixed output voltages 1.8V, 2.84V and 2.84V. The 1.8V is generated using a synchronous buck regulator with greater then 92% efficiency. Both 2.84V supplies are generated from ultra low noise LDO Regulators. Under voltage lock-out (UVLO) prevents the converter from turning on when the input voltage is less then typically 2.6V

Additional blocks include an output over-current protections, thermal sensor, PGOOD detectors, RESET function and shutdown logic.

Synchronous Buck Regulator

The Synchronous buck regulator with integrated N- and P-channel power MOSFET provides pre-set 1.8V for BBP/MAC core supply. Synchronous rectification with internal MOSFETs is used to achieve higher efficiency and reduced number of external components. Operating frequency is typically 750kHz allowing the use of smaller inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 500kHz to 1MHz. The PG_PWM output indicates loss of regulation on PWM output.

The PWM architecture uses a peak current mode control scheme with internal slope compensation. At the beginning of each clock cycle, the high side P-channel MOSFET is turned on. The current in the inductor ramps up and is sensed via an internal circuit. The error amplifier sets the threshold for the PWM comparator. The high side switch is turned off when the sensed inductor current reaches this threshold. After a minimum dead time preventing shoot through current, the low side N-channel MOSFET will be turned on and the current ramps down again. As the clock cycle is completed, the low side switch will be turned off and the next clock cycle starts.

The control loop is internally compensated reducing the amount of external components. The PWM section includes an anti-ringing switch to reduce noise at light loads.

The switch current is internally sensed and the minimum current limit is 600mA.

Synchronization

The typical operating frequency for the converter is 750kHz if no clock signal is applied to SYNC pin. It is possible to synchronize the converter to an external clock within a frequency range from 500kHz to 1000kHz. The device automatically detects the rising edge of the first clock and will synchronize immediately to the external clock. If the clock signal is stopped, the converter automatically switches back to the internal clock and continues operation without interruption. The switch over will be initiated if no rising edge on the SYNC pin is detected for a duration of two internal 1.3µs clock cycles.

Soft Start

As the EN_PWM (Enable) pin goes high, the soft-start function will generate an internal voltage ramp. This causes the start-up current to slowly rise preventing output voltage overshoot and high inrush currents. The soft-start duration is typically 5.5ms with 750kHz switching frequency. When the soft-start is completed, the error amplifier will be connected directly to the internal voltage reference. The SYNC input is ignored during soft start.

Enable PWM

Logic low on EN_PWM pin forces the PWM section into shutdown. In shutdown all the major blocks of the PWM including power switches, drivers, voltage reference, and oscillator are turned off.

Power Good (PG_PWM)

When chip is enabled, this output is HIGH, when V_{OUT} is within 8% of 1.8V and active low outside this range. When the PWM is disabled, the output is active low. $\overline{PG\_PWM}$ is the complement of PG_PWM.

Leave the PG_PWM pin unconnected when not used.

PWM Overvoltage and Overcurrent Protection

The PWM output current is sampled at the end of each PWM cycle. Should it exceed the overcurrent limit, a 4 bit up/down counter counts up two LSB. Should it not be in overcurrent the counter counts down one LSB (but counter will not "rollover" or count below 0000). If >33% of the PWM cycles go into overcurrent, the counter rapidly reaches count 1111 and the PWM output is shut down and the softstart counter is reset. After 16 clocks the PWM output is enabled and the SS cycle is started.

If V_{OUT} exceeds the overvoltage limit for 32 consecutive clock cycles the PWM output is shut off and the SS counters reset. The softstart cycle will not be started until EN or V_{IN} are toggled.

PG_LDO

PG_LDO is an open drain pulldown NMOS output that will sink 1mA at 0.4V max. It goes to the active low state if either LDO output is out of regulation by more than 15%. When the LDO is disabled, the output is active low.

LDO Regulators

Each LDO consists of a 1.184V reference, error amplifier, MOSFET driver, P-Channel pass transistor, dual-mode comparator and internal feedback voltage divider.

The 1.2V band gap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference to the selected feedback voltage and amplifies the difference. The MOSFET driver reads the error signal and applies the appropriate drive to the P-Channel pass transistor. If the feedback voltage is lower then the reference voltage, the pass transistor gate is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher then the reference voltage, the pass transistor gate is driven higher, allowing less current to pass to the output. The output voltage is fed back through an internal resistor divider connected to V_{OUT1}/V_{OUT2} pins.

Internal P-Channel Pass Transistors

The ISL6413 LDO Regulators features a typical 0.5Ω $R_{ds(ON)}$ P-channel MOSFET pass transistors. This provides several advantages over similar designs using PNP bipolar pass transistors. The P-Channel MOSFET requires no base drive, which reduces quiescent current considerably. PNP based regulators waste considerable current in dropout when the pass transistor saturates. They also use high base drive currents under large loads. The ISL6413 does not suffer from these problems.

Integrated RESET for MAC/ Baseband Processors

The ISL6413 includes a microprocessor supervisory block. This block eliminates the extra RESET IC and external components needed in wireless chipset applications. This block performs a single function; it asserts a RESET signal whenever the V_{IN} supply voltage decreases below a preset threshold, keeping it asserted for a programmable time (set by external capacitor CT) after the V_{IN} pin voltage has risen above the RESET threshold.

The push pull output stage of the reset circuit provides both an active-Low and an active-HIGH output. The RESET threshold for ISL6413 is 2.630V typical.

UVLO Reset threshold is always lower then RESET. This insures that as V_{IN} falls, reset goes low before LDOs and PWM are shuts off.

Output Voltages

The ISL6413 provides fixed output voltages for use in Wireless Chipset applications. Internal trimmed resistor networks set the typical output voltages as shown here:

V_{OUT_PWM} = 1.8V; V_{OUT1} = 2.84V; V_{OUT2} = 2.84V.

Integrator Circuitry

The ISL6413 LDO Regulators uses an external 33nF compensation capacitor for minimizing load and line regulation errors and for lowering output noise. When the output voltage shifts due to varying load current or input

voltage, the integrator capacitor voltage is raised or lowered to compensate for the systematic offset at the error amplifier. Compensation is limited to ±5% to minimize transient overshoot when the device goes out of dropout, current limit, or thermal shutdown.

Shutdown

Driving the EN_LDO pin low will put LDO1 and LDO2 into the shutdown mode. Driving the EN_PWM pin low will put the PWM into shutdown mode. Pulling the EN_PWM and EN_LDO both pins low simultaneously, puts the complete chip into shutdown mode, and supply current drops to 15µA typical.

Protection Features for the LDOs

Current Limit

The ISL6413 monitors and controls the pass transistor's gate voltage to limit the output current. The current limit for LDO1 is 330mA and LDO2 is 250mA. The output can be shorted to ground without damaging the part due to the current limit and thermal protection features.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the ISL6413. When the junction temperature (T_J) exceeds +150°C, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistor and allowing the IC to cool. The pass transistor turns on again after the IC's junction temperature typically cools by 20°C, resulting in a pulsed output during continuous thermal overload conditions. Thermal overload protection protects the ISL6413 against fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of +150°C.

Operating Region and Power Dissipation

The maximum power dissipation of ISL6413 depends on the thermal resistance of the IC package and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipated in the device is:

PT = P1 + P2 + P3, where

$P1 = I_{OUT1} \times V_{OUT1}/I_{IN} \times V_{IN}$

$P2 = I_{OUT2} (V_{IN} - V_{OUT2})$

$P3 = I_{OUT3} (V_{IN} - V_{OUT3})$

The maximum power dissipation is:

$Pmax = (Tjmax - T_A)/\theta JA$

Where Tjmax = 150°C, T_A = ambient temperature, and θJA is the thermal resistance from the junction to the surrounding environment.

The ISL6413 package features an exposed thermal pad on its underside. This pad lowers the thermal resistance of the package by providing a direct heat conduction path from the die to the PC board. Additionally, the ISL6413's ground (GND_LDO and PGND) performs the dual function of providing an electrical connection to system ground and channeling heat away. Connect the exposed backside pad direct to the GND_LDO ground plane.

Applications Information

LDO Regulator Capacitor Selection and Regulator Stability

Capacitors are required at the ISL6413 LDO Regulators' input and output for stable operation over the entire load range and the full temperature range. Use >1µF capacitor at the input of LDO Regulators, V_{IN}_LDO pins. The input capacitor lowers the source impedance of the input supply. Larger capacitor values and lower ESR provides better PSRR and line transient response. The input capacitor must be located at a distance of not more then 0.5 inches from the V_{IN} pins of the IC and returned to a clean analog ground. Any good quality ceramic capacitor can be used as an input capacitor.

The output capacitor must meet the requirements of minimum amount of capacitance and ESR for both LDO's. The ISL6413 is specifically designed to work with small ceramic output capacitors. The output capacitor's ESR affects stability and output noise. Use an output capacitor with an ESR of 50mΩ or less to insure stability and optimum transient response. For stable operation, a ceramic capacitor, with a minimum value of 3.3µF, is recommended for V_{OUT1} for 300mA output current, and 3.3µF is recommended for V_{OUT2} at 200mA load current. There is no upper limit to the output capacitor value. Larger capacitor can reduce noise and improve load transient response, stability and PSRR. Higher value of output capacitor (10µF) is recommended for LDO2 when used to power VCO circuitry in wireless chipsets. The output capacitor should be located very close to V_{OUT} pins to minimize impact of PC board inductances and the other end of the capacitor should be returned to a clean analog ground.

PWM Regulator Component Selection

INDUCTOR SELECTION

A 10µH minimum output inductor is used with the ISL6413 PWM section. Values larger then 15µH or less then 10µH may cause stability problems because of the internal compensation of the regulator. The important parameters of the inductor that need to be considered are the current rating of the inductor and the DC resistance of the inductor. The dc resistance of the inductor will influence directly the efficiency of the converter. Therefore, an inductor with lowest dc resistance should be selected for highest efficiency.

In order to avoid saturation of the inductor, the inductor should be rated at least for the maximum output current plus the inductor ripple current.

TABLE 1. RECOMMENDED INDUCTORS

OUTPUT CURRENT	INDUCTOR VALUE	VENDOR PART #	COMMENTS
0mA to 600mA	10µH	Coilcraft DO3316P-103 Coilcraft DT3316P-103 Sumida CDR63B-100 Sumida CDRH5D28-100	High Efficiency
		Coilcraft DO1608C-100 Sumida CDRH4D28-100	Smallest Solution
0mA to 300mA	10µH	Coilcraft DS1608C-103	High Efficiency
		Murata LQH4C100K04	Smallest Solution

OUTPUT CAPACITOR SELECTION

For best performance, a low ESR output capacitor is needed. If an output capacitor is selected with an ESR value ≤120mΩ, its RMS ripple current rating will always meet the application requirements. The RMS ripple current is calculated as:

$$I_{RMS(C)_O} = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}}$$

The overall output ripple voltage is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charge and discharging the output capacitor:

$$\Delta V_O = V_O \times \left(\frac{1 - \frac{V_O}{V_I}}{L \times f} \right) \times \left(\frac{1}{8 \times C_O \times f} + ESR \right)$$

Where the highest output voltage ripple occurs at the highest input voltage VI.

TABLE 2. RECOMMENDED CAPACITORS

CAPACITOR VALUE	ESR/mΩ	VENDOR PART #	COMMENTS
10µF	50	Taiyo Yuden JMK316BJ106KL	Ceramic
47µF	100	Sanyo 6TPA47M	POSCAP
68µF	100	Sprague 594D686X0010C2T	Tantalum

INPUT CAPACITOR SELECTION

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes.

The input capacitor should have a minimum value of 10µF and can be increased without any limit for better input voltage filtering. The input capacitor should be rated for the maximum input ripple current calculated as:

$$I_{RMS} = I_{O(max)} \times \sqrt{\frac{V_O}{V_I} \times \left(1 - \frac{V_O}{V_I}\right)}$$

The worst case RMS ripple current occurs at D = 0.5.

Ceramic capacitors show good performance because of their low ESR value, and because they are less sensitive to voltage transients, compared to tantalum capacitors.

Place the input capacitor as close as possible to the input pin of the IC for best performance.

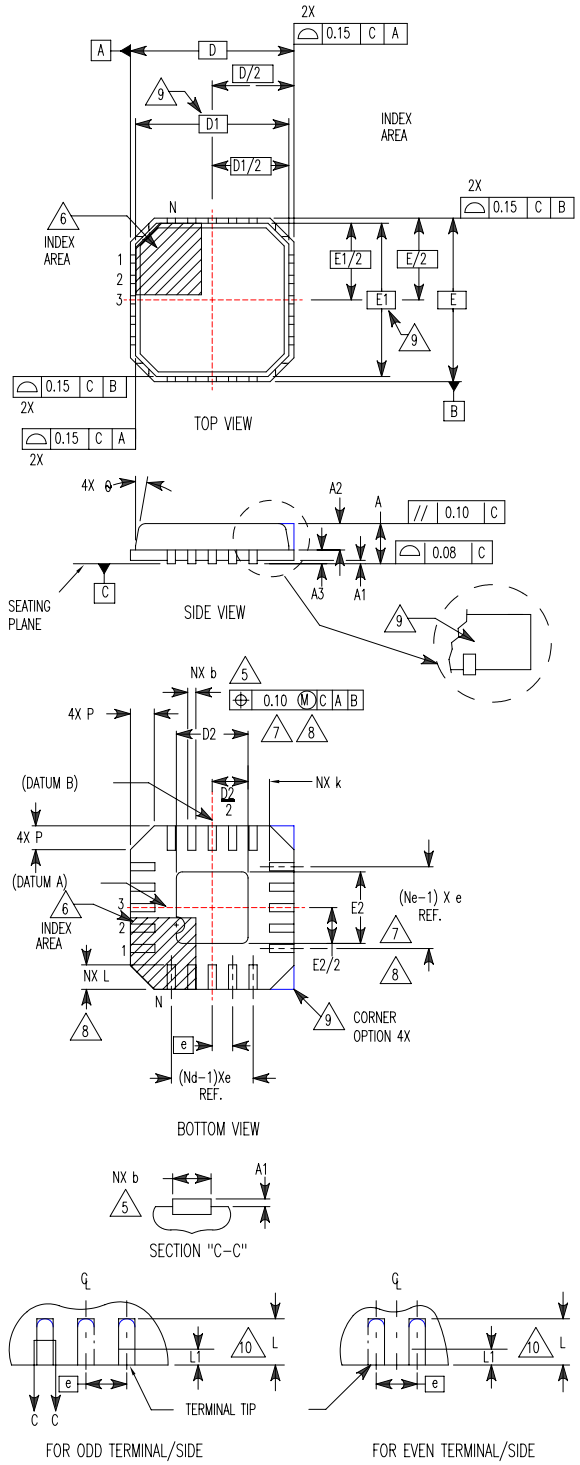
Layout Considerations

As for all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. Use a common ground node to minimize the effects of ground noise.

Allocate two board levels as ground planes, with many vias between them to create a low impedance, high-frequency plane. Tie all the device ground pins through multiple vias each to this ground plane, as close to the device as possible. Also tie the exposed pad on the bottom of the device to this ground plane.

Refer to application note AN1081.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L24.4x4B

24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VGGD-2 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	2.19	2.34	2.49	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	2.19	2.34	2.49	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		24		2
Nd		6		3
Ne		6		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 0 10/03

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.