DATA SHEET

74LV14
Hex inverting Schmitt-trigger

Product specification
Supersedes data of 1997 Feb 03
IC24 Data Handbook

1998 Apr 20

Philips
Semiconductors

Hex inverting Schmitt-trigger 74LV14

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for Low Voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- Output capability: standard
- I_{CC} category: SSI

APPLICATIONS

- Wave and pulse shapers for highly noisy environments

DESCRIPTION

The 74LV14 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT14.

The 74LV14 provides six inverting buffers with Schmitt-trigger action. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nY	C_L = 15 pF; V_{CC} = 3.3 V	13	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	See Notes 1 and 2	15	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV14 N	74LV14 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV14 D	74LV14 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV14 DB	74LV14 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV14 PW	74LV14PW DH	SOT402-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A – 6A	Data inputs
2, 4, 6, 8, 10, 12	1Y – 6Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

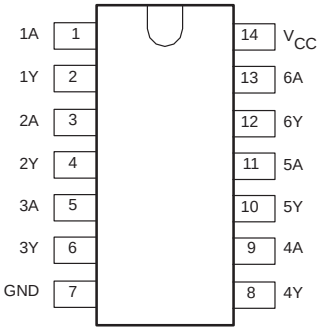
FUNCTION TABLE

INPUT	OUTPUT
nA	**nY**
L	H
H	L

NOTES:

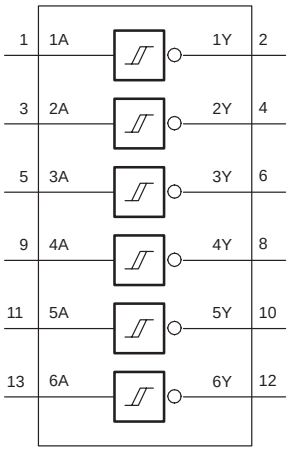
H = HIGH voltage level
L = LOW voltage level

PIN CONFIGURATION



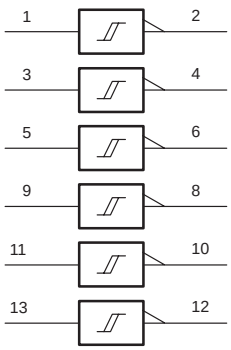
SV00396

LOGIC SYMBOL



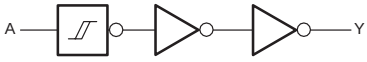
SV00424

LOGIC SYMBOL (IEEE/IEC)



SV00425

LOGIC DIAGRAM



SV00426

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C

NOTE:

1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < –0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < –0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$–0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{OH}	HIGH level output voltage; all outputs	$V_{CC} = 1.2V$; $V_I = V_{IH}$ or V_{IL}; $–I_O = 100\mu A$		1.2				V
		$V_{CC} = 2.0V$; $V_I = V_{IH}$ or V_{IL}; $–I_O = 100\mu A$	1.8	2.0		1.8		
		$V_{CC} = 2.7V$; $V_I = V_{IH}$ or V_{IL}; $–I_O = 100\mu A$	2.5	2.7		2.5		
		$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL}; $–I_O = 100\mu A$	2.8	3.0		2.8		
		$V_{CC} = 4.5V$; $V_I = V_{IH}$ or V_{IL}; $–I_O = 100\mu A$	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL}; $–I_O = 6mA$	2.40	2.82		2.20		V
		$V_{CC} = 4.5V$; $V_I = V_{IH}$ or V_{IL}; $–I_O = 12mA$	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	$V_{CC} = 1.2V$; $V_I = V_{IH}$ or V_{IL}; $I_O = 100\mu A$		0				V
		$V_{CC} = 2.0V$; $V_I = V_{IH}$ or V_{IL}; $I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 2.7V$; $V_I = V_{IH}$ or V_{IL}; $I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL}; $I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 4.5V$; $V_I = V_{IH}$ or V_{IL}; $I_O = 100\mu A$		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL}; $I_O = 6mA$		0.25	0.40		0.50	V
		$V_{CC} = 4.5V$; $V_I = V_{IH}$ or V_{IL}; $I_O = 12mA$		0.35	0.55		0.65	
I_I	Input leakage current	$V_{CC} = 5.5V$; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; SSI	$V_{CC} = 5.5V$; $V_I = V_{CC}$ or GND; $I_O = 0$			20.0		40	µA
ΔI_{CC}	Additional quiescent supply current	$V_{CC} = 2.7V$ to $3.6V$; $V_I = V_{CC} – 0.6V$			500		850	µA

NOTE:
1. All typical values are measured at $T_{amb} = 25°C$.

TRANSFER CHARACTERISTICS

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		–40 TO +85			–40 TO +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MIN.			
V_{T+}	Positive-going threshold	–	0.70	–	–	–	V	1.2	Figure 1 and 2
		0.8	1.10	1.4	0.8	1.4		2.0	
		1.0	1.45	2.0	1.0	2.0		2.7	
		1.2	1.60	2.2	1.2	2.2		3.0	
		1.5	1.95	2.4	1.5	2.4		3.6	
		1.7	2.50	3.15	1.7	3.15		4.5	
		2.1	3.00	3.85	2.1	3.85		5.5	
V_{T-}	Negative-going threshold	–	0.34	–	–	–	V	1.2	Figure 1 and 2
		0.3	0.65	0.9	0.3	0.9		2.0	
		0.4	0.90	1.4	0.4	1.4		2.7	
		0.6	1.05	1.5	0.6	1.5		3.0	
		0.8	1.30	1.8	0.8	1.8		3.6	
		0.9	1.60	2.0	0.9	2.0		4.5	
		1.1	2.00	2.6	1.1	2.6		5.5	
V_H	Hysteresis ($V_{T+} - V_{T-}$)	–	0.30	–	–	–	V	1.2	Figure 1 and 2
		0.2	0.55	0.8	0.2	0.8		2.0	
		0.3	0.60	1.1	0.3	1.1		2.7	
		0.4	0.65	1.2	0.4	1.2		3.0	
		0.4	0.70	1.2	0.4	1.2		3.6	
		0.4	0.80	1.4	0.4	1.4		4.5	
		0.6	1.00	1.5	0.6	1.5		5.5	

NOTES:
1. All typical values are measured at T_{amb} = 25°C
2. The V_{IH} and V_{IL} from the DC family characteristics are superseded by the V_{T+} and V_{T-}.

AC CHARACTERISTICS

GND = 0V; $t_r \leq t_f$ = 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
$t_{PHL/PLH}$	Propagation delay nA to nY	Figure 6	1.2		80				ns
			2.0		27	37		48	
			2.7		20	28		35	
			3.0 to 3.6		15[2]	22		28	
			4.5 to 5.5			18		23	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.

TRANSFER CHARACTERISTIC WAVEFORMS

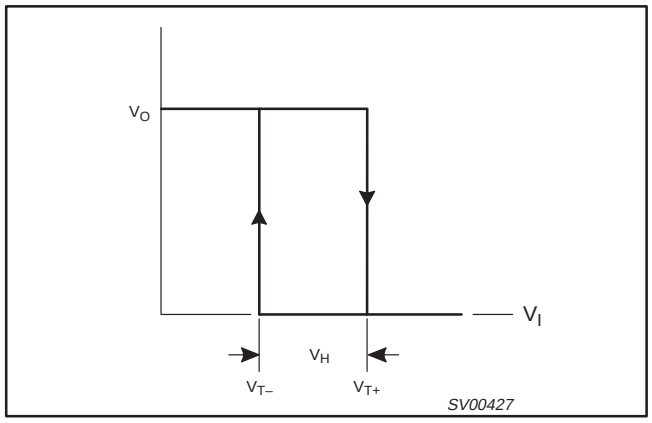


Figure 1. Transfer characteristic.

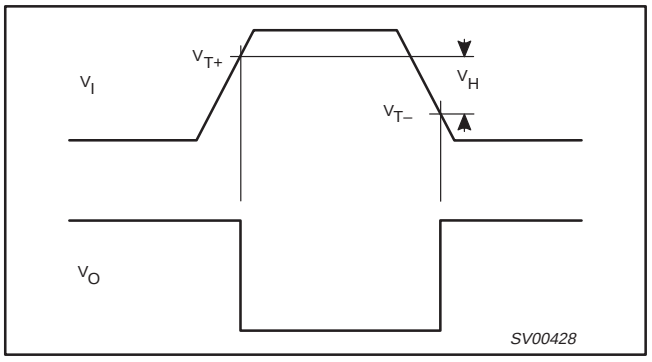


Figure 2. Definition of v_{T+}, V_{T-} and V_H; where V_{T+} and V_{T-} are between limits of 20% and 70%

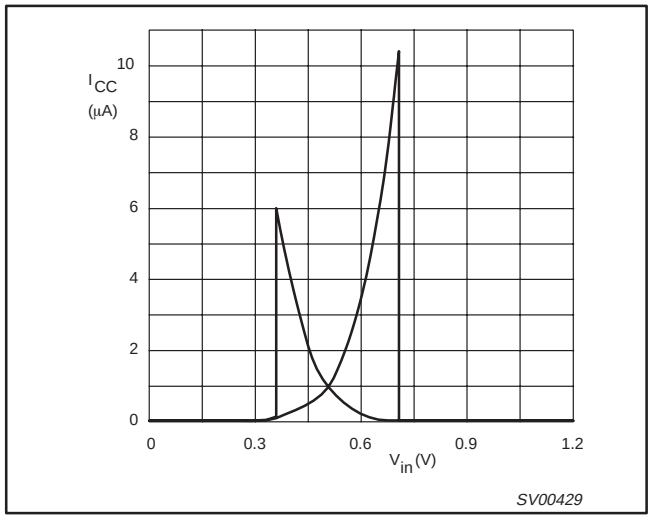


Figure 3. Typical 74LV14 transfer characteristics; V_{CC} = 1.2V.

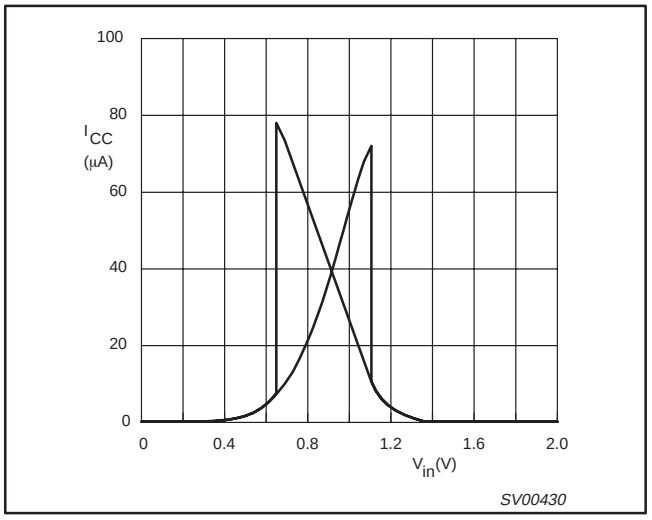


Figure 4. Typical 74LV14 transfer characteristics; V_{CC} = 2.0V.

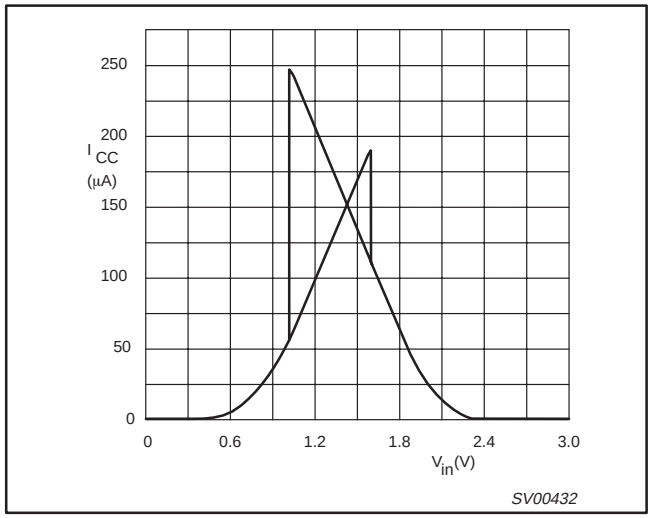


Figure 5. Typical 74LV14 transfer characteristics; V_{CC} = 3.0V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

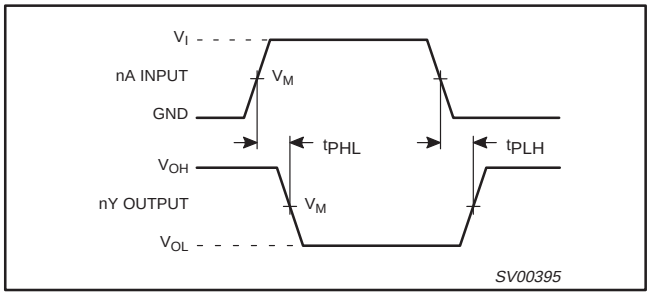


Figure 6. Input (nA) to output (nY) propagation delays.

APPLICATION INFORMATION

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$P_{ad} = f_i \times (t_r \times I_{CCa} + t_f \times I_{CCa}) \times V_{CC}$.

Where:

P_{ad} = additional power dissipation (μW)
f_i = input frequency (MHz)
t_r = input rise time (ns); 10% – 90%
t_f = input fall time (ns); 10% – 90%
I_{CCa} = average additional supply current (μA)

Average I_{CCa} differs with positive or negative input transitions, as shown in Figure 7.

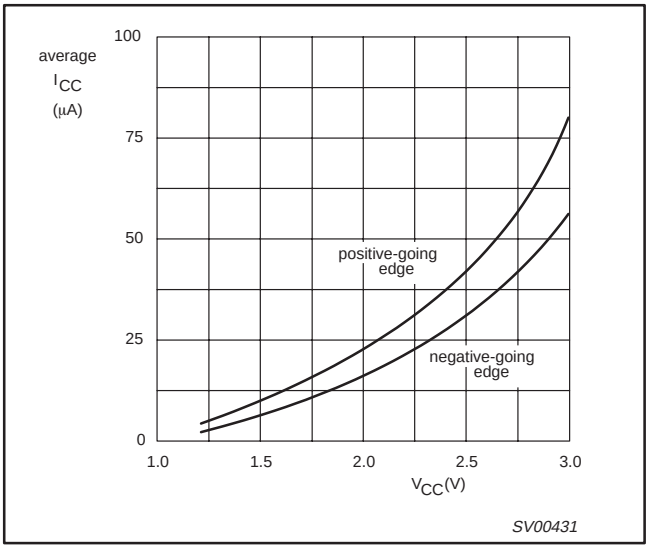


Figure 7. Average I_{CC} for LV Schmitt-trigger devices; linear change of V_I between 0.1 V_{CC} to 0.9 V_{CC}.

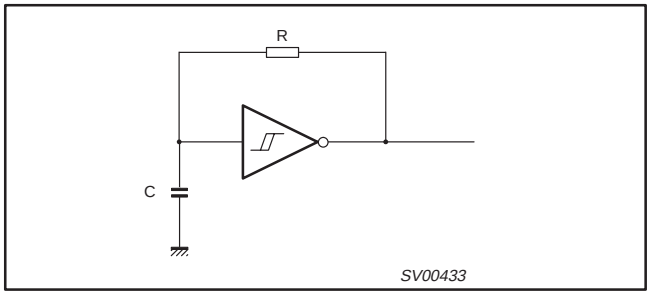


Figure 8. Relaxation oscillator using the LV14.

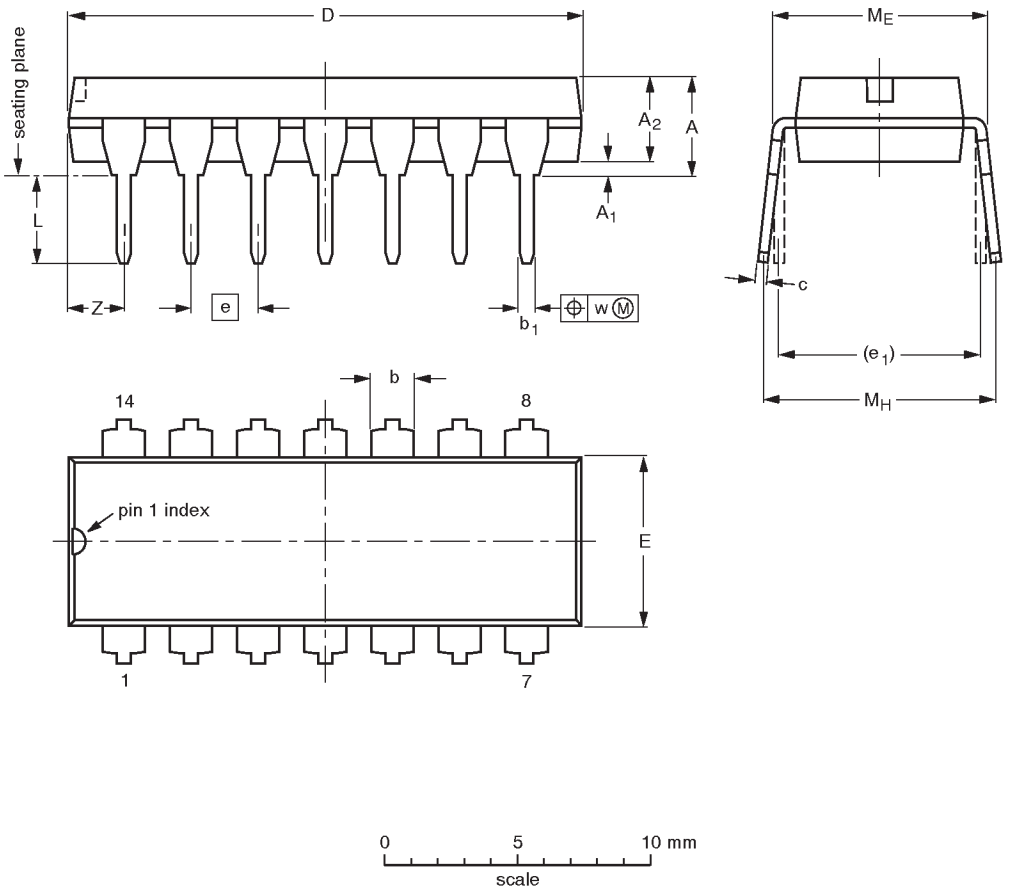
Note to application information:

All values given are typical unless otherwise specified.

Note to Figure 8

$$f = \frac{1}{T} \approx \frac{1}{0.8 \times RC}$$

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

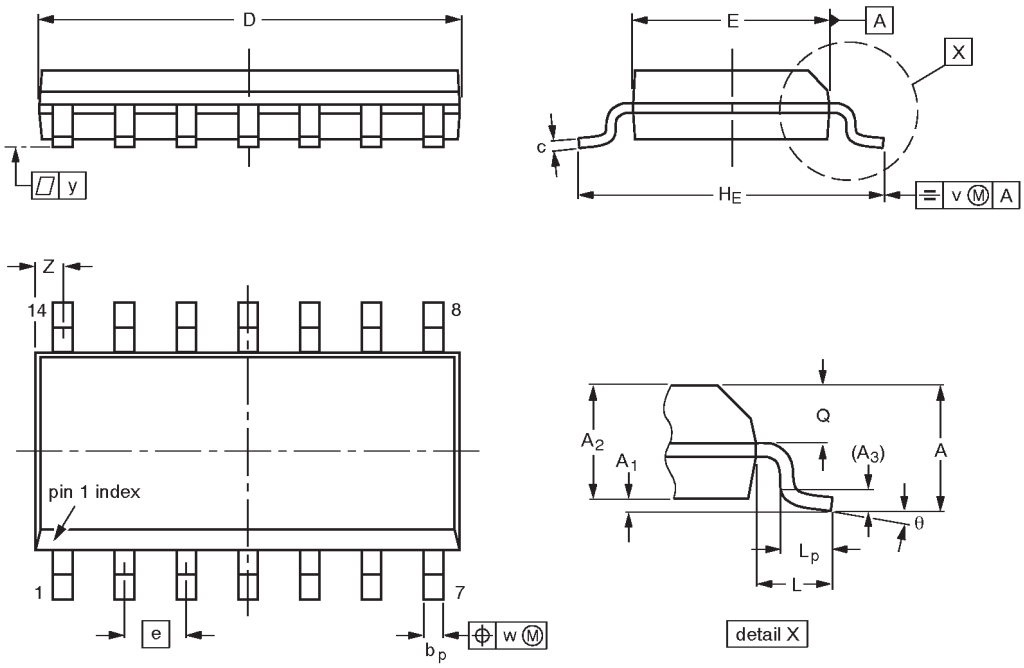
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

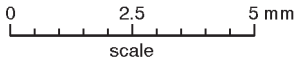
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

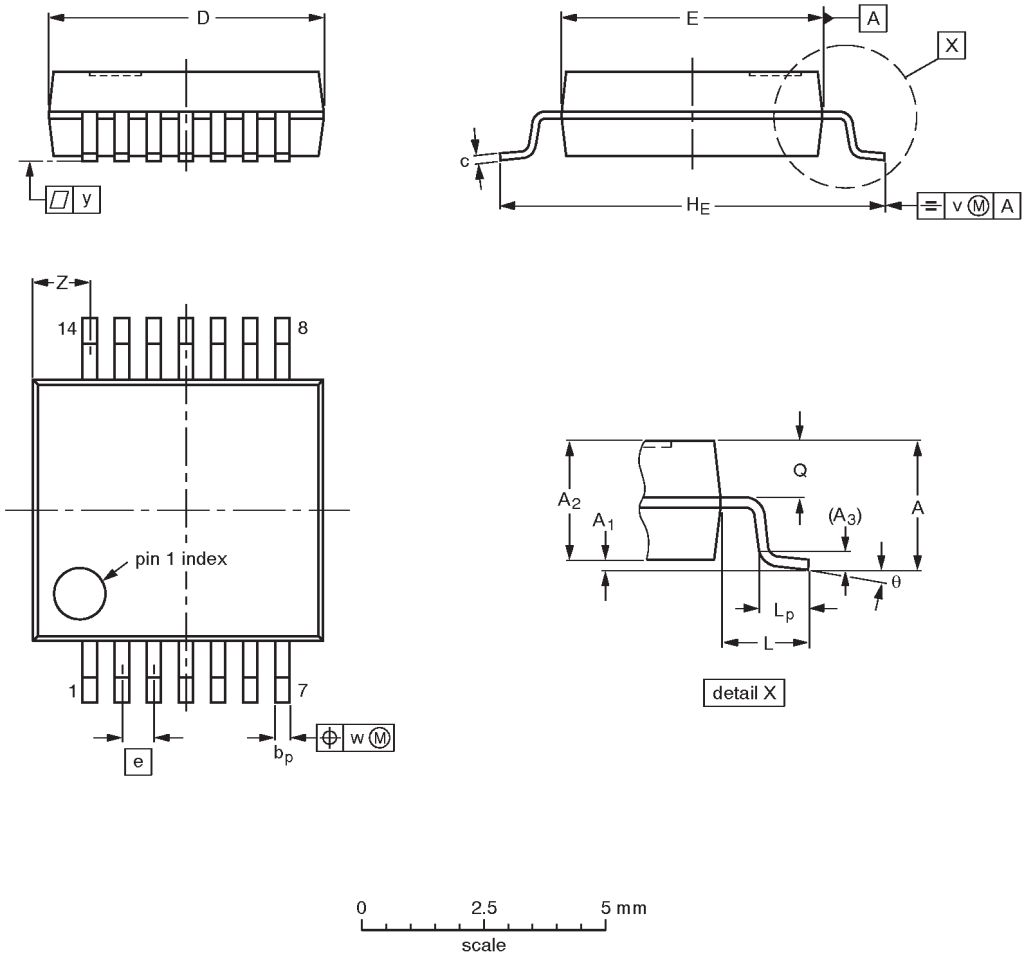
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~91-08-13~~ 95-01-23

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

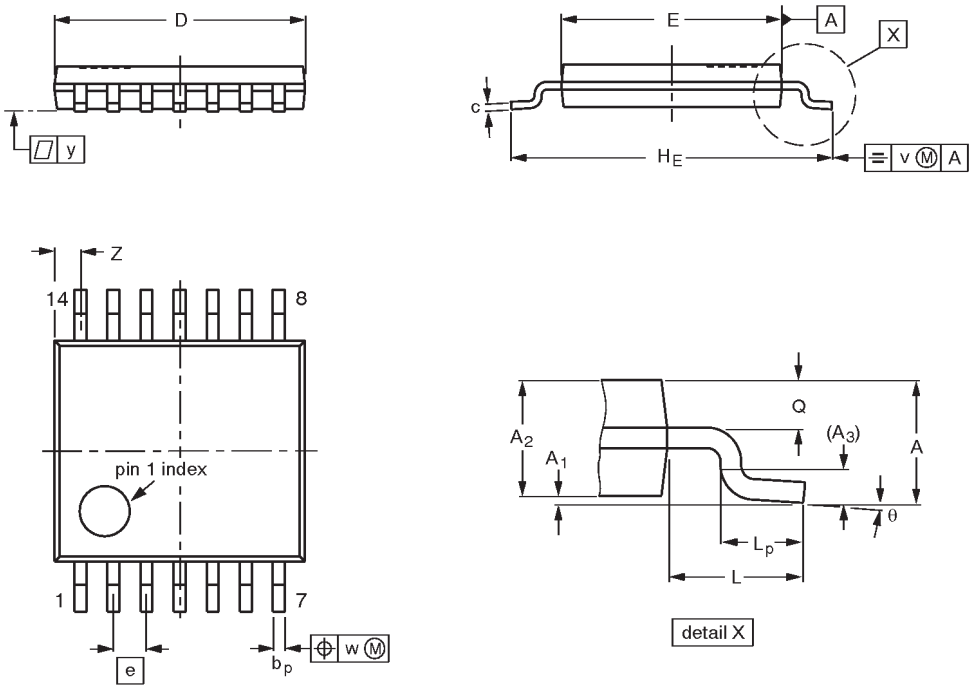
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

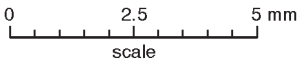
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				~~95-02-04~~ 96-01-18

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				~~94-07-12~~ 95-04-04

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

print code Date of release: 05-96

Document order number: 9397-750-04409

Let's make things better.

Philips Semiconductors

PHILIPS