

# MOS FIELD EFFECT TRANSISTOR $\mu$ PA2717GR

# SWITCHING P-CHANNEL POWER MOS FET

#### **DESCRIPTION**

The  $\mu$ PA2717GR is P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Li-ion battery protection circuit.

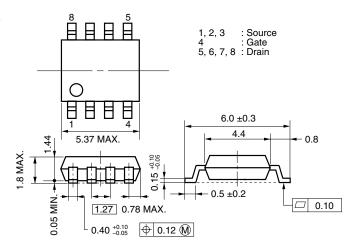
#### **FEATURES**

- Low on-state resistance
  - $R_{DS(on)1}$  = 5.5 m $\Omega$  MAX. (V<sub>GS</sub> = -10 V, I<sub>D</sub> = -7.5 A)
  - $R_{DS(on)2} = 8.9 \text{ m}\Omega \text{ MAX.} \text{ (Vgs = -4.5 V, ID = -7.5 A)}$
- Low Ciss: Ciss = 3550 pF TYP.
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

#### ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2717GR	Power SOP8

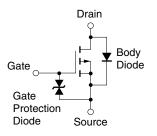
#### PACKAGE DRAWING (Unit: mm)



#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	VDSS	-30	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	Vgss	∓20	V
Drain Current (DC)	$I_{D(DC)}$	∓15	Α
Drain Current (pulse) Note1	ID(pulse)	∓150	Α
Total Power Dissipation Note2	P <sub>T1</sub>	2	W
Total Power Dissipation Note3	P <sub>T2</sub>	2	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to + 150	°C
Single Avalanche Current Note4	las	<b>–</b> 15	Α
Single Avalanche Energy Note4	Eas	22.5	mJ

#### **EQUIVALENT CIRCUIT**



- **Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%
  - 2. Mounted on ceramic substrate of 1200 mm<sup>2</sup> x 2.2 mm
  - 3. Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm, PW = 10 sec
  - **4.** Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = -15 V, R<sub>G</sub> = 25  $\Omega$ , L = 100  $\mu$ H, V<sub>GS</sub> = -20  $\rightarrow$  0 V

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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#### **ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)**

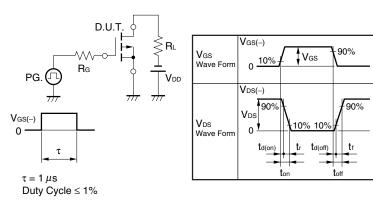
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V			-1	μΑ
Gate Leakage Current	Igss	V <sub>GS</sub> = ∓20 V, V <sub>DS</sub> = 0 V			∓10	μΑ
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-1.0		-2.5	V
Forward Transfer Admittance Note	y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -7.5 A	13			S
Drain to Source On-state Resistance Note	RDS(on)1	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -7.5 A		4.7	5.5	mΩ
	RDS(on)2	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -7.5 A		6.1	8.9	mΩ
	RDS(on)3	V <sub>GS</sub> = -4.0 V, I <sub>D</sub> = -7.5 A		6.9	10.4	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = -10 V		3550		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V		1260		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		600		pF
Turn-on Delay Time	t <sub>d(on)</sub>	$V_{DD} = -15 \text{ V}, I_D = -7.5 \text{ A}$		17		ns
Rise Time	tr	V <sub>GS</sub> = -10 V		32		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		920		ns
Fall Time	tf			510		ns
Total Gate Charge	QG	V <sub>DD</sub> = -24 V		130		nC
Gate to Source Charge	Qgs	V <sub>GS</sub> = -10 V		11		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = -15 A		36		nC
Body Diode Forward Voltage Note	V <sub>F(S-D)</sub>	I <sub>F</sub> = 15 A, V <sub>GS</sub> = 0 V		0.82		V
Reverse Recovery Time	trr	I <sub>F</sub> = 15 A, V <sub>GS</sub> = 0 V		500		ns
Reverse Recovery Charge	Qrr	di/dt = 50 A/μs		1320		nC

Note Pulsed

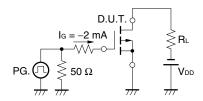
#### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

# $R_{G} = 25 \Omega$ $V_{GS} = -20 \rightarrow 0 V$ $V_{DD}$ $V_{DD}$

#### TEST CIRCUIT 2 SWITCHING TIME

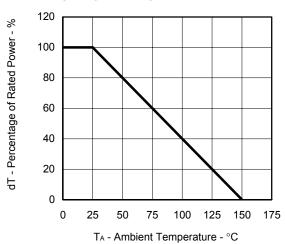


#### **TEST CIRCUIT 3 GATE CHARGE**

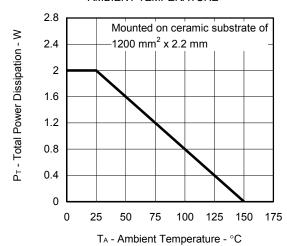


#### TYPICAL CHARACTERISTICS (TA = 25°C)

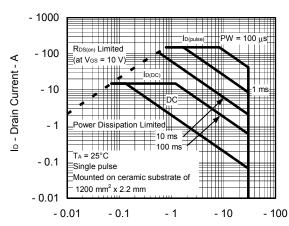
# DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



# TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

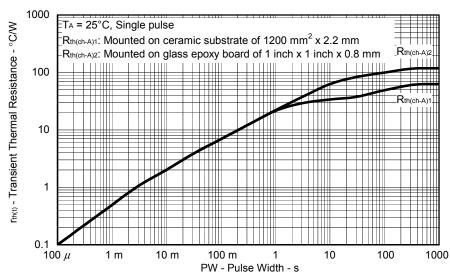


#### FORWARD BIAS SAFE OPERATING AREA



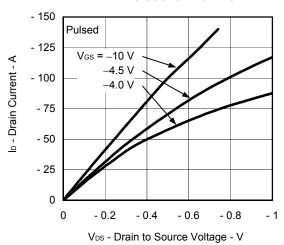
#### VDS - Drain to Source Voltage - V

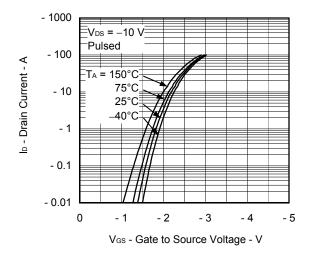
#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



3

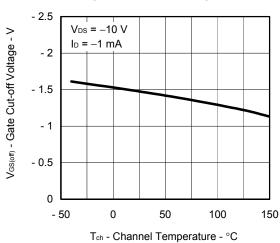
## DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



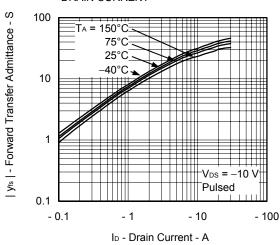


FORWARD TRANSFER CHARACTERISTICS

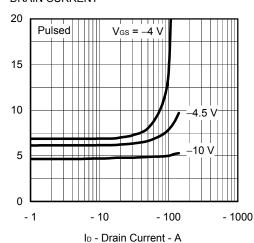
# GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



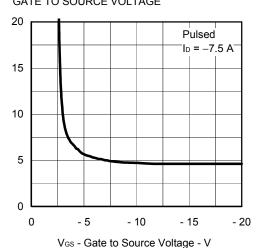
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



# DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

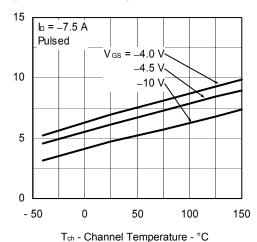


RDS(m) - Drain to Source On-state Resistance - m\Omega

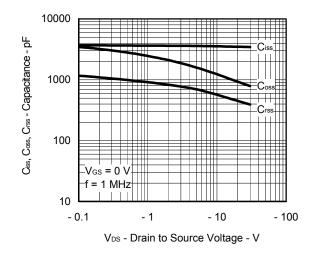
R<sub>DS(m)</sub> - Drain to Source On-state Resistance - mΩ

RDS(m) - Drain to Source On-state Resistance - m\Omega

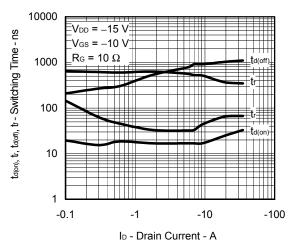
# DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



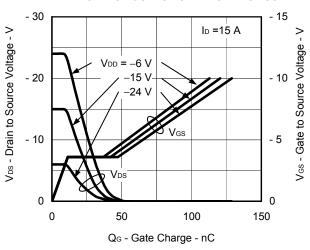
#### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



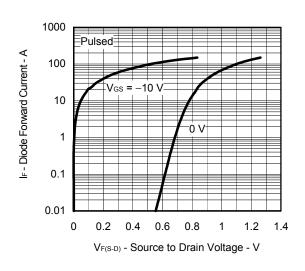
#### **SWITCHING CHARACTERISTICS**



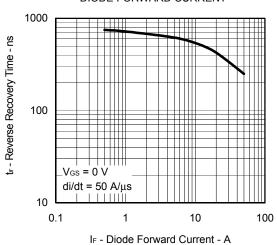
#### DYNAMIC INPUT/OUTPUT CHARACTERISTICS



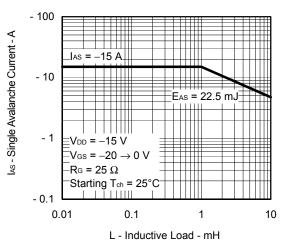
#### SOURCE TO DRAIN DIODE FORWARD VOLTAGE



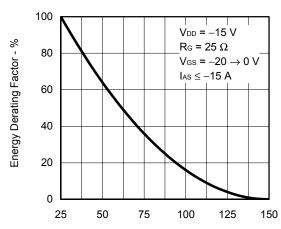
## REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



# SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



# SINGLE AVALANCHE ENERGY DERATING FACTOR



Starting Tch - Starting Channel Temperature - °C

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