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MOTOROLA

MC10319

High Speed 8-Bit Analog-to-Digital Converter

The MC10319 is an 8–bit high speed parallel flash A/D converter. The device employs an internal Grey Code structure to eliminate large output errors on fast slewing input signals. It is fully TTL compatible, requiring a + 5.0 V supply and a wide tolerance negative supply of – 3.0 to – 6.0 V. Three–state TTL outputs allow direct drive of a data bus or common I/O memory.

The MC10319 contains 256 parallel comparators across a precision input reference network. The comparator outputs are fed to latches and then to an encoder network, to produce an 8–bit data byte plus an overrange bit. The data is latched and converted to 3–state LS–TTL outputs. The overrange bit is always active to allow for either sensing of the overrange condition or ease of interconnecting a pair of devices to produce a 9–bit A/D converter.

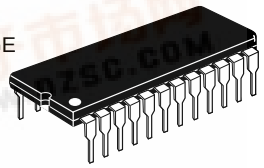
Applications include video display and radar processing, high speed instrumentation and TV broadcast encoding.

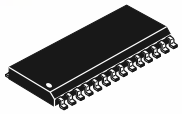
- Internal Grey Code for Speed and Accuracy, Binary Outputs
- 8–Bit Resolution/9–Bit Typical Accuracy
- Easily Interconnected for 9–Bit Conversion
- 3–State LS–TTL Outputs with True/Complement Enable Inputs
- 25 MHz Sampling Rate
- Wide Input Range: 1.0 to 2.0 V_{pp}, between ± 2.0 V
- Low Input Capacitance: 50 pF
- Low Power Dissipation: 618 mW
- No Sample/Hold Required for Video Bandwidth Signals
- Single Clock Cycle Conversion

HIGH SPEED 8–BIT ANALOG–TO–DIGITAL FLASH CONVERTER

SEMICONDUCTOR TECHNICAL DATA

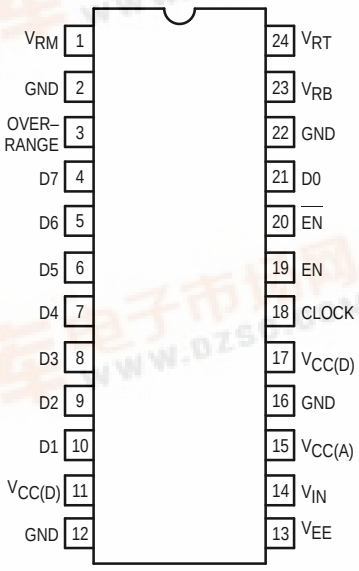
P SUFFIX
PLASTIC PACKAGE
CASE 709



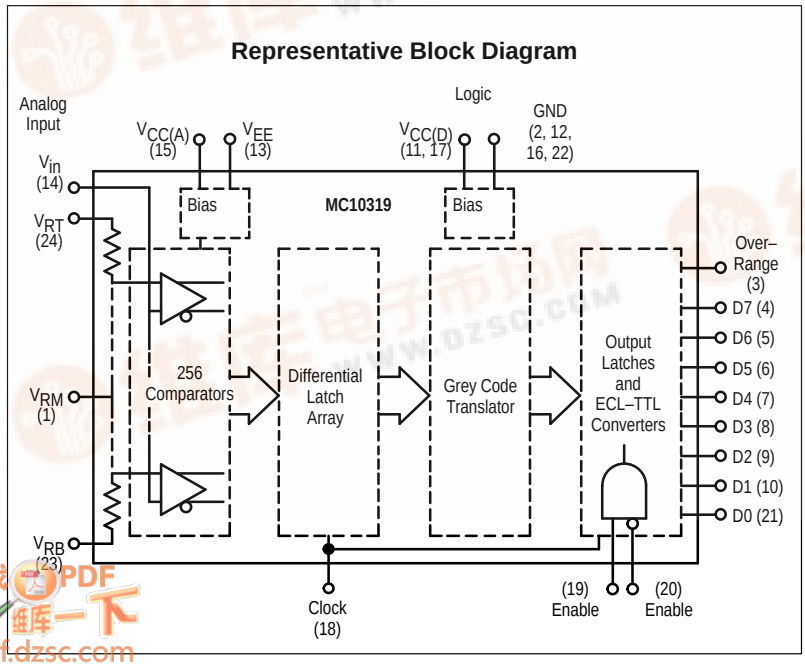


DW SUFFIX
PLASTIC PACKAGE
CASE 751F
(SO–28L)

PIN CONNECTIONS
(P only)



Representative Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC10319DW	T_A = 0° to +70°C	SO–28L
MC10319P		Plastic

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	$V_{CC(A),(D)}$ V_{EE}	+ 7.0 – 7.0	Vdc
Positive Supply Voltage Differential	$V_{CC(D)}$– $V_{CC(A)}$	– 0.3 to + 0.3	Vdc
Digital Input Voltage (Pins 18 to 20)	$V_{I(D)}$	– 0.5 to + 7.0	Vdc
Analog Input Voltage (Pins 1, 14, 23, 24)	$V_{I(A)}$	– 2.5 to + 2.5	Vdc
Reference Voltage Span (Pin 24 to Pin 23)	–	2.3	Vdc
Applied Output Voltage (Pins 4 to 10, 21 in 3–State)	–	– 0.3 to + 7.0	Vdc
Junction Temperature	T_J	+ 150	°C
Storage Temperature	T_{stg}	– 65 to + 150	°C

Devices should not be operated at these values. The “Recommended Operating Limits” table provides guidelines for actual device operation.

RECOMMENDED OPERATING LIMITS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (Pin 15) (Pins 11, 17)	$V_{CC(A)}$ $V_{CC(D)}$	+ 4.5	+ 5.0	+ 5.5	Vdc
$V_{CC(D)} - V_{CC(A)}$	ΔV_{CC}	– 0.1	0	+ 0.1	Vdc
Power Supply Voltage (Pin 13)	V_{EE}	– 6.0	– 5.0	– 3.0	Vdc
Digital Input Voltages (Pins 18 to 20)	$V_{I(D)}$	0	–	+ 5.0	Vdc
Analog Input (Pin 14)	$V_{I(A)}$	– 2.1	–	+ 2.1	Vdc
Voltage @ V_{RT} (Pin 24)	V_{RT}	– 1.0	–	+ 2.1	Vdc
Voltage @ V_{RB} (Pin 23)	V_{RB}	– 2.1	–	+ 1.0	Vdc
$V_{RT} - V_{RB}$	ΔV_R	+ 1.0	–	+ 2.1	Vdc
$V_{RB} - V_{EE}$	–	1.3	–	–	Vdc
Applied Output Voltage (Pins 4 to 10, 21 in 3–State)	V_o	0	–	5.5	Vdc
Clock Pulse Width – High Low	t_{CKH} t_{CKL}	5.0 15	20 20	– –	ns
Clock Frequency	f_{CLK}	0	–	25	MHz
Operating Ambient Temperature	T_A	0	–	+ 70	°C

ELECTRICAL CHARACTERISTICS ($0° < T_A < 70°C$, V_{CC} = 5.0 V, V_{EE} = – 5.2 V, V_{RT} = +1.0 V, V_{RB} = – 1.0 V, unless noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
TRANSFER CHARACTERISTICS (f_{CKL} = 25 MHz)					
Resolution	N	–	–	8.0	Bits
Monotonicity	MON		Guaranteed		Bits
Integral Nonlinearity	INL	–	± 1/4	± 1.0	LSB
Differential Nonlinearity	DNL	–	–	± 1.0	LSB
Differential Phase (See Figure 16)	DP	–	1	–	Deg.
Differential Gain (See Figure 16)	DG	–	1	–	%
Power Supply Rejection Ratio (4.5 V < V_{CC} < 5.5 V, V_{EE} = – 5.2 V) (– 6.0 V < V_{EE} < – 3.0 V, V_{CC} = + 5.0 V)	PSRR	 – –	 0.1 0	 – –	LSB/V

ELECTRICAL CHARACTERISTICS – continued

($0° < T_A < 70°C$, V_{CC} = 5.0 V, V_{EE} = – 5.2 V, V_{RT} = +1.0 V, V_{RB} = – 1.0 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ANALOG INPUTS (Pin 14)					
Input Current @ $V_{in} = V_{RB}$ (See Figure 5)	I_{INL}	– 100	0	–	μA
Input Current @ $V_{in} = V_{RT}$ (See Figure 5)	I_{INH}	–	60	150	μA
Input Capacitance ($V_{RT} – V_{RB}$ = 2.0 V, See Figure 4)	C_{in}	–	36	–	pF
Input Capacitance ($V_{RT} – V_{RB}$ = 1.0 V, See Figure 4)	C_{in}	–	55	–	pF
Bipolar Offset Error	V_{OS}	–	0.1	–	LSB
REFERENCE					
Ladder Resistance (V_{RT} to V_{RB}, T_A = 25°C)	R_{ref}	104	130	156	Ω
Temperature Coefficient	T_C	–	+ 0.29	–	%/°C
Ladder Capacitance (Pin 1 open)	C_{ref}	–	25	–	pF
ENABLE INPUTS (V_{CC} = 5.5 V) (See Figure 6)					
Input Voltage – High (Pins 19 to 20)	V_{IHE}	2.0	–	–	V
Input Voltage – Low (Pins 19 to 20)	V_{ILE}	–	–	0.8	V
Input Current @ 2.7 V	I_{IHE}	–	0	20	μA
Input Current @ 0.4 V @ $\overline{EN}$ (0 < EN < 5.0 V)	I_{IL1}	– 400	– 100	–	μA
Input Current @ 0.4 V @ $\overline{EN}$ ($\overline{EN}$ = 0 V)	I_{IL2}	– 400	– 100	–	μA
Input Current @ 0.4 V @ $\overline{EN}$ ($\overline{EN}$ = 2.0 V)	I_{IL3}	– 20	– 2.0	–	μA
Input Clamp Voltage (I_{IK} = – 18 mA)	V_{IKE}	– 1.5	– 1.3	–	V
CLOCK INPUTS (V_{CC} = 5.5 V)					
Input Voltage High	V_{IHC}	2.0	–	–	Vdc
Input Voltage Low	V_{ILC}	–	–	0.8	Vdc
Input Current @ 0.4 V (See Figure 7)	I_{ILC}	– 400	– 80	–	μA
Input Current @ 2.7 V (See Figure 7)	I_{IHC}	– 100	– 20	–	μA
Input Clamp Voltage (I_{IK} = – 18 mA)	V_{IKC}	– 1.5	– 1.3	–	Vdc
DIGITAL OUTPUTS					
High Output Voltage (I_{OH} = – 400 μA, V_{CC} = 4.5 V, See Figure 8)	V_{OH}	2.4	3.0	–	V
Low Output Voltage (I_{OL} = 4.0 mA, See Figure 9)	V_{OL}	–	0.35	0.4	V
Output Short Circuit Current* (V_{CC} = 5.5 V)	I_{SC}	–	35	–	mA
Output Leakage Current (0.4 < V_O < 2.4 V, See Figure 3, V_{CC} = 5.5 V, D0 to D7 in 3–State Mode)	I_{LK}	– 50	–	+ 50	μA
Output Capacitance (D0 to D7 in 3–State Mode)	C_{out}	–	9.0	–	pF
POWER SUPPLIES					
$V_{CC(A)}$ Current (4.5 V < $V_{CC(A)}$ < 5.5 V) (Outputs unloaded)	$I_{CC(A)}$	10	17	25	mA
$V_{CC(D)}$ Current (4.5 V < $V_{CC(D)}$ < 5.5 V) (Outputs unloaded)	$I_{CC(D)}$	50	90	133	mA
V_{EE} Current (– 6.0 < V_{EE} < – 3.0 V)	I_{EE}	– 14	– 10	– 6.0	mA
Power Dissipation ($V_{RT} – V_{RB}$ = 2.0 V) (Outputs unloaded)	P_D	–	618	995	mW

*Only one output is to be shorted at a time, not to exceed 1 second.

TIMING CHARACTERISTICS (T_A = 25°C, V_{CC} = + 5.0 V, V_{EE} = – 5.2 V, V_{RT} = + 1.0 V, V_{RB} = – 1.0 V, see System Timing Diagram, Figure 1.)

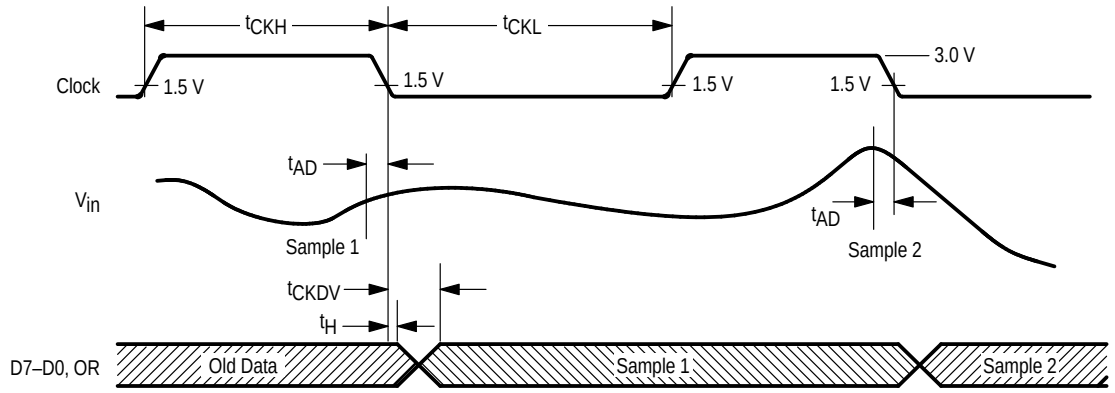
Characteristic	Symbol	Min	Typ	Max	Unit
INPUTS					
Min Clock Pulse Width – High	t_{CKH}	–	5.0	–	ns
Min Clock Pulse Width – Low	t_{CKL}	–	15	–	ns
Max Clock Rise, Fall Time	$t_{R,F}$	–	100	–	ns
Clock Frequency	f_{CLK}	0	30	25	MHz
OUTPUTS					
New Data Valid from Clock Low	t_{CKDV}	–	19	–	ns
Aperture Delay	t_{AD}	–	4.0	–	ns
Hold Time	t_H	–	6.0	–	ns
Data High to 3–State from Enable Low*	t_{EHZ}	–	27	–	ns
Data Low to 3–State from Enable Low*	t_{ELZ}	–	18	–	ns
Data High to 3–State from Enable High*	t_{EHZ}	–	32	–	ns
Data Low to 3–State from Enable High*	t_{ELZ}	–	18	–	ns
Valid Data from Enable High (Pin 20 = 0 V)*	t_{EDV}	–	15	–	ns
Valid Data from Enable Low (Pin 19 = 5.0 V)*	t_{EDV}	–	16	–	ns
Output Transition Time* (10% to 90%)	t_{tr}	–	8.0	–	ns

*See Figure 2 for output loading.

PIN FUNCTION DESCRIPTION

Function	Pin		Description
	P Suffix	DW Suffix	
V_{RM}	1	1	The midpoint of the reference resistor ladder. Bypassing can be done at this point to improve performance at high frequencies.
GND	2, 12 16, 22	2, 13, 17 18, 25, 26	Digital ground. The pins should be connected directly together, and through a low impedance path to the power supply.
OVR	3	3	Overrange output. Indicates V_{in} is more positive than V_{RT} 1/2 LSB. This output does not have 3–state capability.
D7–D0	4 to 10, 21	4 to 10, 24	Digital Outputs. D7 (Pin 4) is the MSB. D∅ (Pin 21 or 24) is the LSB. LS–TTL compatible with 3–state capability.
$V_{CC(D)}$	11, 17	11, 12 19, 20	Power supply for the digital section. +5.0 V, ±10% required. Reference to digital ground.
V_{EE}	13	14	Negative power supply. Nominally – 5.2 V, it can range from – 3.0 to – 6.0 V, and must be more negative than V_{RB} by > 1.3 V. Reference to analog ground.
V_{in}	14	15	Signal voltage input. This voltage is compared to the reference to generate a digital equivalent. Input impedance is nominally 16 to 33K in parallel with 36 pF.
$V_{CC(A)}$	15	16	Power supply for the analog section. +5.0 V, ±10% required. Reference to analog ground.
CLK	18	21	Clock input. TTL compatible.
EN	19	22	Enable input. TTL compatible, a logic 1 (and $\overline{EN}$ at a logic 0) enables the data outputs. A logic 0 puts the outputs in a 3–state mode.
$\overline{EN}$	20	23	Enable input. TTL compatible, a logic 0 (and EN at a logic 1) enables the data outputs. A logic 1 puts the outputs in a 3–state mode.
V_{RB}	23	27	The bottom (most negative point) of the internal reference resistor ladder.
V_{RT}	24	28	The top (most positive point) of the internal reference resistor ladder.

Figure 1. System Timing Diagram



t_{CKDV} and t_H measured at output levels of 0.8 and 2.4 V.

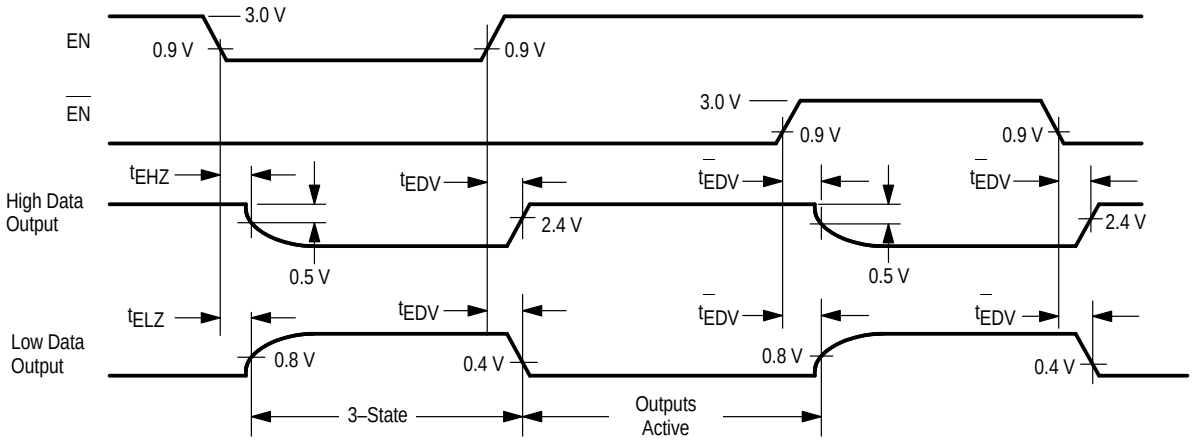
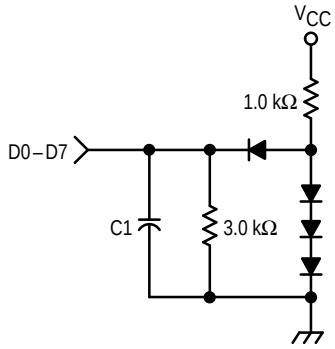


Figure 2. Data Output Test Circuit



Diodes = 1N914 or equivalent, C1 ≈ 15 pF

Figure 3. Output 3–State Leakage Current

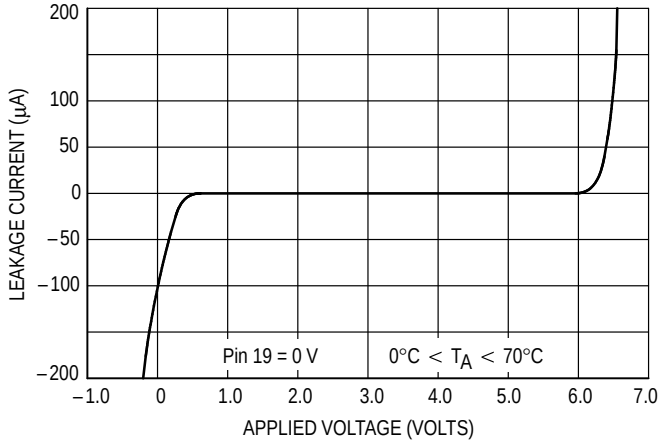


Figure 4. Input Capacitance @ V_{in} (Pin 14)

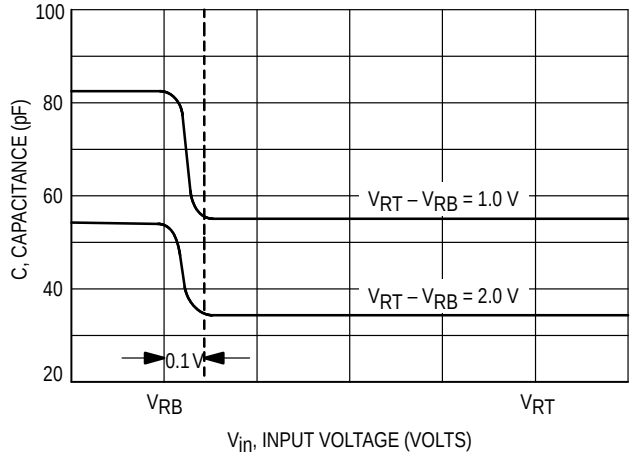


Figure 5. Input Current @ V_{in} (Pin 14)

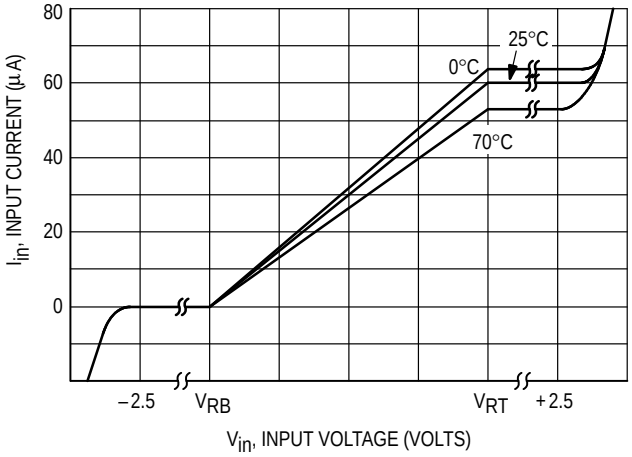


Figure 6. Input Current @ Enable, $\overline{\text{Enable}}$

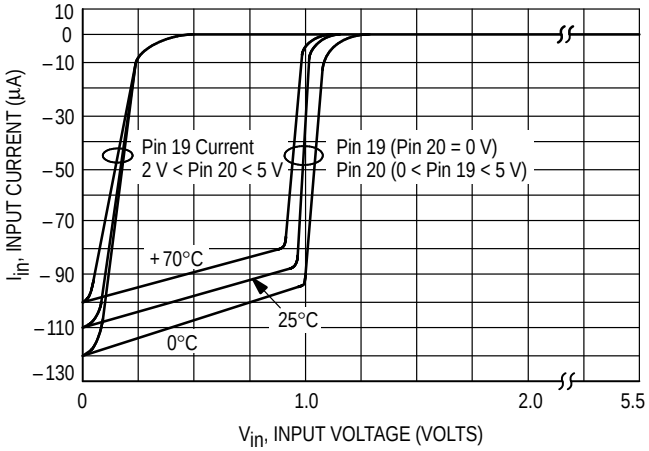


Figure 7. Clock Input Current

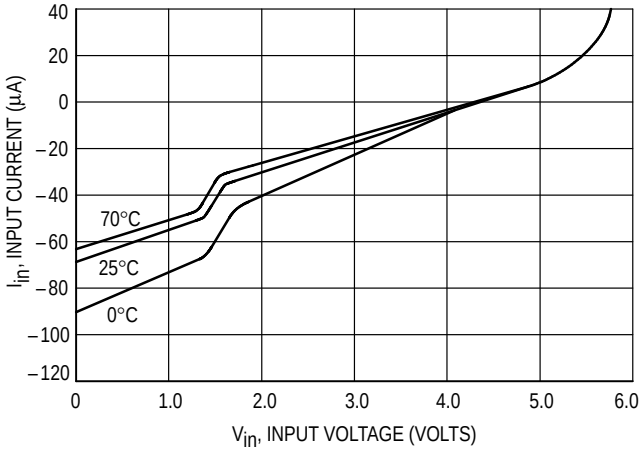


Figure 8. Output Voltage versus Output Current

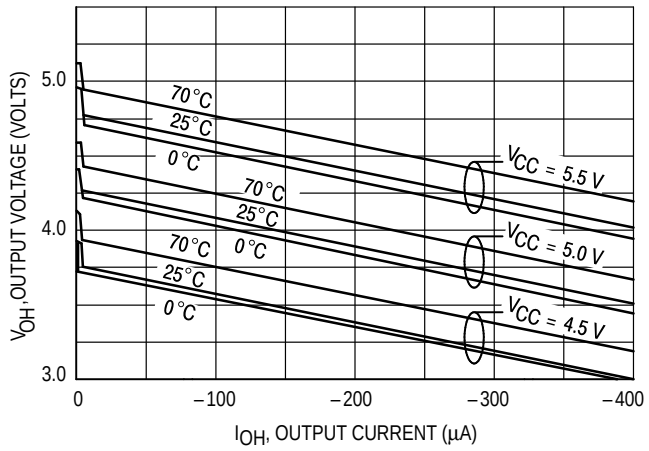


Figure 9. Output Voltage versus Output Current

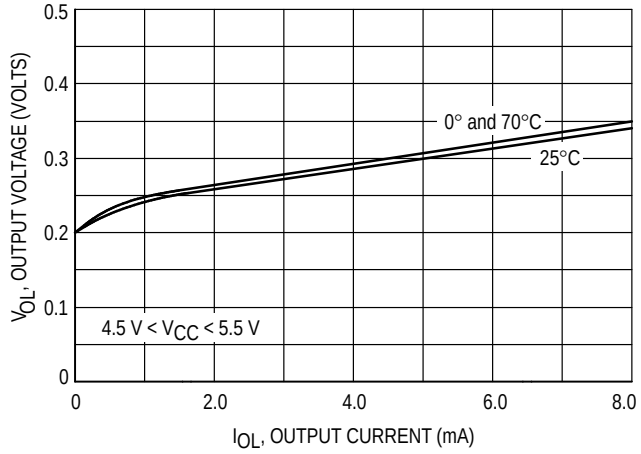


Figure 10. Supply Current versus Temperature

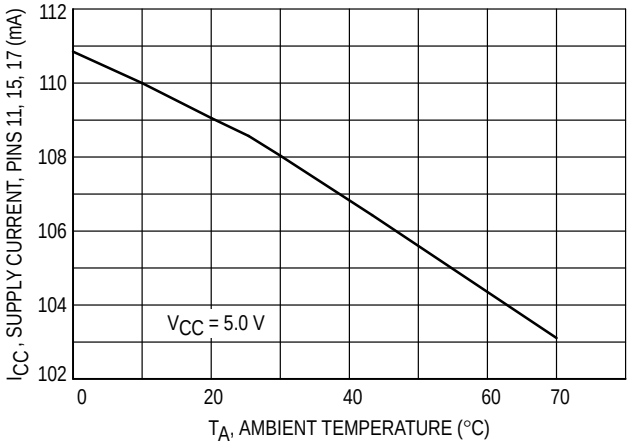


Figure 11. Supply Current versus Temperature

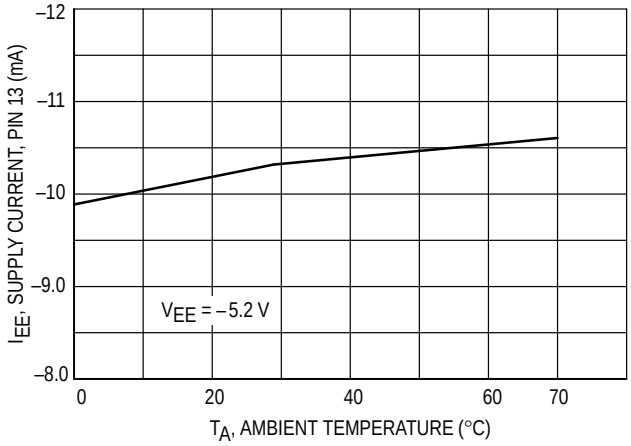


Figure 12. Differential Linearity Error

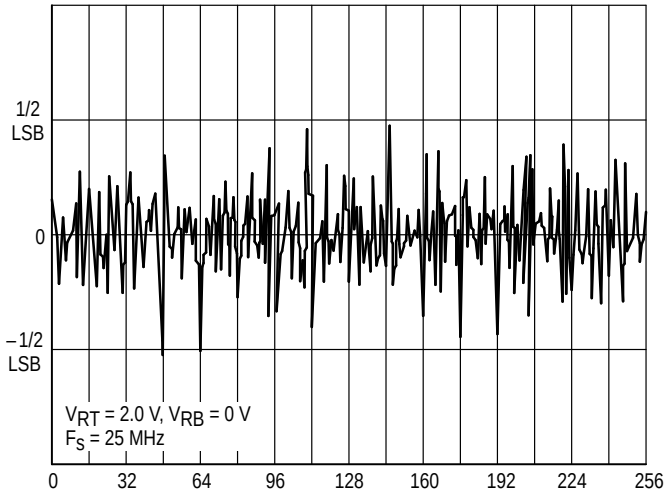


Figure 13. Integral Linearity Error

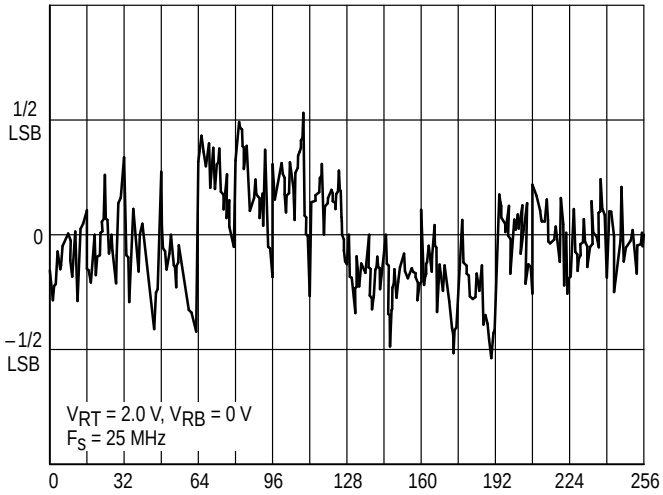


Figure 14. Differential Linearity Error

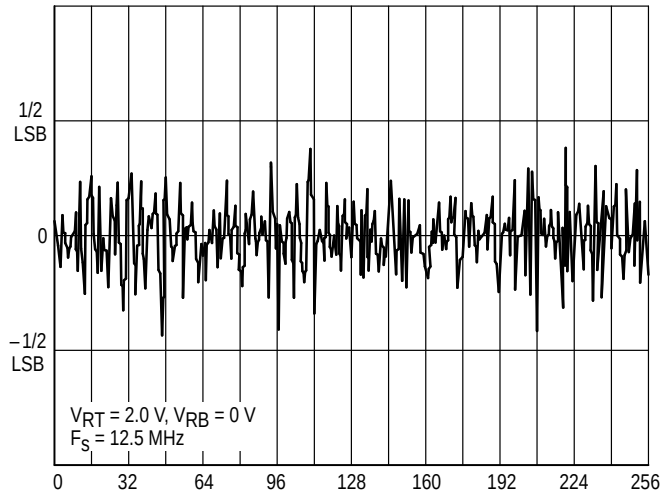
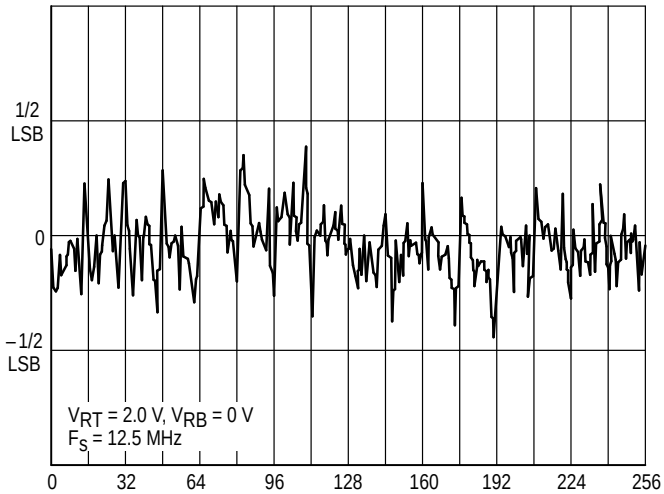


Figure 15. Integral Linearity Error



MC10319

DESIGN GUIDELINES

Introduction

The MC10319 is a high speed, 8–bit, parallel (“flash”) type analog–to–digital converter containing 256 comparators at the front end. See Figure 17 for a block diagram. The comparators are arranged such that one input of each is referenced to evenly spaced voltages, derived from the reference resistor ladder. The other input of the comparators is connected to the input signal (V_{in}). Some of the comparator′s differential outputs will be “true,” while other comparators will have “not true” outputs, depending on their relative position. Their outputs are then latched, and converted to an 8–bit Grey code by the Differential Latch Array. The Grey code ensures that any input errors due to cross talk, feed–thru, or timing disparities result in glitches at the output of only a few LSBs, rather than the more traditional 1/2 scale and 1/4 scale glitches.

The Grey code is then translated to an 8–bit binary code, and the differential levels are translated to TTL levels before being applied to the output latches. Enable inputs at this final stage permit the TTL outputs (except overrange) to be put into a high impedance (3–state) condition.

ANALOG SECTION

Signal Input

The signal voltage to be digitized (V_{in}) is applied simultaneously to one input of each of the 256 comparators through Pin 14. The other inputs of the comparators are connected to 256 evenly spaced voltages derived from the reference ladder. The output code depends on the relative position of the input signal and the reference voltages. The comparators have a bandwidth of $>$ 50 MHz, which is more than sufficient for the allowable (Nyquist Theorem) input frequency of 12.5 MHz.

The current into Pin 14 varies linearly from 0 (when $V_{in} = V_{RB}$) to ≈60 μA (when $V_{in} = V_{RT}$). If V_{in} is taken below V_{RB} or above V_{RT}, the input current will remain at the value corresponding to V_{RB} and V_{RT} respectively (see Figure 5). However, V_{in} must be maintained within the absolute range of ±2.5 V (with respect to ground) – otherwise excessive currents will result at Pin 14, due to internal clamps.

The input capacitance at Pin 14 is typically 36 pF if [$V_{RT} – V_{RB}$] is 2.0 V, and increases to 55 pF if [$V_{RT} – V_{RB}$] is reduced to 1.0 V (see Figure 4). The capacitance is constant as V_{in} varies from V_{RT} down to ≈0.1 V above V_{RB}. Taking V_{in} to V_{RB} will show an increase in the capacitance of ≈50%. If V_{in} is taken above V_{RT}, or below V_{RB}, the capacitance will stay at the values corresponding to V_{RT} and V_{RB}, respectively.

The source impedance of the signal voltage should be maintained below 100 Ω (at the frequencies of interest) in order to avoid sampling errors.

Reference

The reference resistor ladder is composed of a string of equal value resistors to provide 256 equally spaced voltages for the comparators (see Figure 17 for the actual configuration). The voltage difference between adjacent comparators corresponds to 1 LSB of the input range. The first comparator (closest to V_{RB}) is referenced 1/2 LSB above V_{RB}, and 256th comparator (for the overrange) is referenced 1/2 LSB below V_{RT}. The total resistance of the ladder is nominally 130 Ω, ±20%, requiring 15.4 mA @ 2.0 V, and 7.7 mA @ 1.0 V. There is a nominal warm–up change of ≈ +9.0% in the ladder resistance due to the +0.29%/°C temperature coefficient.

The minimum recommended span [$V_{RT} – V_{RB}$] is 1.0 V. A lower span will allow offsets and nonlinearities to become significant. The maximum recommended span is 2.1 V due to power limitations of the resistor ladder. The span may be anywhere within the range of – 2.1 to + 2.1 V with respect to ground, and V_{RB} must be at least 1.3 V more positive than V_{EE}. The reference voltages must be stable and free of noise and spikes, since the accuracy of a conversion is directly related to the quality of the reference.

In most applications, the reference voltages will remain fixed. In applications involving a varying reference for modulation or signal scrambling, the modulating signal may be applied to V_{RT}, or V_{RB}, or both. The output will vary inversly with the reference signal, introducing a nonlinearity into the transfer function. The addition of the modulating signal and the dc level applied to the reference must be such that the absolute voltage at V_{RT} and V_{RB} is maintained within the values listed in the Recommended Operating Limits. The RMS value of the span must be maintained $\leq$ 2.1 V.

V_{RM} (Pin 1) is the midpoint of the resistor ladder, excluding the Overrange comparator. The voltage at V_{RM} is:

$$\frac{V_{RT} + V_{RB}}{2.0} - 1/2 \text{ LSB}$$

In most applications, bypassing this pin to ground (0.1 μF) is sufficient to maintain accuracy. In applications involving very high frequencies, and where linearity is critical, it may be necessary to trim the voltage at the midpoint. A means for accomplishing this is indicated in Figure 18.

Power Supplies

$V_{CC(A)}$ is the positive power supply for the comparators, and $V_{CC(D)}$ is the positive power supply for the digital portion. Both are to be +5.0 V, ±10%, and the two are to be within 100 mV of each other. There is indirect internal coupling between $V_{CC(D)}$ and $V_{CC(A)}$. If they are powered separately, and one supply fails, there will be current flow through the MC10319 to the failed supply.

$I_{CC(A)}$ is nominally 17 mA, and does not vary with clock frequency or with V_{in}. It does vary linearly with $V_{CC(A)}$. $I_{CC(D)}$ is nominally 90 mA, and is independent of clock frequency. It does vary, however, by 6 to 7 mA as V_{in} is changed, with the lowest current occurring when $V_{in} = V_{RT}$. It varies linearly with $V_{CC(D)}$.

V_{EE} is the negative power supply for the comparators, and is to be within the range – 3.0 to – 6.0 V. Additionally, V_{EE} must be at least 1.3 V more negative than V_{RB}. I_{EE} is a nominal – 10 mA, and is independent of clock frequency, V_{in}, and V_{EE}.

For proper operation, the supplies **must** be bypassed **at the IC**. A 10 μF tantalum, in parallel with a 0.1 μF ceramic is recommended for each supply to ground.

DIGITAL SECTION

Clock

The Clock input is TTL compatible with a typical frequency range of 0 to 30 MHz. There is no duty cycle limitations, but the minimum low and high times must be adhered to. See Figure 7 for the input current requirements.

The conversion sequence is shown in Figure 19, and is as follows:

- On the rising edge, the data output latches are latched with old data, and the comparator output latches are released to follow the input signal (V_{in}).
- During the high time, the comparators track the input signal. The data output latches retain the old data.
- On the falling edge, the comparator outputs are latched with the data immediately prior to this edge. The conversion to digital occurs within the device, and the data output latches are released to indicate the new data within 20 ns.
- During the clock low time, the comparator outputs remain latched, and the data output latches remain transparent.

A summary of the sequence is that data present at V_{in} just prior to the Clock falling edge is digitized and available at the data outputs immediately after that same falling edge.

The comparator output latches provide the circuit with an effective sample–and–hold function, eliminating the need for an external sample–and–hold.

Enable Inputs

The two Enable inputs are TTL compatible, and are used to change the data outputs (D7–D0) from active to 3–state. This capability allows cascading two MC10319s into a 9–bit configuration, flip–flopping two MC10319s into a 50 MHz configuration, connecting the outputs directly to a data bus, multiplexing multiple converters, etc. See the Applications Information section for more details. For the outputs to be active, Pin 19 must be a Logic “1”, and Pin 20 must be a Logic “0”. Changing either input will put the outputs into the high impedance mode. The Enable inputs affect **only** the state of the outputs – they do not inhibit a conversion. The input current into Pins 19 and 20 is shown in Figure 6, and the input/output timing is shown in Figure 1 and 20. Leaving either pin open is equivalent to a Logic “1”, although good design practice dictates that an input should never be left open.

The Overrange output (Pin 3) is not affected by the Enable inputs as it does not have 3–state capability.

Outputs

The Data outputs are TTL level outputs with high impedance capability. Pin 4 is the MSB (D7), and Pin 21 is the LSB (D0). The eight outputs are active as long as the Enable inputs are true (Pin 19 = high, Pin 20 = low). The timing of the outputs relative to the Clock input and the Enable inputs is shown in Figures 1 and 20. Figures 8 and 9 indicate the output voltage versus load current, while Figure 3 indicates the leakage current when in the high impedance mode.

The output code is natural binary, depicted in the table below.

The Overrange output (Pin 3) goes high when the input, V_{in}, is more positive than V_{RT} – 1/2 LSB. This output is always active – it does not have high impedance capability. Besides being used to indicate an input overrange, it is additionally used for cascading two MC10319s to form a 9–bit A/D converter (see Figure 27).

Table 1. Output Code

Input	V_{RT}, V_{RB} (V)			Output Code	Overrange
	2.048 V, 0 V	+ 1.0 V, – 1.0 V	+ 1.0 V, 0 V		
$> V_{RT}$ – 1/2 LSB	> 2.044V	> 0.9961 V	> 0.9980 V	FF_H	1
V_{RT} – 1/2 LSB	2.044 V	0.9961 V	0.9980 V	FF_H	$0 \leftrightarrow 1$
V_{RT} – 1 LSB	2.040 V	0.992 V	0.9961 V	FF_H	0
V_{RT} – 1–1/2 LSB	2.036 V	0.988 V	0.9941 V	$FE_H \leftrightarrow FF_H$	0
Midpoint	1.024 V	0.000 V	0.5000 V	80_H	0
V_{RB} + 1/2 LSB	4.0 mV	– 0.9961 V	1.95 mV	$00_H \leftrightarrow 01_H$	0
$< V_{RB}$	< 0 V	< – 1.0 V	< 0 V	00_H	0

APPLICATIONS INFORMATION

Power Supplies, Grounding

The PC board layout, and the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC}, V_{EE}, or ground can cause an incorrect output code due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC10319 can cause incorrect operation if that noise does not have a clear path to ac ground.

Both the V_{CC} and V_{EE} power supplies must be decoupled to ground **at the IC** (within 1″ max) with a 10 μF tantalum and a 0.1 μF ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present when digital circuits are present) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the operation can be disrupted. Noise can be reduced by inserting resistors and/or inductors between the supplies and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 V or greater at frequencies of 50 to 200 kHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, 3–terminal regulators (MC78L05ACP, MC7905.2CT), with appropriate high frequency filtering, should be used and dedicated to the MC10319.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Limits table.

The PC board tracks supplying V_{CC} and V_{EE} to the MC10319 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The MC10319 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the boards, then it is preferable to have dedicated lines from the supply or connector directly to the MC10319.

The four ground pins (2, 12, 16, and 22) must be connected directly together. Any long path between them can cause stability problems due to the inductance (at 25 MHz) of the PC tracks. The ground return for the signal source must be noise free.

Reference Voltage Circuits

Since the accuracy of the conversion is directly related to the quality of the references, it is imperative that accurate and stable voltages be provided to V_{RT} and V_{RB}. If the reference span is 2.0 V, then 1/2 LSB is only 3.9 mV, and it is desireable that V_{RT} and V_{RB} be accurate to within this amount, and furthermore, that they do not drift more than this amount once set. Over the temperature range of 0° to 70°C, a maximum temperature coefficient of 28 ppm/°C is required.

The voltage supplies used for digital circuits should preferably **not** be used as a source for generating V_{RT} and V_{RB}, due to the noise spikes (50 to 400 mV) present on the supplies and on their ground lines. Generally ±15 V, or ±12 V, are available for analog circuits, and are usually clean compared to supplies used for digital circuits, although ripple may be present in varying amounts. Ripple is easier to filter out than spikes, however, and so these supplies are preferred.

Figure 21 depicts a circuit which can provide an extremely stable voltage to V_{RT} **at the current required** (the maximum reference current is 19.2 mA @ 2.0 V). The MC1403 series of reference sources has very low temperature coefficients, good noise rejection, and a high initial accuracy, allowing the circuit to be built without an adjustment pot if the V_{RT} voltage is to remain fixed at one value. Using 0.1% wirewound resistors for the divider provides sufficient accuracy and stability in many cases. Alternately, resistor networks provide high ratio accuracies, and close temperature tracking. If the application requires V_{RT} to be changed periodically, the two resistors can be replaced with a 20 turn, cermet potentiometer. Wirewound potentiometers should not be used for this type of application since the pot's slider jumps from winding to winding, and an exact setting can be difficult to obtain. Cermet pots allow for a smooth continuous adjustment.

In Figure 21, R1 reduces the power dissipation in the transistor, and can be carbon composition. The 0.1 μF capacitor in the feedback path provides stability in the unity gain configuration. Recommended op amps are: LM358, MC34001 series, LM308A, LM324, and LM11C. Offset drift is the key parameter to consider in choosing an op amp, and the LM308A has the lowest drift of those mentioned. Bypass capacitors are not shown in Figure 21, but should always be provided at the input to the 2.5 V reference, and at the power supply pins of the op amp.

Figure 22 shows a simpler and more economical circuit, using the LM317LZ regulator, but with lower initial accuracy and temperature stability. The op amp/current booster is not needed since the LM317LZ can supply the current directly. In a well controlled environment, this circuit will suffice for many applications. Because of the lower initial accuracy, an adjustment pot is a necessity.

Figure 23 shows two circuits for providing the voltage to V_{RB}. The circuits are similar to those of Figures 21 and 22, and have similar accuracy and stability. The output transistor is a PNP in this case since the circuit must sink the reference current.

VIDEO APPLICATIONS

The MC10319 is suitable for digitizing video signals directly without signal conditioning, although the standard 1.0 V_{pp} video signal can be amplified to a 2.0 V_{pp} signal for slightly better accuracy. Figure 24 shows the input (top trace) and reconstructed output of a standard NTSC test signal, sampled at 25 MSPS, consisting of a sync pulse, 3.58 MHz color burst, a 3.58 MHz signal in a Sin^2x envelope, a pulse, a white level signal, and a black level signal. Figure 25 shows a Sin^2x pulse that has been digitized and reconstructed at 25 MSPS. The width of the pulse is ≈450 ns at the base. Figure 26 shows an application circuit for digitizing video.

9–Bit A/D Converter

Figure 27 shows how two MC10319s can be connected to form a 9–bit converter. In this configuration, the outputs (D7 to D0) of the two 8–bit converters are paralleled. The outputs of one device are active, while the outputs of the other are in the 3–state mode. The selection is made by the Overrange output of the lower MC10319, which controls Enable inputs on the two devices. Additionally, this output provides the 9th bit.

The reference ladders are connected in series, providing the 512 steps required for 9 bits. The input voltage range is determined by V_{RT} of the upper MC10319, and V_{RB} of the lower device. A minimum of 1.0 volt is required across each converter. The 500 Ω pot (20 turn cermet) allows for adjustment of the midpoint since the reference resistors of the two MC10319s may not be identical in value. Without the adjustment, a non–equal voltage division would occur, resulting in a nonlinear conversion. If the references are to be symmetrical about ground (e.g., ± 1.0 V), the adjustment can be eliminated, and the midpoint connected to ground. The use of latches on the outputs is optional, depending on the application.

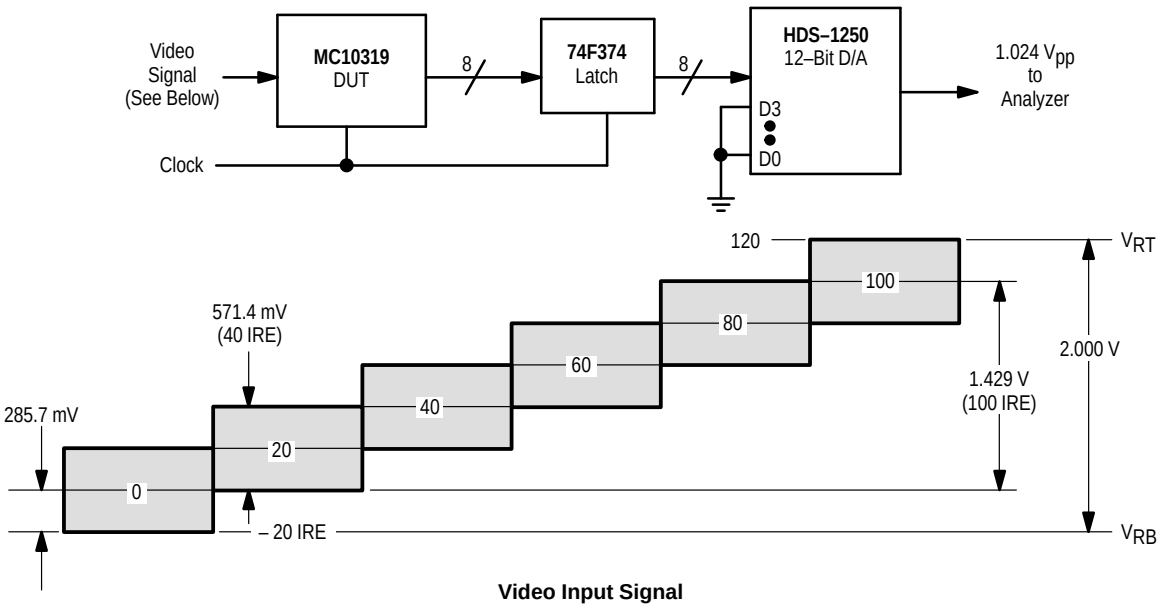
50 MHz, 8–Bit A/D Converter

Figure 28 shows how two MC10319s can be connected together in a flip–flop arrangement in order to have an effective conversion speed of 50 MHz. The 74F74 D–type flip–flop provides a 25 MHz clock to each converter, and at the same time, controls the Enables so as to alternately enable and disable the outputs. The Overranges do not have 3–state capability, and so cannot be paralleled. Instead they are OR'd together. The use of latches is optional, and depends on the application. Data should be latched, or written to RAM (in a DMA operation), on the high–to–low transition of the 50 MHz clock.

Negative Voltage Regulator

In the cases where a negative power supply is not available (neither the – 3.0 to – 6.0 V, nor a higher negative voltage from which to derive it), the circuit of Figure 29 can be used to generate – 5.0 V from the + 5.0 V supply. The PC board space required is small (≈ 2.0 in^2), and it can be located physically close to the MC10319. The MC34063A is a switching regulator, and in Figure 29 is configured in an inverting mode of operation. The regulator operating specifications are also given.

Figure 16. Differential Phase and Gain Test



Video Input Signal

1. Input waveform: 571.4 mV_{pp}, sine wave @ 3.579545 MHz, dc levels as shown above.
2. MC10319 clock at 14.31818 MHz (4x) asynchronous to input.
3. Differential gain: peak–to–peak output @ each IRE level compared to that at 0 IRE.
4. Differential phase: Phase @ each IRE level compared to that @ 0 IRE.

Figure 17. Representative Block Diagram

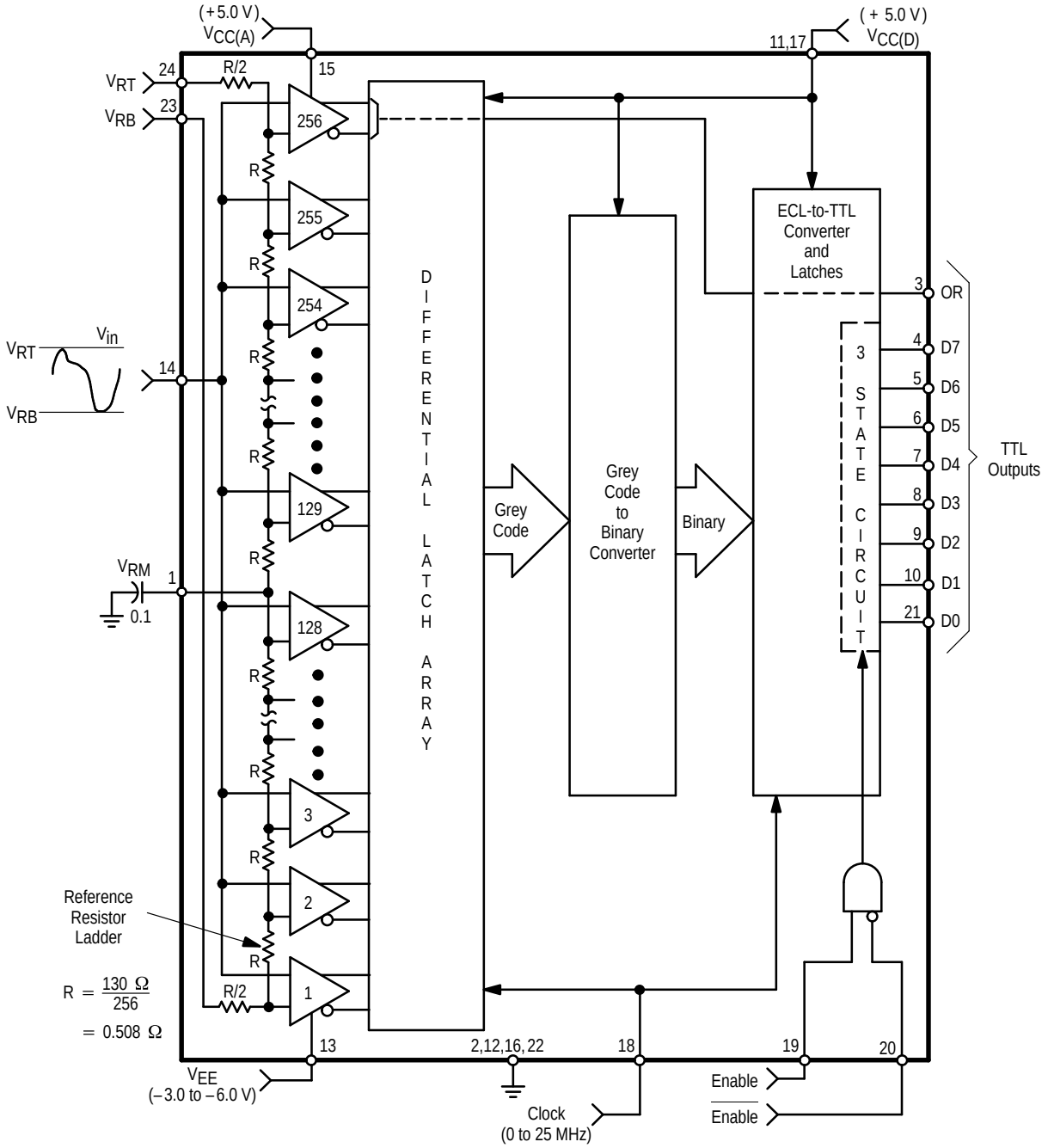


Figure 18. Adjusting V_{RM} for Improved Linearity

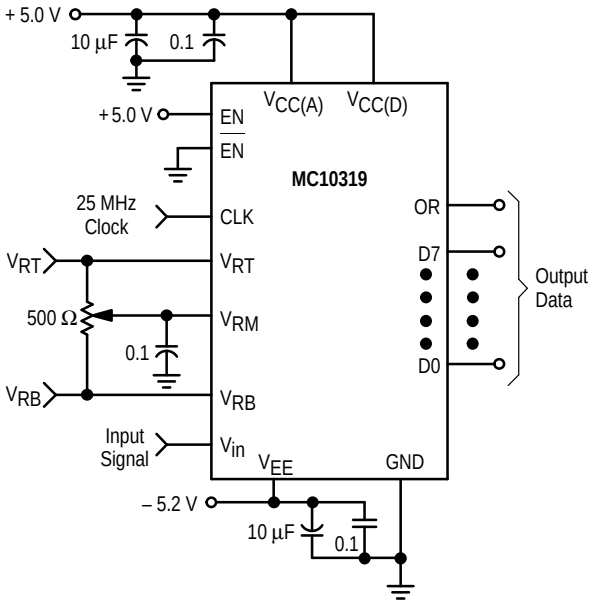


Figure 19. Conversion Sequence

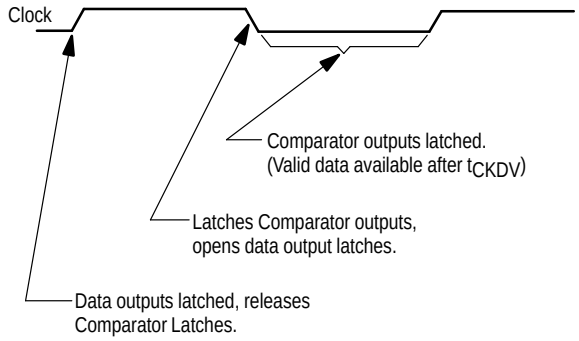
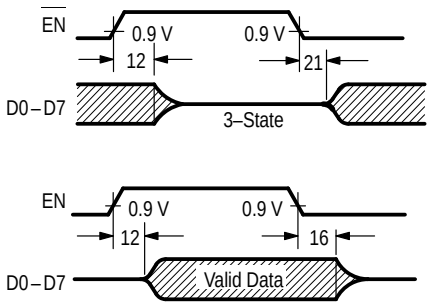


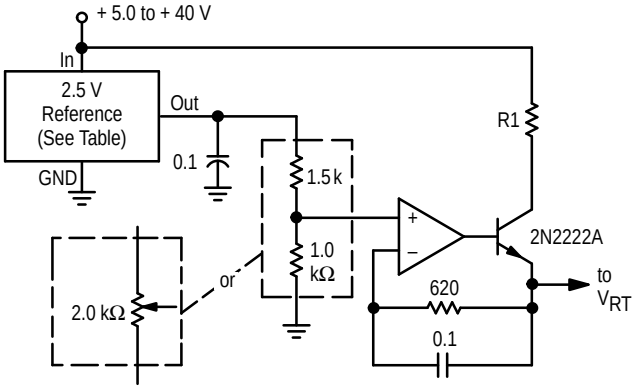
Figure 20. Enable to Output Critical Timing



Timing @ D7 to D0 measured where waveform starts to change.
Indicated time values are typical @ 25°C, and are in ns.

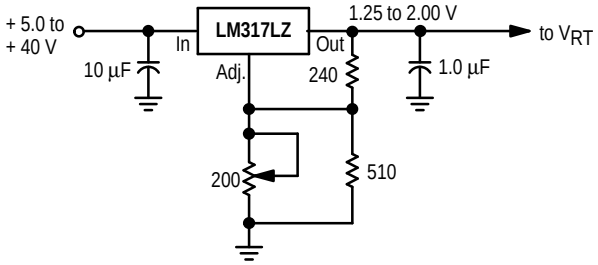
Figure 21. Precision V_{RT} Voltage Source

R1 = 100 Ω for + 5.0 V
620 Ω for + 15 V



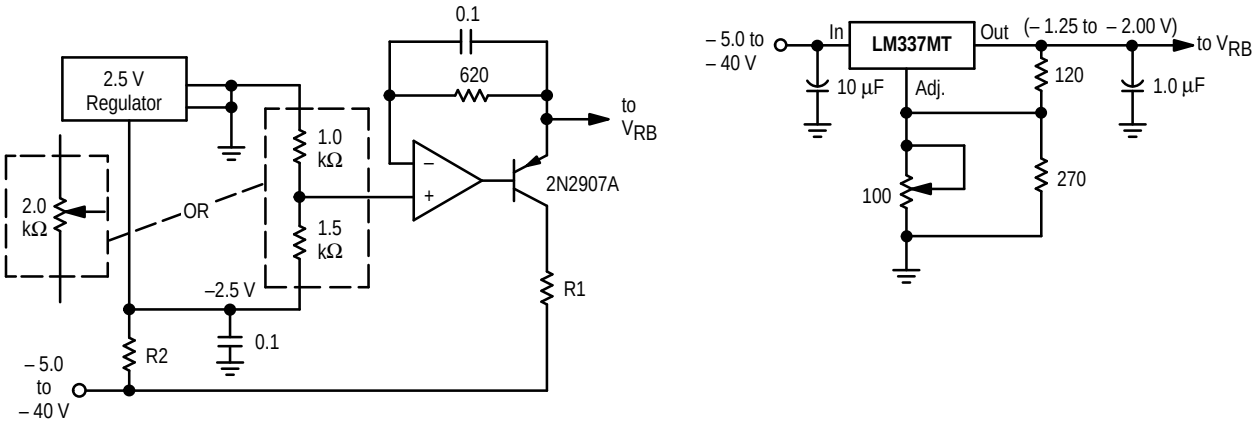
2.5 V References	MC1403	MC1403A
Line Regulation	0.5 mV	0.5 mV
T_C (ppm/°C) max	40	25
ΔV_{out} for 0 to + 70°C	7.0 mV	4.4 mV
Initial Accuracy	± 1%	± 1%

Figure 22. Voltage Source for V_{RT} Pin



LM317LZ	
Line Regulation	1.0 mV
T_C (ppm/°C) max	60
ΔV_{out} for 0 to + 70°C	8.4 mV
Initial Accuracy	± 4%

Figure 23. Voltage Sources for V_{RB} Pin



R1 = 100 Ω for –5.0 V
= 620 Ω for –15 V

R2 = 620 Ω for –5.0 V
= 3.0 kΩ for –15 V

2.5 V Reference	LM337MT
Line Regulation	1.0 mV
T_C (ppm/°C) max	48
ΔV_{out} for 0 to +70°C	6.7 mV
Initial Accuracy	±4%

Figure 24. Composite Video Waveform

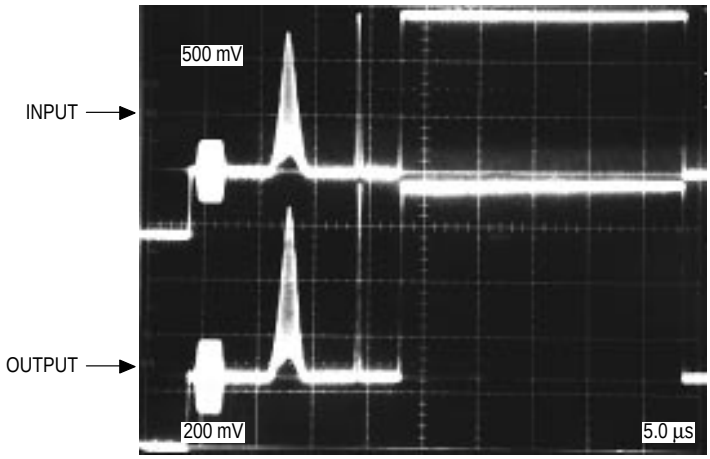


Figure 25. SIN^2 x Waveform

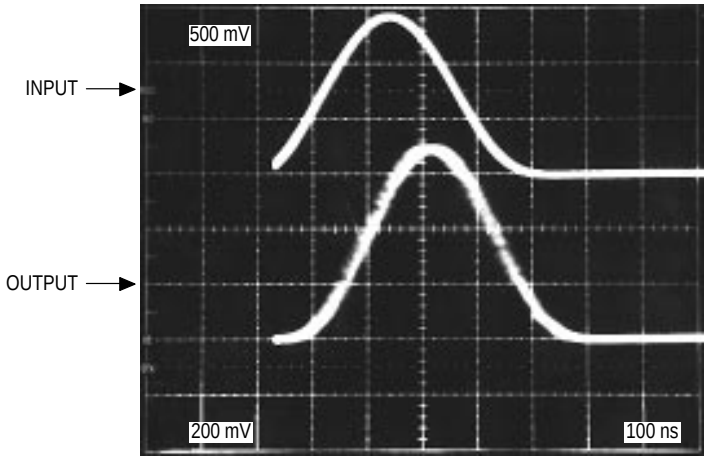
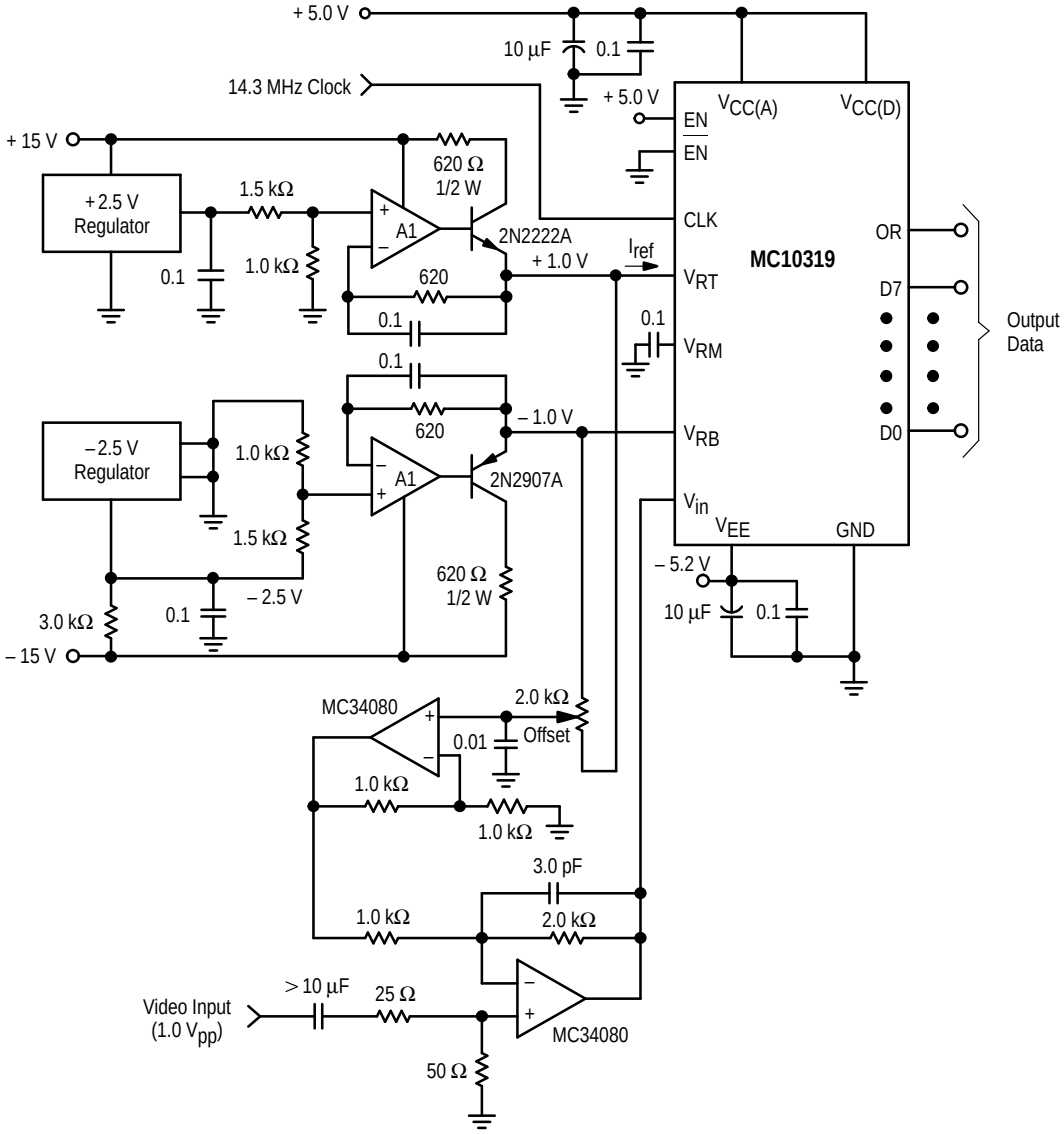


Figure 26. Application Circuit for Digitizing Video



NOTES: 1) MC34080′s powered from ± 15 V supplies. MC34083 (Dual) may be used.
2) Bypass capacitors required at power supply pins of **all** ICs.
3) Ground plane required over all parts of circuit board.
4) Care in layout around MC34080′s necessary for good frequency response.
5) A1 = MC34002.

Figure 27. 9–Bit A/D Converter

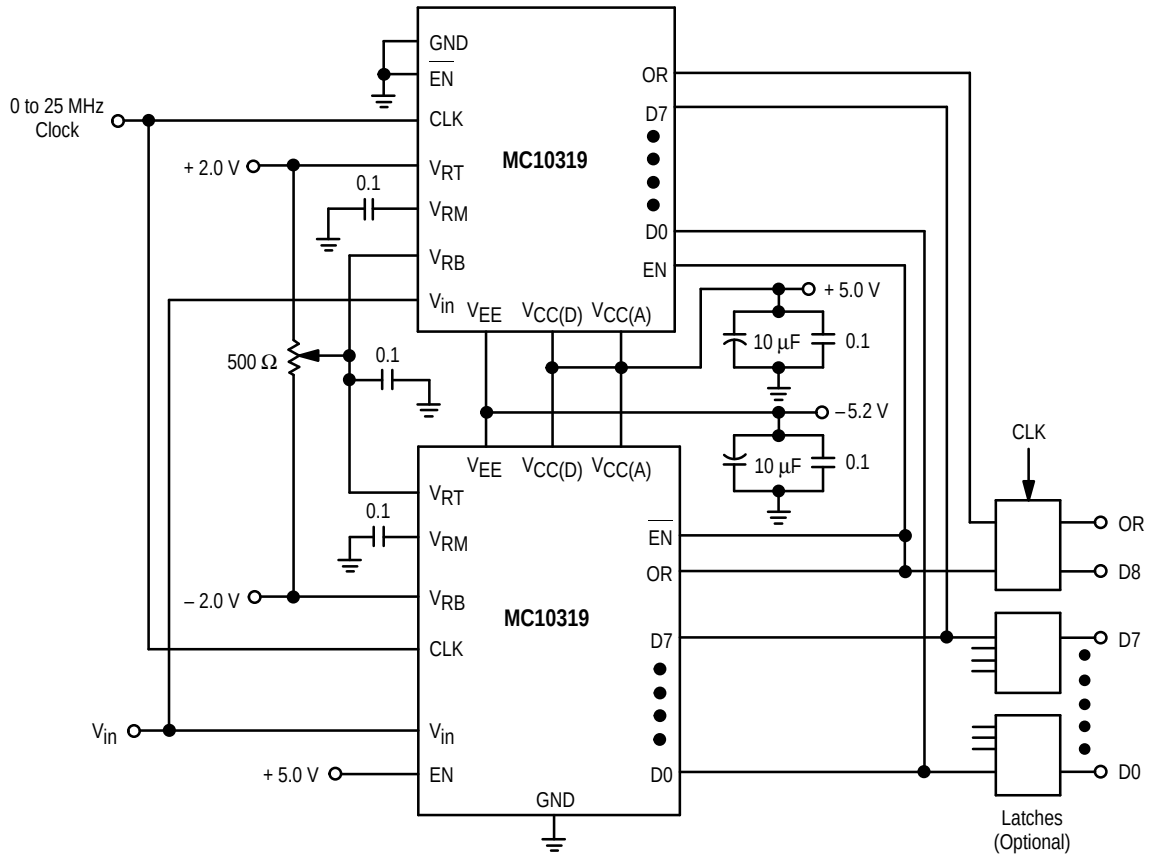
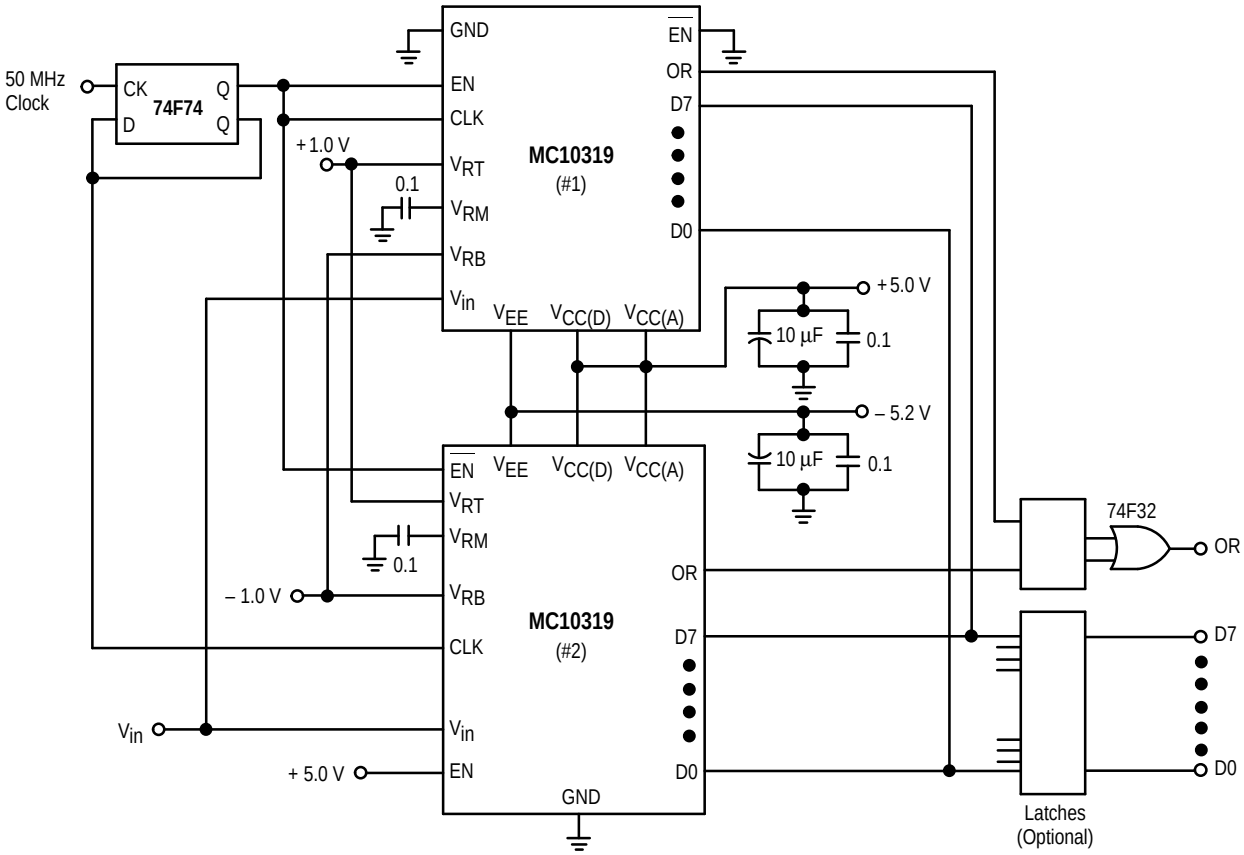


Figure 28. 50 MHz 8–Bit A/D Converter



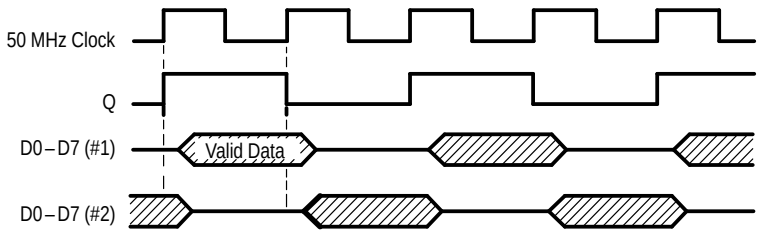
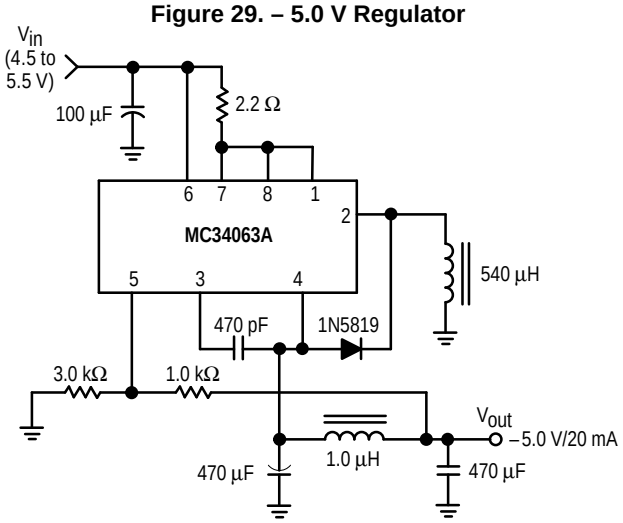


Figure 29. – 5.0 V Regulator



Test	Conditions	Results
Line Regulation	4.5 V < V_{in} < 5.5 V, I_{out} = 10 mA	0.16%
Load Regulation	V_{in} = 5.0 V, 8.0 mA < I_{out} < 20 mA	0.4%
Output Ripple	V_{in} = 5.0 V, I_{out} = 20 mA	2.0 mV_{pp}
Short Circuit I_{out}	V_{in} = 5.0 V, R1 = 0.1 Ω	140 mA
Efficiency	V_{in} = 5.0 V, I_{out} = 50 mA	52%

GLOSSARY

Aperture Delay – The time difference between the sampling signal (typically a clock edge) and the actual analog signal converted. The actual signal converted may occur before or after the sampling signal, depending on the internal configuration of the converter.

Bipolar Input – A mode of operation whereby the analog input (of an A/D), or output (of a DAC), includes both negative and positive values. Examples are – 1.0 to + 1.0 V, – 5.0 to + 5.0 V, – 2.0 to + 8.0 V, etc.

Bipolar Offset Error – The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative reference voltage.

Bipolar Zero Error – The error (usually expressed in LSBs) of the input voltage location (of an A/D) of the 80_H to 81_H transition. The ideal location is 1/2 LSB above zero volts in the case of an A/D setup for a symmetrical bipolar input (e.g., – 1.0 to + 1.0 V).

Differential Nonlinearity – The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n (n = number of bits). This error must be within ± 1 LSB for proper operation.

ECL – Emitter coupled logic.

Full Scale Range (Actual) – The difference between the actual minimum and maximum end points of the analog input (of an A/D).

Full Scale Range (Ideal) – The difference between the actual minimum and maximum end points of the analog input (of an A/D), plus one LSB.

Gain Error – The difference between the actual and expected gain (end point to end point), with respect to the reference, of a data converter. The gain error is usually expressed in LSBs.

Grey Code – Also known as *reflected binary code*, it is a digital code such that each code differs from adjacent codes by only one bit. Since more than one bit is never changed at each transition, race condition errors are eliminated.

Integral Nonlinearity – The maximum error of an A/D, or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningful. This parameter is the best overall indicator of the device′s performance.

Line Regulation – The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.

Load Regulation – The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

LSB – Least Significant Bit. It is the lowest order bit of a binary code.

Monotonicity – The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of an A/D), results in the output never decreasing.

MSB – Most Significant Bit. It is the highest order bit of a binary code.

Natural Binary Code – A binary code defined by:

$$N = A_n2^n + \ldots + A_32^3 + A_22^2 + A_12^1 + A_02^0$$

where each “A” coefficient has a value of 1 or 0. Typically, all zeroes correspond to a zero input voltage of an A/D, and all ones correspond to the most positive input voltage.

Nyquist Theorem – See Sampling Theorem.

Offset Binary Code – Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary, except that all zeros correspond to the most negative input voltage (of an A/D), while all ones correspond to the most positive input.

Power Supply Sensitivity – The change in a data converter′s performance with changes in the power supply voltage(s). This parameter is usually expressed in percent of full scale versus ΔV.

Quantitization Error – Also known as *digitization error* or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of ± 1/2 LSB.

Resolution – The smallest change which can be discerned by an A/D converter, or produced by a DAC. It is usually expressed as the number of bits (n), where the converter has 2^n possible states.

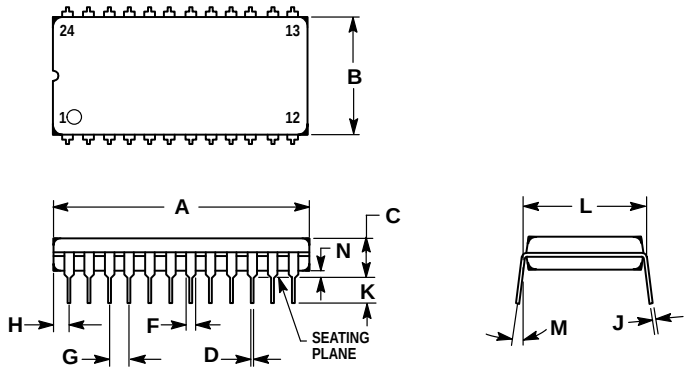
Sampling Theorem – Also known as the *Nyquist Theorem.* It states that the sampling frequency of an A/D must be no less that 2x the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

Unipolar Input – A mode of operation whereby the analog input range (of an A/D), or output range (of a DAC), includes values of a signal polarity. Examples are 0 to + 2.0 V, 0 to – 5.0 V, 2.0 to 8.0 V, etc.

Unipolar Offset Error – The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative input voltage.

OUTLINE DIMENSIONS

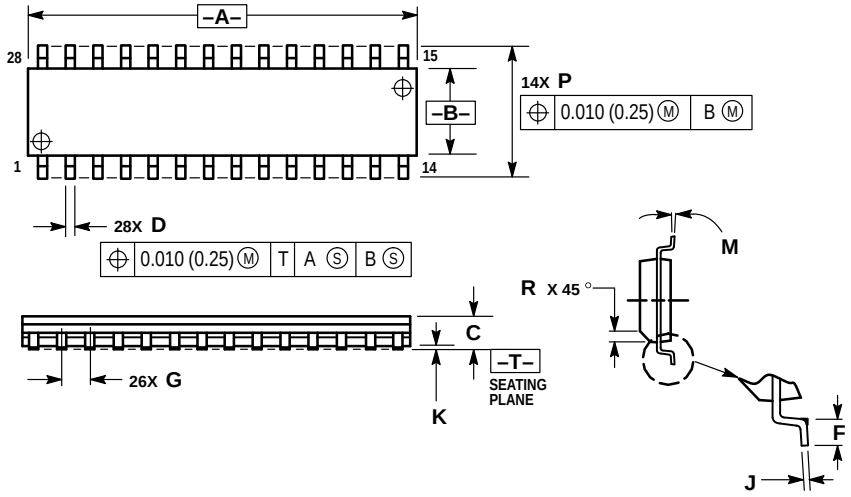
P SUFFIX
PLASTIC PACKAGE
CASE 709–02
ISSUE C



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0 °	15 °	0 °	15 °
N	0.51	1.02	0.020	0.040

DW SUFFIX
PLASTIC PACKAGE
CASE 751F–04
(SO–28L)
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.01	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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