

DATA SHEET

74LVCH16541A

16-bit buffer/line driver (3-State)

Product specification

1998 May 19

IC24 Data Handbook

16-bit buffer/line driver; 5V tolerant I/O (3-State)

74LVCH16541A

FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2 V to 3.6 V
- Drive capability $\pm 24\text{mA}$ @ 3.3V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold
- Bushold inputs eliminate the need for external pull-up resistors to hold unused inputs

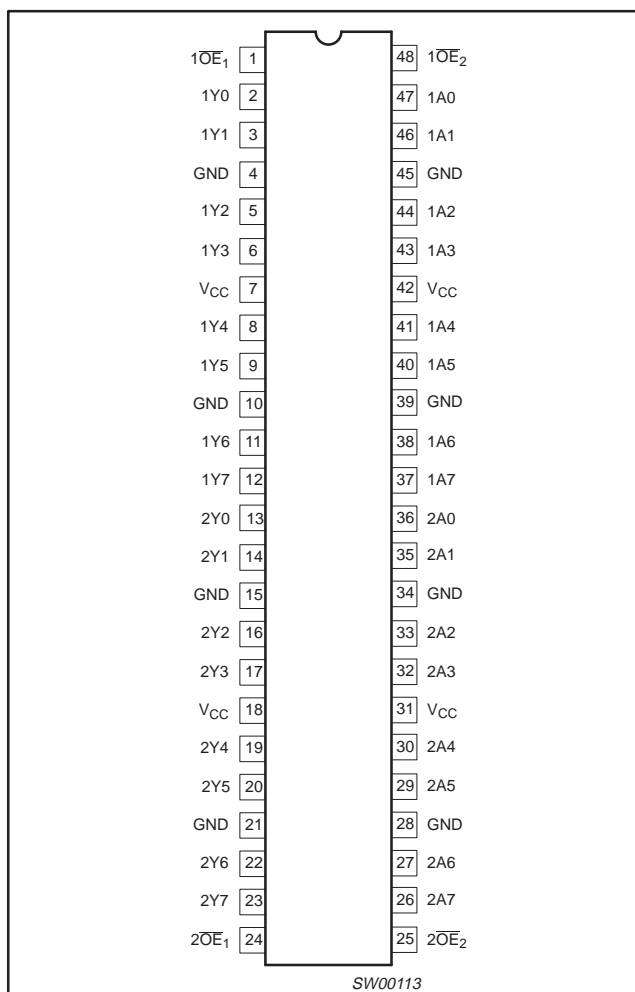
DESCRIPTION

The 74LVCH16541A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVCH16541A is a 16-bit inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs 1OE_n and 2OE_n . A HIGH on $n\text{OE}_n$ causes the outputs to assume a high impedance OFF-state.

To ensure the high impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f \leq 2.5\text{ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	$C_L = 50\text{pF}$ $V_{CC} = 3.3\text{V}$	2.7	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	$V_I = \text{GND to } V_{CC}^1$ outputs enabled output disabled	32 5	pF

NOTES:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW): $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	-40°C to $+85^\circ\text{C}$	74LVCH16541A DL	VCH16541A DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to $+85^\circ\text{C}$	74LVCH16541A DGG	VCH16541A DGG	SOT362-1

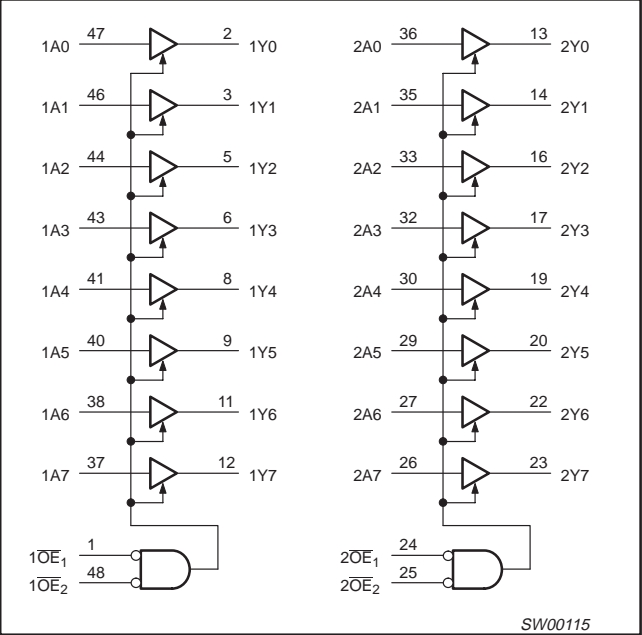
16-bit buffer/line driver; 5V tolerant I/O (3-State)

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PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	$\overline{nOE_1}$	Output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Y0 to 1Y7	Data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2Y0 to 2Y7	Data outputs
25, 48	$\overline{nOE_2}$	Output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	2A0 to 2A7	Data inputs
47, 46, 44, 43, 41, 40, 38, 37	1A0 to 1A7	Data inputs

LOGIC SYMBOL

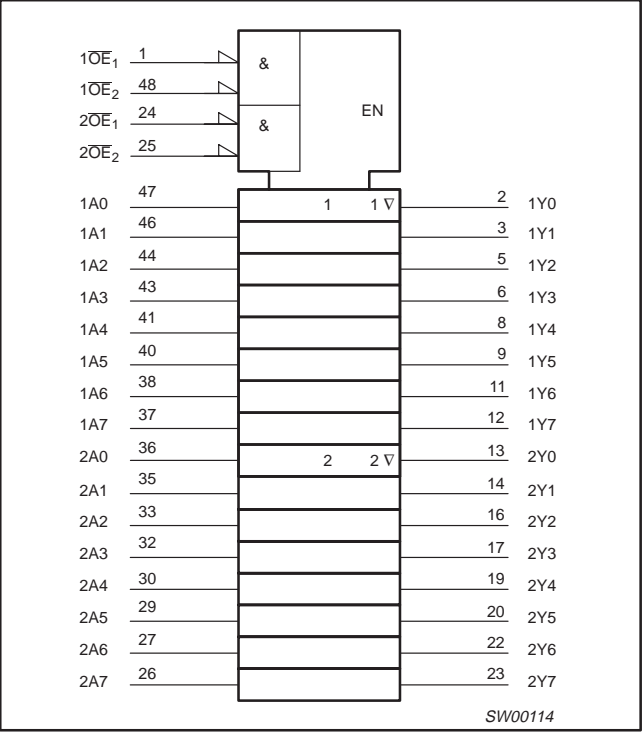


FUNCTION TABLE

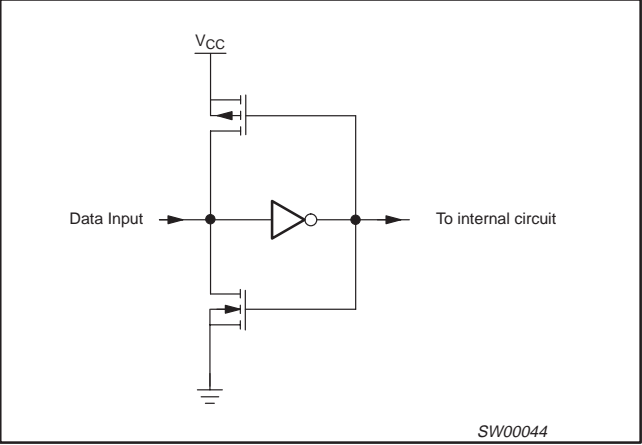
INPUTS			OUTPUT
$\overline{nOE_1}$	$\overline{nOE_2}$	nAn	nYn
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUSHOLD CIRCUIT



16-bit buffer/line driver; 5V tolerant I/O (3-State)

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage (for maximum speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range	For data input pins with bus hold	0	V_{CC}	V
		For data input pins without bus hold	0	5.5	
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free air		-40	+85	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.2$ to $2.7V$ $V_{CC} = 2.7$ to $3.6V$	0 0	20 10	ns/V

ABSOLUTE MAXIMUM VALUES^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage		-0.5	+6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–	-50	mA
V_I	DC input voltage	Note 3	-0.5	+6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 3	-0.5	$V_{CC} + 0.5$	V
	DC output voltage; output 3-State		-0.5	6.5	
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}	–	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		–	±100	mA
T_{stg}	Storage temperature range		-65	+150	°C
P_{tot}	Power dissipation per package – SSOP (plastic medium-shrink) – TSSOP (plastic thin-medium-shrink)	For temperature range: -40 to +125°C above +70°C derate linearly 8mW/K above +60°C derate linearly 5.5mW/K		500 500	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

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DC CHARACTERISTICS

Over recommended operating conditions

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level input voltage	V _{CC} = 1.2V	V _{CC}			V
		V _{CC} = 2.7 to 3.6V	2.0			
V _{IL}	LOW level input voltage	V _{CC} = 1.2V			GND	V
		V _{CC} = 2.7 to 3.6V			0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.7; V _I = V _{IH} or V _{IL} ; I _O = −12mA	V _{CC} -0.5			V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = −100μA	V _{CC} -0.2	V _{CC}		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = −18mA	V _{CC} -0.6			
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = −24mA	V _{CC} -0.8			
V _{OL}	LOW level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA			0.40	V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA			0.20	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA			0.55	
I _I	Input leakage current	V _{CC} = 3.6V; V _I = 5.5V or GND ⁶		± 0.1	± 5	μA
I _{OZ}	3-State output OFF-state current	V _{CC} = 3.6V; V _I = V _{IH} or V _{IL} ; V _O = 5.5V or GND		0.1	± 5	μA
I _{OFF}	Power off leakage current	V _{CC} = 0.0V; V _I or V _O = 5.5V		0.1	±10	μA
I _{CC}	Quiescent supply current	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0		0.1	20	μA
ΔI _{CC}	Additional quiescent supply current given per input pin	V _{CC} = 2.7 to 3.6V; V _I = V _{CC} − 0.6V; I _O = 0		5	500	μA
I _{BHL}	Bus hold LOW sustaining current	V _{CC} = 3.0V; V _I = 0.8V ^{2, 3, 4}	75			μA
I _{BHH}	Bus hold HIGH sustaining current	V _{CC} = 3.0V; V _I = 2.0V ^{2, 3, 4}	−75			μA
I _{BHLO}	Bus hold LOW overdrive current	V _{CC} = 3.6V ^{2, 3, 5}	500			μA
I _{BHHO}	Bus hold HIGH overdrive current	V _{CC} = 3.6V ^{2, 3, 5}	−500			μA

NOTES:

1. All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.
2. Valid for data inputs of bus hold parts (LVCH16-A) only.
3. For data inputs only, control inputs do not have a bus hold circuit.
4. The specified sustaining current at the data input holds the input below the specified V_I level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bus hold parts, the bus hold circuit is switched off when V_I exceeds V_{CC} allowing 5.5V on the input terminal.

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AC CHARACTERISTICS

GND = 0V; $t_R = t_F \leq 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

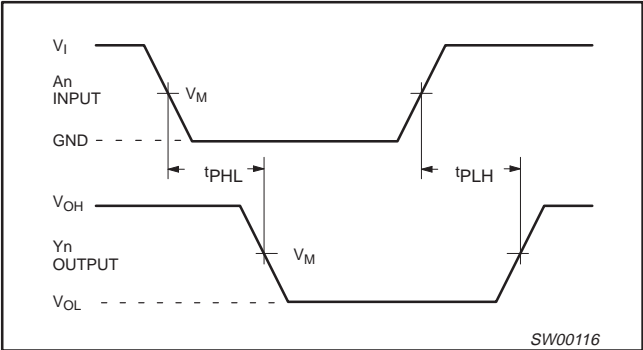
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V _{CC} = 3.3V ±0.3V			V _{CC} = 2.7V		
			MIN	TYP ¹	MAX	MIN	MAX	
t _{PHL} t _{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	1, 3	1.5	2.7	4.5	1.5	5.5	ns
t _{PZH} t _{PZL}	3-State output enable time 1OEn to 1Yn; 2OEn to 2Yn	2, 3	1.5	3.5	5.9	1.5	6.9	ns
t _{PHZ} t _{PLZ}	3-State output disable time 1OEn to 1Yn; 2OEn to 2Yn	2, 3	1.5	3.9	5.5	1.5	6.5	ns

NOTE:

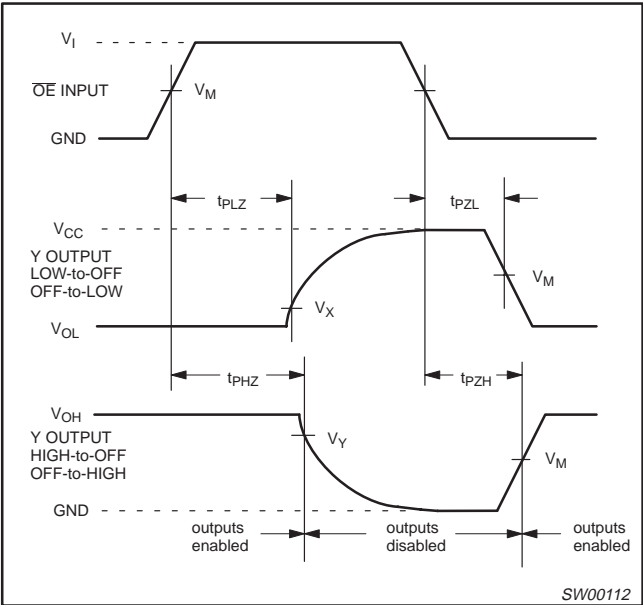
1. All typical values are at $V_{CC} = 3.3\text{V}$ and $T_{\text{amb}} = 25^\circ\text{C}$.

AC WAVEFORMS

$V_M = 1.5\text{V}$ at $V_{CC} \geq 2.7\text{V}$; $V_M = 0.5 V_{CC}$ at $V_{CC} < 2.7\text{V}$.
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_X = V_{OL} + 0.3\text{V}$ at $V_{CC} \geq 2.7\text{V}$; $V_X = V_{OL} + 0.1 V_{CC}$ at $V_{CC} < 2.7\text{V}$
 $V_Y = V_{OH} - 0.3\text{V}$ at $V_{CC} \geq 2.7\text{V}$; $V_Y = V_{OH} - 0.1 V_{CC}$ at $V_{CC} < 2.7\text{V}$

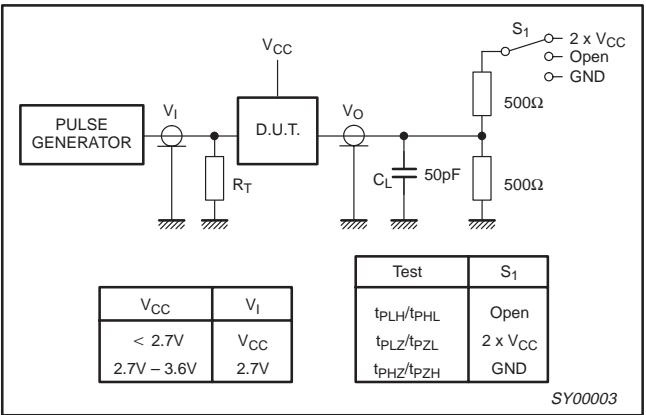


Waveform 1. Input (An) to output (Yn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



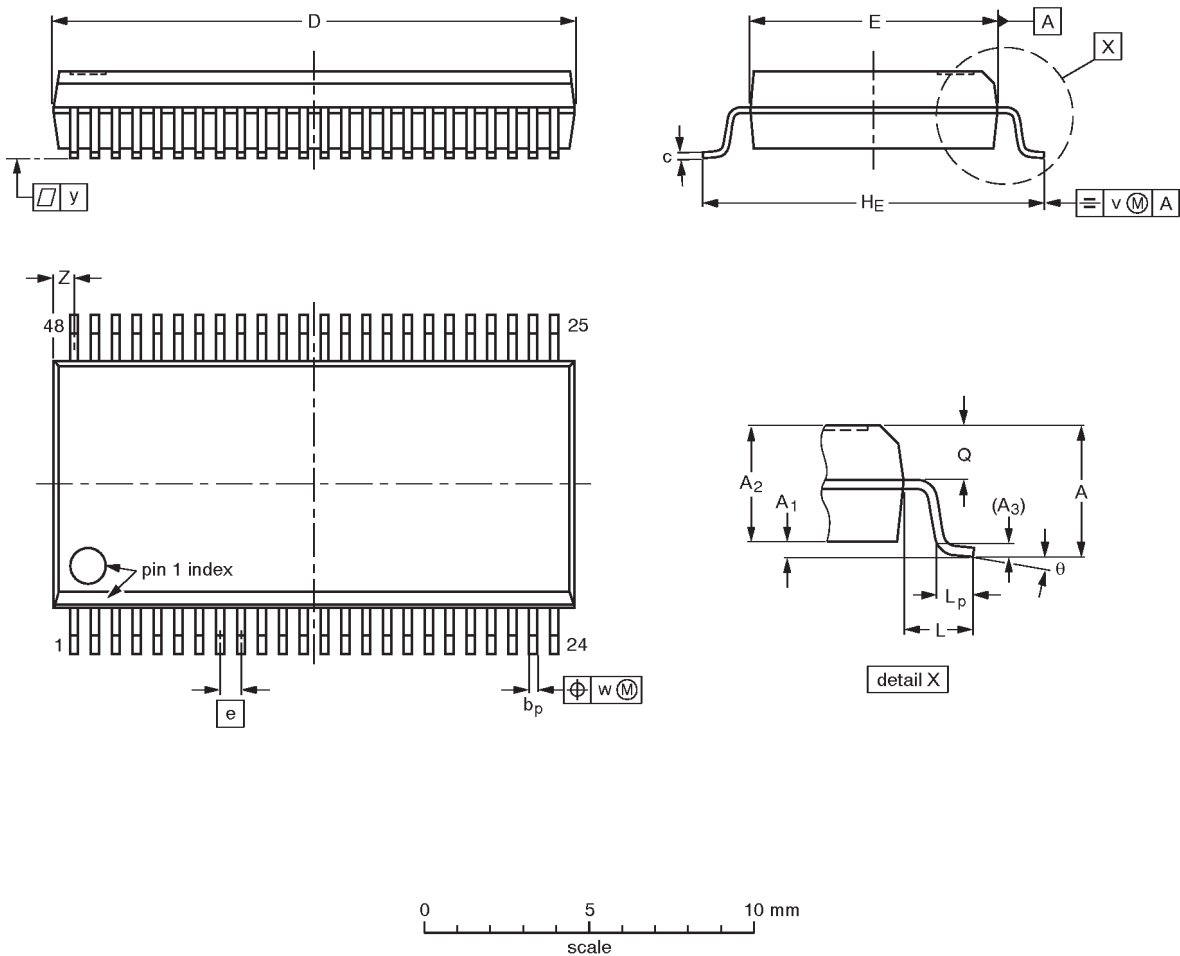
Waveform 3. Load circuitry for switching times

16-bit buffer/line driver (3-State)

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

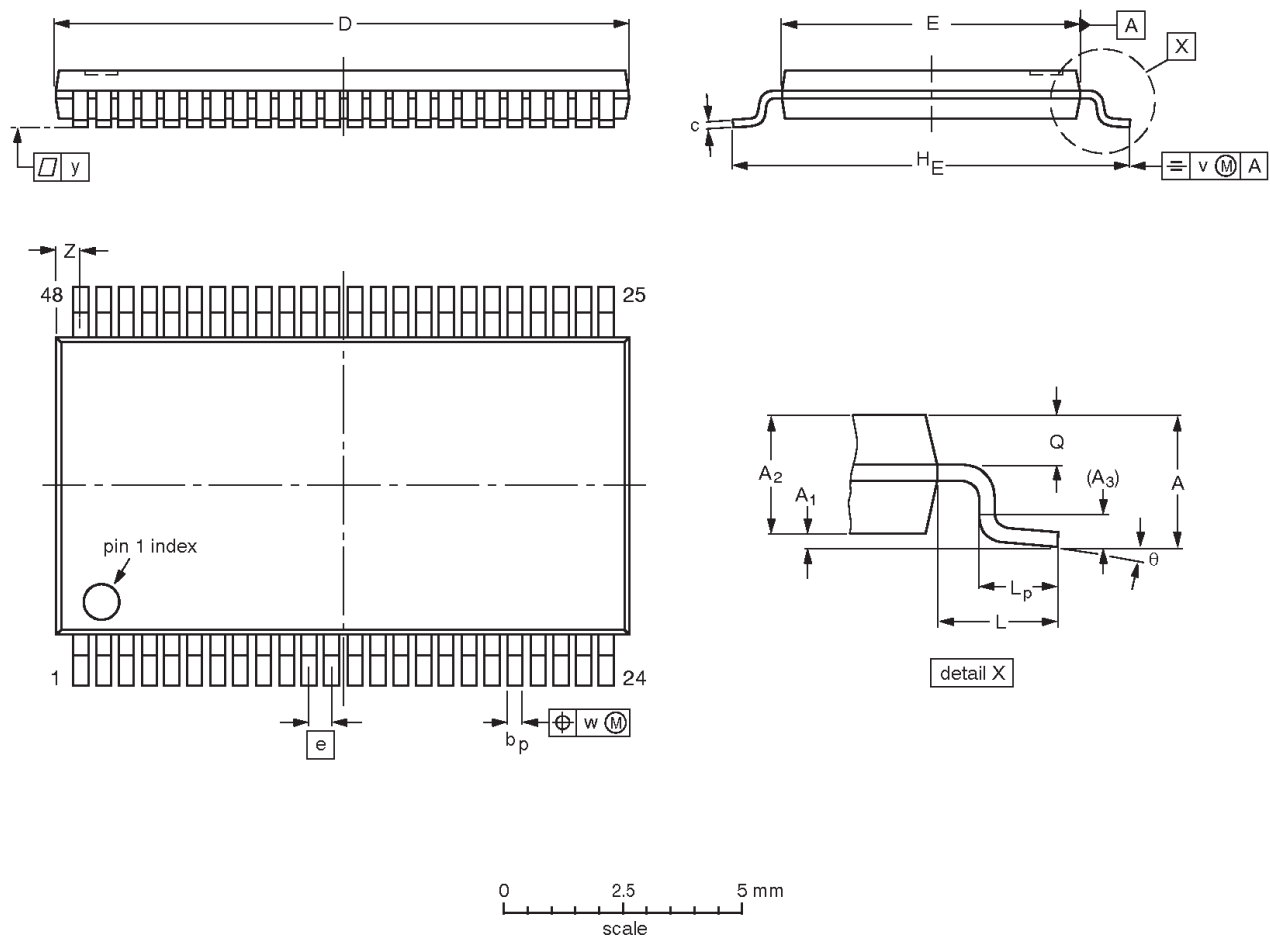
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				-93-11-02- 95-02-04

16-bit buffer/line driver (3-State)

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153ED					93-02-03 95-02-10

16-bit buffer/line driver (3-State)**74LVCH16541A**

NOTES

16-bit buffer/line driver (3-State)

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Data sheet status

Data sheet status	Product status	Definition ^[1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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