Am3341/2841/2841A

64 x 4 Bits First-In First-Out Memories

Distinctive Characteristics

- "Plug-In" replacement for Fairchild 3341
- Asynchronous buffer for up to 64 four-bit words
- Easily expandable to larger buffers

Complex MOS Integrated Circuits

- Am2841 has 1MHz guaranteed data rate
- Am2841A has 1.2MHz guaranteed data rate
- 100% reliability assurance testing in compliance with MIL-STD-883
- Special input circuit provides true TTL compatibility

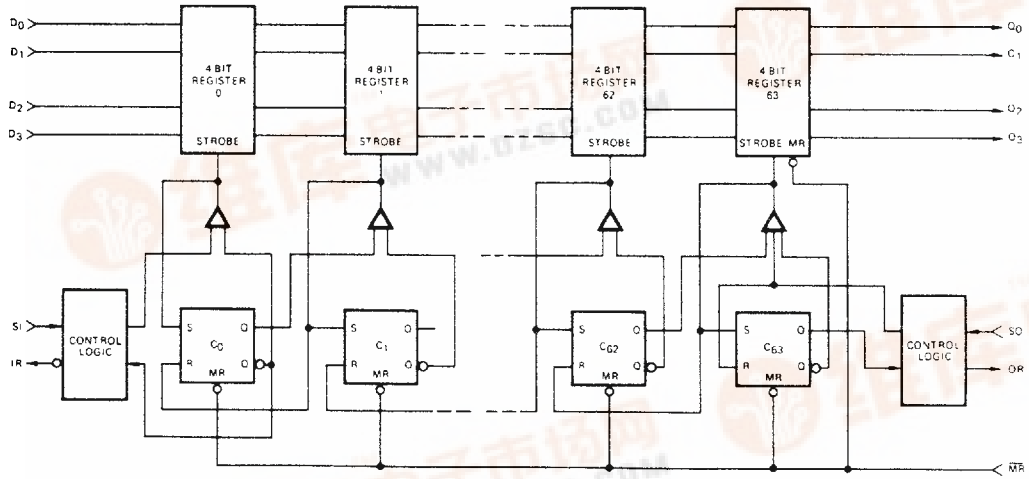
FUNCTIONAL DESCRIPTION

The Am3341/Am2841/Am2841A is an asynchronous first-in first-out memory stack, organized as 64 four-bit words. The device accepts a four-bit parallel word D_0–D_3 under control of the shift in (SI) input. Data entered into the FIFO immediately ripples through the device to the outputs Q_0–Q_3. Up to 64 words may be entered before any words are read from the memory. The stored words line up at the output end in the order in which they were written. A read command on the shift out input (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals act as memory full and memory empty flags and also provide the necessary pulses for interconnecting FIFOs to obtain deeper stacks.

Parallel expansion to wider words only requires that rows of FIFOs be placed side by side.

Reading and writing operations are completely independent, so the device can be used as a buffer between two digital machines operating asynchronously and at widely differing clock rates. Special input circuits are provided on all inputs to pull the input signals up to an MOS V_{IH} when a TTL V_{OH} is reached, providing true TTL compatibility without the inconvenience and extra power drain of external pull-up resistors. A detailed description of the operation is on pages 4 and 5 of this data sheet. The Am2841 and Am2841A are functionally identical to the Am3341, but are higher performance devices.

LOGIC BLOCK DIAGRAM

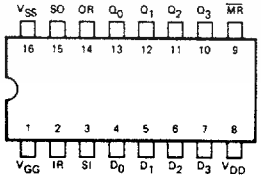


ORDERING INFORMATION

Package Type	Temperature Range	Am3341 Order Number	Am2841 Order Number	Am2841A Order Number
Molded DIP	0°C to +70°C	AM3341PC	AM2841PC	AM2841APC
Hermetic DIP	0°C to +70°C	AM3341DC	AM2841DC	AM2841ADC
Hermetic DIP	−55°C to +125°C		AM2841DM	
Dice	Note	AM3341XX	AM2841XX	AM2841AXX

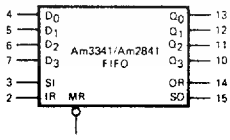
Note:
The dice supplied will contain units which meet both 0°C to +70°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



Notes: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{SS} = Pin 16
V_{GG} = Pin 1
V_{DD} = GND = Pin 8

MAXIMUM RATING (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{DD} Supply Voltage	V_{SS} −7V to V_{SS} +0.3V
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
DC Input Voltage	V_{SS} −10V to V_{SS} +0.3V

OPERATING RANGE

Part No.	Ambient Temperature	V_{SS}	V_{DD}	V_{GG}
Am3341PC, DC Am2841PC, DC Am2841APC, DC	0°C to +70°C	+5.0 ±5%	GND	−12.0 ±5%
Am2841DM	−55°C to +125°C	+5.0 ±5%	GND	−12.0 ±5%

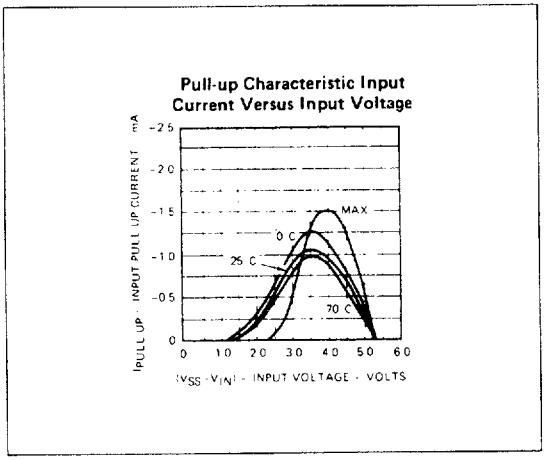
ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = .300mA		V_{SS} −1.0			Volts
V_{OL}	Output LOW Voltage	I_{OL} = 1.6mA				0.4	Volts
V_{IH}	Input HIGH Level			V_{SS} −1.0			Volts
V_{IL}	Input LOW Level					0.8	Volts
I_{IL}	Input Leakage Current	V_{IN} = 0V				1.0	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{SS} −1.0V		250			μA
V_{PUP}	Input Pull-up Initiation Voltage	(Note 2)	V_{SS} = MIN.			2.0	Volts
			V_{SS} = MAX.			2.2	Volts
V_{BAR}	Voltage at Peak Input Current	(Note 2)				V_{SS} −1.5	Volts
I_{BAR}	Maximum Input Current	(Note 2)				1.6	mA
I_{GG}	V_{GG} Current	T_A = 0°C to +70°C			7	12	mA
		T_A = −55°C to +125°C				16	
I_{DD}	V_{DD} Current	T_A = 0°C to +70°C			30	45	mA
		T_A = −55°C to +125°C				60	

Notes: 1. Typical limits are at V_{SS} = 5.0V, V_{GG} = −12.0V, T_A = 25°C
2 See graph of input V I characteristics

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Definition	Test Conditions	Am3341			Am2841			Am2841A			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{max}	Maximum SI or SO Frequency		0.75			1.0			1.2			MHz
t_{IR+}	Delay, SI HIGH to IR LOW		90	250	550	80		400	80		350	ns
t_{IR-}	Delay, SI LOW to IR HIGH		138	275	550	100		550	100		450	ns
t_{OV+}	Minimum Time SI and IR both HIGH		100					80			80	ns
t_{OV-}	Minimum Time SI and IR both LOW		100					80			80	ns
t_{DSI}	Data Release Time		400					200			200	ns
t_{DD}	Data Set-up Time		25			0			0			ns
t_{OR+}	Delay, SO HIGH to OR LOW		90	250	500	70	200	450	80	200	370	ns
t_{OR-}	Delay, SO LOW to OR HIGH		170	350	850	70	200	550	70	200	450	ns
t_{PT}	Ripple through Time	FIFO Empty		10	32		8	16		8	16	μs
t_{DH}	Delay, OR LOW to Data Out	SO = LOW	75			75			75			ns
t_{MRW}	Minimum Reset Pulse Width				400			400			400	ns
t_{DA}	Delay, Data Out to OR HIGH	SO = HIGH	0	30		0	20		0	20		ns
CI	Input Capacitance (Except $\overline{MR}$)				7			7			7	pF
C_{MR}	Input Capacitance $\overline{MR}$				15			7			7	pF



DESCRIPTION OF THE Am3341 FIFO OPERATION

The Am3341 FIFO consists internally of 64 four-bit data registers and one 64-bit control register, as shown in the logic block diagram. A "1" in a bit of the control register indicates that a four-bit data word is stored in the corresponding data register. A "0" in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the n^{th} bit of the control register contains a "1" and the (n+1)th bit contains a "0", then a strobe is generated causing the (n+1)th data register to read the contents of the n^{th} data register, simultaneously setting the (n+1)th control register bit and clearing the n^{th} control register bit, so that the control flag moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are "empty" locations ahead of it. The fall through operation stops when the data reaches a register n with a "1" in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the four data inputs D_0–D_3 by applying a LOW-to-HIGH transition on the shift in (SI) input. A "1" is placed in the first control register bit simultaneously. The first control register bit is returned, buffered, to the input ready (IR) output, and this pin goes LOW indicating that data has been entered into the first data register and the input is now "busy", unable to accept more data. When SI next goes LOW, the fall-through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This causes IR to go HIGH, indicating the inputs are available for

The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A HIGH on OR indicates there is a "1" in the last control register bit and therefore there is valid data on the four data outputs Q_0–Q_3. An input signal, shift out (SO), is used to shift the data out of the FIFO. A LOW-to-HIGH transition on SO clears the last register bit, causing OR to go LOW, indicating that the data on the outputs may no longer be valid. When SO goes LOW, the "0" which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The "0" in the control register then "bubbles" back toward the input as the data shifts toward the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and SO goes HIGH, OR will go LOW as before, but when SO next goes LOW, there is no data to move into the last location, so OR remains LOW until more data arrives at the output. Similarly, when the memory is full data written into the first location will not shift into the second when SI goes LOW, and IR will remain LOW instead of returning to a HIGH state.

The pairs of input and output control signals are designed so that the SO input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the SI input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFOs to operate together, as shown in the application on the last page.

An over-riding master reset ($\overline{MR}$) is used to reset all control register bits and remove the data from the output (i.e. reset the

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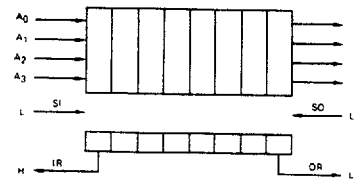

INITIAL CONDITION

FIFO empty, SI LOW IR HIGH, word "A" on inputs.

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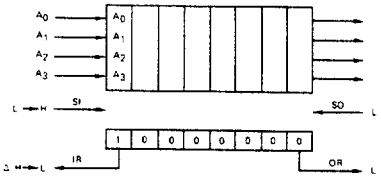
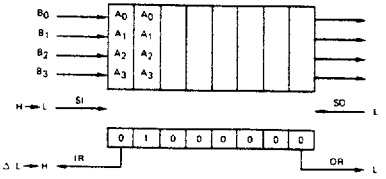


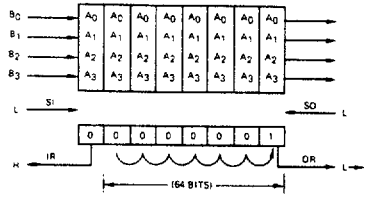
Write input into first stage by raising SI. (Δ = delay) IR goes LOW indicating data has been entered.

3



Release data into FIFO by lowering SI. After delay, data moves to second location, and IR goes HIGH indicating input available for new data word.

4



Data spontaneously ripple through registers to end of FIFO, causing OR to go HIGH. The time required for data to fall completely through the FIFO is the "Ripple-through Time".

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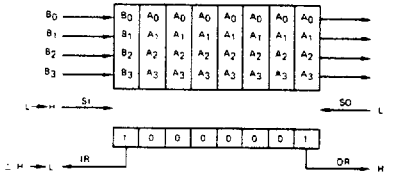

Word "B" written into FIFO

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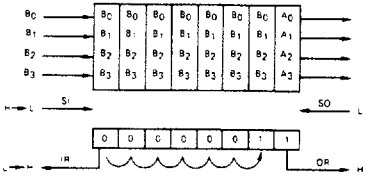

SI goes LOW allowing word "B" to fall through.

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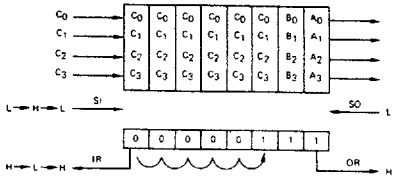
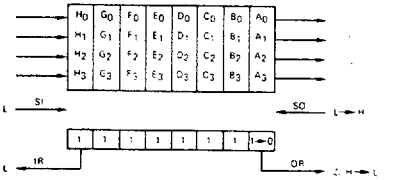


Word "C" written in same manner, and so on. When buffer is full, all control bits are 1's and IR stays LOW.

8



FIRST READ OPERATION

SO goes HIGH, indicating "Ready to Read". OR then goes LOW indicating "Data Read".

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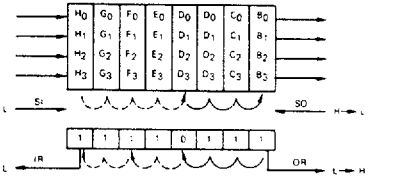

When SO goes LOW, the "0" in the last control bit bubbles toward the memory input. OR goes HIGH as the new word arrives at the output. IR goes HIGH when "0" reaches input.

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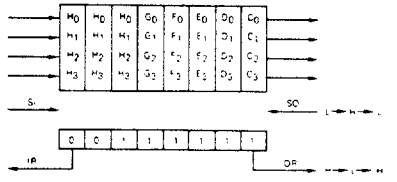

Read word "B" out, word "C" moves to output, and so on.

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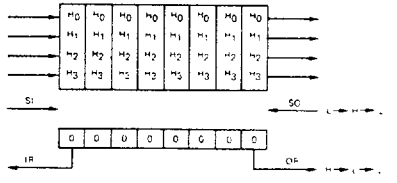
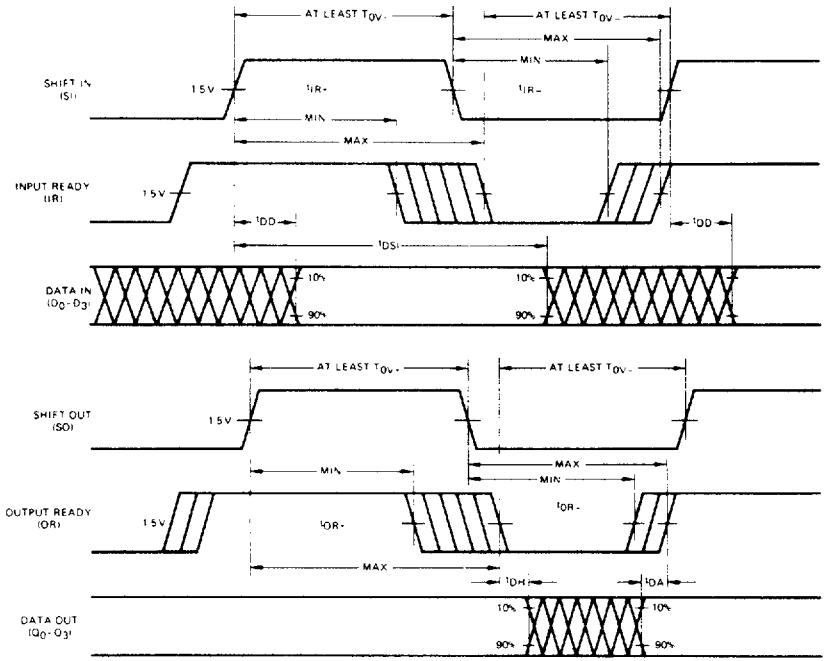


Read word "H". OR stays LOW because FIFO is empty. Word "H" remains in output until new word falls through.

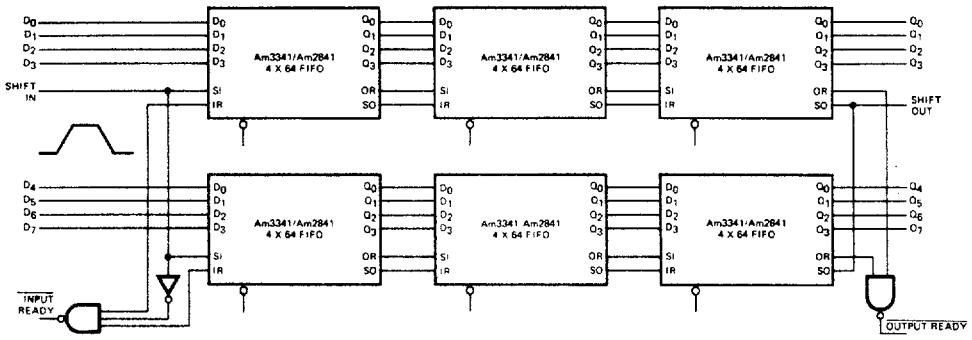
TIMING DIAGRAM



USER NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and always stays LOW until after the new data has appeared on the outputs, so anytime OR is HIGH, there is good, stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go HIGH for one internal cycle (at least t_{OR+}) and then will go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the control register and the outputs are cleared. IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, then IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.

APPLICATION

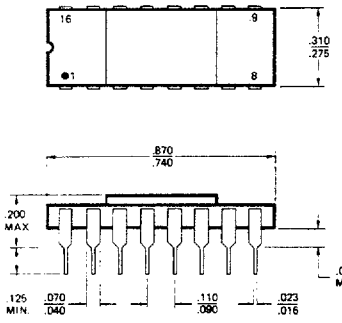


The composite input ready indicates both devices are ready to receive data. The shift in pulse must be wide enough for all devices to load data under worst case conditions.

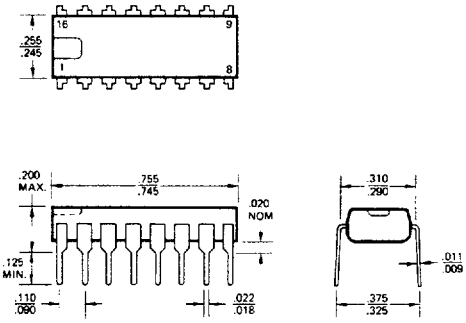
8 X 192 FIFO Buffer Using Am3341/Am2841

PHYSICAL DIMENSIONS
Dual-In-Line

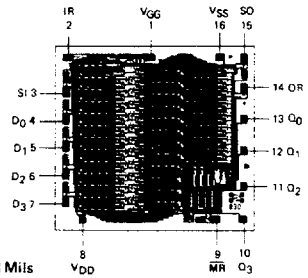
16-Pin Side Brazed



16-Pin Molded



Metallization and Pad Layout



126 x 138 Mils