

MAXIM

Differential LVPECL/LVECL/HSTL Receiver/Drivers

MAX9321/MAX9321A

General Description

The MAX9321/MAX9321A are low-skew differential receiver/drivers designed for clock and data distribution. The differential input can be adapted to accept a single-ended input by connecting the on-chip VBB supply to an input as a reference voltage.

The MAX9321/MAX9321A feature ultra-low propagation delay (172ps) and part-to-part skew (20ps) with 24mA maximum supply current, making these devices ideal for clock buffering or repeating. For interfacing to differential HSTL and LVPECL signals, these devices operate over a +2.25V to +3.8V supply range, allowing high-performance clock and data distribution in systems with a nominal +2.5V or +3.3V supply. For differential LVECL operation, these devices operate from a -2.25V to -3.8V supply. Multiple pinouts are provided to simplify routing across a backplane to either side of a double-sided board.

Both devices are offered in space-saving 8-pin SOT23, SO, and μMAX packages.

Applications

Precision Clock Buffers

Low-Jitter Data Repeaters

Features

- ◆ Improved Second Source of the MC10LVEP16 (MAX9321)
- ◆ +2.25V to +3.8V Differential HSTL/LVPECL Operation
- ◆ -2.25V to -3.8V Differential LVECL Operation
- ◆ Low 17mA Supply Current
- ◆ 20ps Part-to-Part Skew
- ◆ 172ps Propagation Delay
- ◆ Minimum 300mV Output at 3GHz
- ◆ Output Low for Open Input
- ◆ ESD Protection >2kV (Human Body Model)
- ◆ On-Chip Reference for Single-Ended Input
- ◆ Available in Thermally Enhanced Exposed-Pad SO Package

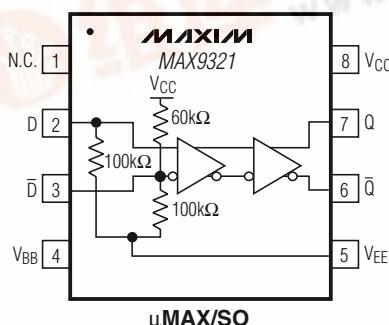
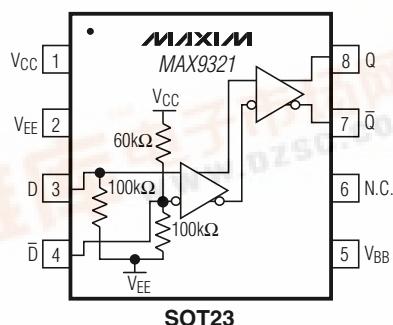
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX9321EKA-T	-40°C to +85°C	8 SOT23-8	AALK
MAX9321EUA*	-40°C to +85°C	8 μMAX	—
MAX9321ESA	-40°C to +85°C	8 SO	—
MAX9321AEKA-T	-40°C to +85°C	8 SOT23-8	AAIX
MAX9321AEUA*	-40°C to +85°C	8 μMAX	—
MAX9321AES	-40°C to +85°C	8 SO-EP**	—

*Future product—contact factory for availability.

**EP = Exposed pad.

Pin Configurations



Pin Configurations continued at end of data sheet.

Differential LVPECL/LVECL/HSTL Receiver/Drivers

ABSOLUTE MAXIMUM RATINGS

V _{CC} to V _{EE}	+4.1V
D or \bar{D}	V _{EE} - 0.3V to V _{CC} + 0.3V
D to \bar{D}	±3.0V
Continuous Output Current	50mA
Surge Output Current	100mA
V _{BB} Sink/Source Current	±0.6mA
Junction-to-Ambient Thermal Resistance in Still Air	
8-Pin SOT23	+112°C/W
8-Pin μ MAX	+221°C/W
8-Pin SO-EP	+53°C/W
Junction-to-Ambient Thermal Resistance with	
500 LPFM Airflow	
8-Pin SOT23	+78°C/W
8-Pin μ MAX	+155°C/W
8-Pin SO	+99°C/W

Junction-to-Case Thermal Resistance	
8-Pin SOT23	+80°C/W
8-Pin μ MAX	+39°C/W
8-Pin SO	+40°C/W
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
ESD Protection	
Human Body Model (D, \bar{D} , Q, \bar{Q} , V _{BB})	>2kV
Soldering Temperature (10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = +2.25V to +3.8V, outputs loaded with 50Ω ±1% to V_{CC} - 2.0V. Typical values are at V_{CC} - V_{EE} = +3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 1–5)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIFFERENTIAL INPUT (D, \bar{D})												
Single-Ended Input High Voltage	V _{IH}	V _{BB} connected to \bar{D} (V _{IL} for V _{BB} connected to D), Figure 1	V _{CC} - 1.210	V _{CC}	V _{CC} - 1.145	V _{CC}	V _{CC} - 1.085	V _{CC}	V			
Single-Ended Input Low Voltage	V _{IL}	V _{BB} connected to \bar{D} (V _{IH} for V _{BB} connected to D), Figure 1	V _{EE}	V _{CC} - 1.65	V _{EE}	V _{CC} - 1.545	V _{EE}	V _{CC} - 1.485	V			
High Voltage of Differential Input	V _{IHD}		V _{EE} + 1.2	V _{CC}	V _{EE} + 1.2	V _{CC}	V _{EE} + 1.2	V _{CC}	V			
Low Voltage of Differential Input	V _{ILD}		V _{EE}	V _{CC} - 0.1	V _{EE}	V _{CC} - 0.1	V _{EE}	V _{CC} - 0.1	V			
Differential Input Voltage	V _{IHD} - V _{ILD}	For V _{CC} - V _{EE} < 3.0V	0.1	V _{CC} - V _{EE}	0.1	V _{CC} - V _{EE}	0.1	V _{CC} - V _{EE}	V			
		For V _{CC} - V _{EE} ≥ 3.0V	0.1	3.0	0.1	3.0	0.1	3.0				
Input High Current	I _{IH}			150		150		150	150	150	μA	
D Input Low Current	I _{ILD}		-10	100	-10	100	-10	100	100	100	μA	
\bar{D} Input Low Current	I _{ILD}		-150	+150	-150	+150	-150	+150	+150	+150	μA	

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} - V_{EE} = +2.25V$ to $+3.8V$, outputs loaded with $50\Omega \pm 1\%$ to $V_{CC} - 2V$. Typical values are at $V_{CC} - V_{EE} = +3.3V$, $V_{IHD} = V_{CC} - 1V$, $V_{ILD} = V_{CC} - 1.5V$, unless otherwise noted.) (Notes 1–5)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIFFERENTIAL OUTPUT (Q, \bar{Q})												
Single-Ended Output High Voltage	V_{OH}	Figure 1	$V_{CC} - 1.135$	$V_{CC} - 0.885$	$V_{CC} - 1.07$	$V_{CC} - 0.82$	$V_{CC} - 1.01$	$V_{CC} - 0.76$	V			
Single-Ended Output Low Voltage	V_{OL}	Figure 1	$V_{CC} - 1.935$	$V_{CC} - 1.685$	$V_{CC} - 1.87$	$V_{CC} - 1.62$	$V_{CC} - 1.81$	$V_{CC} - 1.56$	V			
Differential Output Voltage	$V_{OH} - V_{OL}$	Figure 1	550	550	550	550	550	550	mV			
REFERENCE (V_{BB})												
Reference Voltage Output (Note 6)	V_{BB}	$I_{BB} = \pm 0.5mA$	$V_{CC} - 1.55$	$V_{CC} - 1.31$	$V_{CC} - 1.445$	$V_{CC} - 1.245$	$V_{CC} - 1.385$	$V_{CC} - 1.185$	V			
POWER SUPPLY												
Supply Current (Note 7)	I_{EE}		16	24	17	24	18	24	mA			

AC ELECTRICAL CHARACTERISTICS

($V_{CC} - V_{EE} = +2.25V$ to $+3.8V$, outputs loaded with $50\Omega \pm 1\%$ to $V_{CC} - 2V$, input frequency = 1.5GHz, input transition time = 125ps (20% to 80%), $V_{IHD} = V_{EE} + 1.2V$ to V_{CC} , $V_{ILD} = V_{EE}$ to $V_{CC} - 0.15V$, $V_{IHD} - V_{ILD} = 0.15V$ to the smaller of 3V or $V_{CC} - V_{EE}$. Typical values are at $V_{CC} - V_{EE} = 3.3V$, $V_{IHD} = V_{CC} - 1V$, $V_{ILD} = V_{CC} - 1.5V$, unless otherwise noted.) (Notes 8, 11)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input-to-Output Delay	t_{PLHD} , t_{PHLD}	Figure 2	145	184	235	145	172	245	130	167	230	ps
Part-to-Part Skew (Note 9)	t_{SKPP}		25	90	20	100	20	100	20	100	20	ps
Added Random Jitter (Note 10)	t_{RJ}	$f_{IN} = 1.5GHz$, Clock pattern	1.7	2.8	1.7	2.8	1.7	2.8	1.7	2.8	1.7	ps (RMS)
		$f_{IN} = 3.0GHz$, Clock pattern	0.6	1.5	0.6	1.5	0.6	1.5	0.6	1.5	0.6	

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AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} - V_{EE} = +2.25V$ to $+3.8V$, outputs loaded with $50\Omega \pm 1\%$ to $V_{CC} - 2V$, input frequency = 1.5GHz , input transition time = 125ps (20% to 80%), $V_{IHD} = V_{EE} + 1.2V$ to V_{CC} , $V_{ILD} = V_{EE}$ to $V_{CC} - 0.15V$, $V_{IHD} - V_{ILD} = 0.15V$ to the smaller of $3V$ or $V_{CC} - V_{EE}$. Typical values are at $V_{CC} - V_{EE} = 3.3V$, $V_{IHD} = V_{CC} - 1V$, $V_{ILD} = V_{CC} - 1.5V$, unless otherwise noted.) (Notes 8, 11)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Added Deterministic Jitter (Note 10)	t_{DJ}	3.0Gbps 2^{23} -1 PRBS pattern		57	80		57	80		57	80	ps (p-p)
Switching Frequency	f_{MAX}	$V_{OH} - V_{OL} \geq 300\text{mV}$, Clock pattern, Figure 2	3.0			3.0			3.0			GHz
		$V_{OH} - V_{OL} \geq 550\text{mV}$, Clock pattern, Figure 2		2.0			2.0			2.0		
Output Rise/Fall Time (20% to 80%)	t_R, t_F	Figure 2	50	88	120	50	89	120	50	90	120	ps

Note 1: Guaranteed by design and characterization.

Note 2: Measurements are made with the device in thermal equilibrium.

Note 3: Current into a pin is defined as positive. Current out of a pin is defined as negative.

Note 4: DC parameters production tested at $T_A = +25^\circ\text{C}$. Guaranteed by design and characterization over the full operating temperature range.

Note 5: Single-ended input operation is limited to $V_{CC} - V_{EE} \geq 3.0V$.

Note 6: Use V_{BB} as a reference for inputs on the same device only.

Note 7: All pins open except V_{CC} and V_{EE} .

Note 8: Guaranteed by design and characterization. Limits are set at ± 6 sigma.

Note 9: Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.

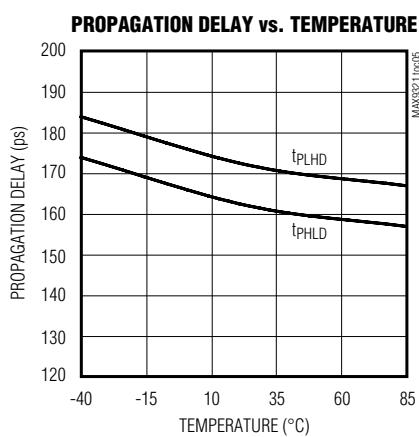
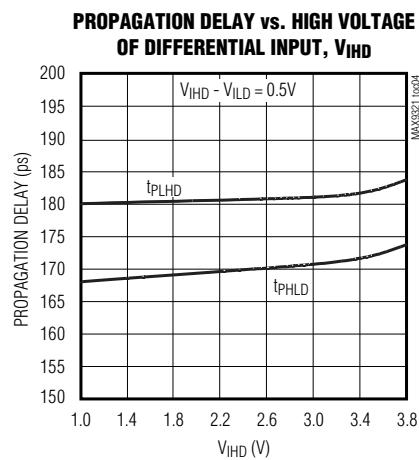
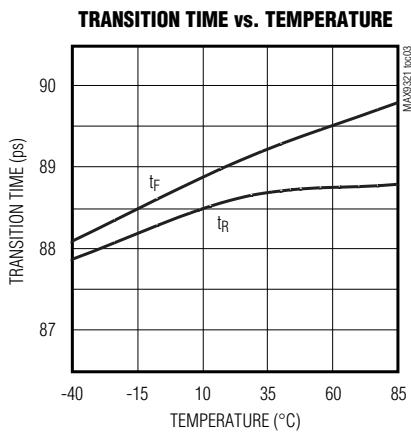
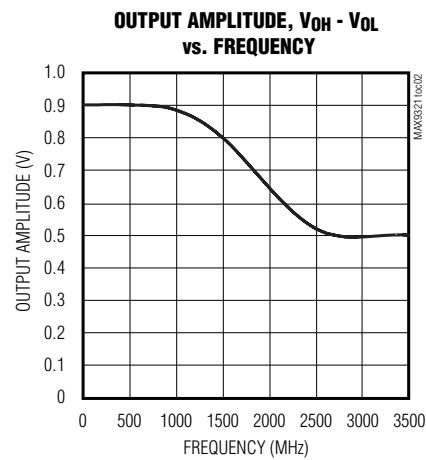
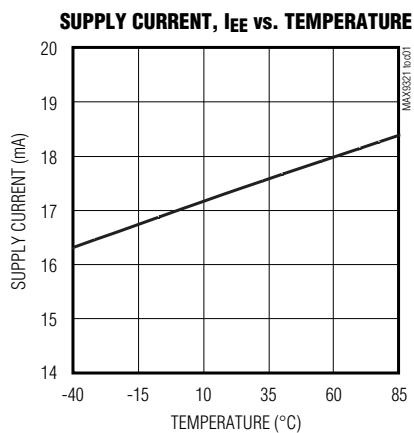
Note 10: Device jitter added to the input signal.

Differential LVPECL/LVECL/HSTL Receiver/Drivers

Typical Operating Characteristics

(SO packages) ($V_{CC} = +3.3V$, $V_{EE} = 0$, input transition time = 125ps (20% to 80%), $V_{IH} = V_{CC} - 1V$, $V_{IL} = V_{CC} - 1.5V$, $f_{IN} = 1.5GHz$, outputs loaded with 50Ω to $V_{CC} - 2V$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX9321/MAX9321A



Differential LVPECL/LVECL/HSTL Receiver/Drivers

Pin Description (MAX9321)

PIN		NAME	FUNCTION
μ MAX/SO	SOT23		
1	6	N.C.	No Connection
2	3	D	Noninverting Differential Input. 100k Ω pulldown to V _{EE} .
3	4	\bar{D}	Inverting Differential Input. 60k Ω pullup to V _{CC} and 100k Ω pulldown to V _{EE} .
4	5	V _{BB}	Reference Output Voltage. Connect to the inverting or noninverting input to provide a reference for single-ended operation. When used, bypass with a 0.01 μ F ceramic capacitor to V _{CC} ; otherwise leave open.
5	2	V _{EE}	Negative Supply Voltage
6	7	\bar{Q}	Inverting Output. Typically terminate with 50 Ω resistor to V _{CC} - 2V.
7	8	Q	Noninverting Output. Typically terminate with 50 Ω resistor to V _{CC} - 2V.
8	1	V _{CC}	Positive Supply Voltage. Bypass from V _{CC} to V _{EE} with 0.1 μ F and 0.01 μ F ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.

Pin Description (MAX9321A)

PIN		NAME	FUNCTION
μ MAX/SO	SOT23		
1	6	N.C.	No Connection
2	3	\bar{D}	Inverting Differential Input. 60k Ω pullup to V _{CC} and 100k Ω pulldown to V _{EE} .
3	4	D	Noninverting Differential Input. 100k Ω pulldown to V _{EE} .
4	5	V _{BB}	Reference Output Voltage. Connect to the inverting or noninverting input to provide a reference for single-ended operation. When used, bypass with a 0.01 μ F ceramic capacitor to V _{CC} ; otherwise leave open.
5	2	V _{EE}	Negative Supply Voltage
6	8	Q	Noninverting Output. Typically terminate with 50 Ω resistor to V _{CC} - 2V.
7	7	\bar{Q}	Inverting Output. Typically terminate with 50 Ω resistor to V _{CC} - 2V.
8	1	V _{CC}	Positive Supply Voltage. Bypass from V _{CC} to V _{EE} with 0.1 μ F and 0.01 μ F ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.

Differential LVPECL/LVECL/HSTL Receiver/Drivers

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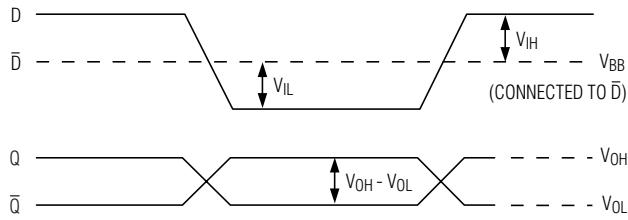


Figure 1. Switching with Single-Ended Input

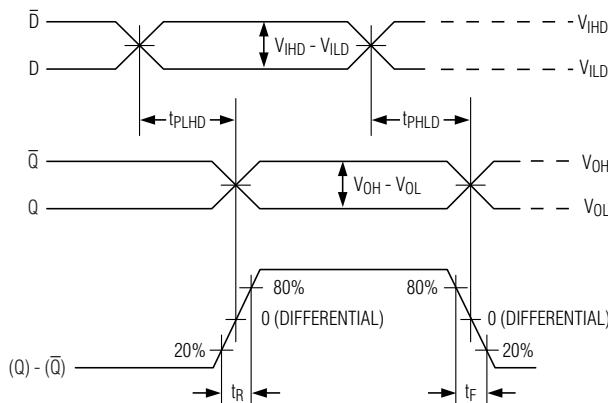


Figure 2. Differential Transition Time and Propagation Delay Timing Diagram

Detailed Description

The MAX9321/MAX9321A are low-skew differential receiver/drivers designed for clock and data distribution. For interfacing to differential HSTL and LVPECL signals, these devices operate over a +2.25V to +3.8V supply range, allowing high-performance clock and data distribution in systems with a nominal +2.5V or +3.3V supply. For differential LVECL operation, these devices operate from a -2.25V to -3.8V supply.

Inputs

The differential input can be configured to accept a single-ended input when operating at approximately $V_{CC} - V_{EE} = 3.0V$ to $3.8V$. This is accomplished by connecting the on-chip reference voltage, V_{BB} , to an input as a reference. For example, the differential D, \bar{D} input is converted to a noninverting, single-ended input by connecting V_{BB} to \bar{D} and connecting the single-ended input to D. An inverting input is obtained by connecting

V_{BB} to D and connecting the single-ended input to \bar{D} . With the differential input configured as single ended (using V_{BB}), the single-ended input can be driven to V_{CC} and V_{EE} or with a single-ended LVPECL/LVECL signal.

When the differential input is configured as a single-ended input (using V_{BB}), the approximate supply range is $V_{CC} - V_{EE} = 3.0V$ to $3.8V$. This is because one of the inputs must be $V_{EE} + 1.2V$ or higher for proper operation of the input stage. V_{BB} must be at least $V_{EE} + 1.2V$ because it becomes the high-level input when the other (single-ended) input swings below it. Therefore, minimum $V_{BB} = V_{EE} + 1.2V$.

The minimum V_{BB} output is $V_{CC} - 1.510V$. Substituting the minimum V_{BB} into $V_{BB} = V_{EE} + 1.2V$ results in a minimum supply of $2.71V$. Rounding up to a standard supply gives the single-ended operating supply range of $V_{CC} - V_{EE} = 3.0V$ to $3.8V$.

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When using the VBB reference output, bypass it with a $0.01\mu\text{F}$ ceramic capacitor to VCC. If the VBB reference is not used, it can be left open. The VBB reference can source or sink 0.5mA . Use VBB only for an input on the same device as the VBB reference.

The maximum magnitude of the differential input from D to \bar{D} is 3.0V or $\text{VCC} - \text{VEE}$, whichever is less. This limit also applies to the difference between any reference voltage input and a single-ended input.

The differential input has bias resistors that drive the output to a differential low when the inputs are open. The inverting input is biased with a $60\text{k}\Omega$ pullup to VCC and a $100\text{k}\Omega$ pulldown to VEE. The noninverting input is biased with a $100\text{k}\Omega$ pulldown to VEE.

Specifications for the high and low voltage of the differential input (VIHD and VILD) and the differential input voltage ($\text{VIHD} - \text{VILD}$) apply simultaneously (VILD cannot be higher than VIHD).

Outputs

Output levels are referenced to VCC and are considered LVPECL or LVECL, depending on the level of the VCC supply. With VCC connected to a positive supply and VEE connected to GND, the output is LVPECL. The output is LVECL when VCC is connected to GND and VEE is connected to a negative supply.

A single-ended input of at least $\text{VBB} \pm 100\text{mV}$ or a differential input of at least $\pm 100\text{mV}$ switches the outputs to the VOH and VOL levels specified in the *DC Electrical Characteristics* table.

Applications Information

Supply Bypassing

Bypass VCC to VEE with high-frequency surface-mount ceramic $0.1\mu\text{F}$ and $0.01\mu\text{F}$ capacitors in parallel as close to the device as possible, with the $0.01\mu\text{F}$ value

capacitor closest to the device. Use multiple parallel vias for low inductance. When using the VBB reference output, bypass it with a $0.01\mu\text{F}$ ceramic capacitor to VCC (if the VBB reference is not used, it can be left open).

Traces

Input and output trace characteristics affect the performance of the MAX9321/MAX9321A. Connect each signal of a differential input or output to a 50Ω characteristic impedance trace. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and across cables. Reduce skew within a differential pair by matching the electrical length of the traces.

The exposed-pad (EP) SO package can be soldered to the PC board for enhanced thermal performance. If the EP is not soldered to the PC board, the thermal resistance is the same as the regular SO package. The EP is connected to the chip VEE supply. Be sure that the pad does not touch signal lines or other supplies.

Contact Maxim's Packaging department for guidelines on the use of EP packages.

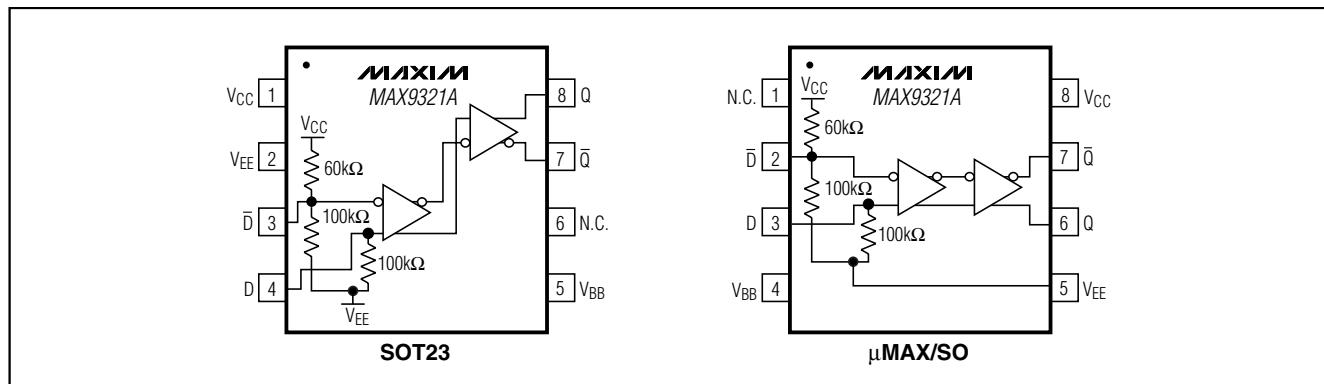
Output Termination

Terminate outputs through 50Ω to $\text{VCC} - 2\text{V}$ or use an equivalent Thevenin termination. When a single-ended signal is taken from the differential output, terminate both outputs. For example, when Q is used as a single-ended output, terminate both Q and \bar{Q} .

Chip Information

TRANSISTOR COUNT: 162

Pin Configurations (continued)

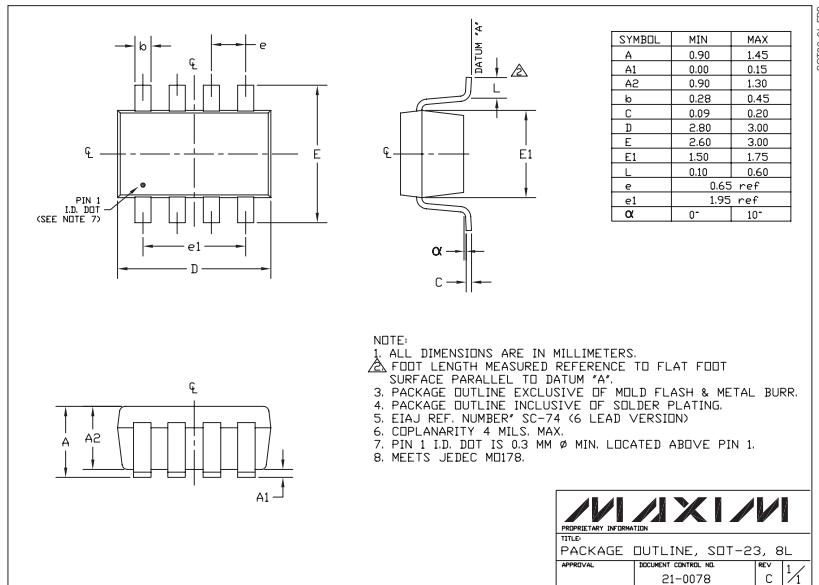


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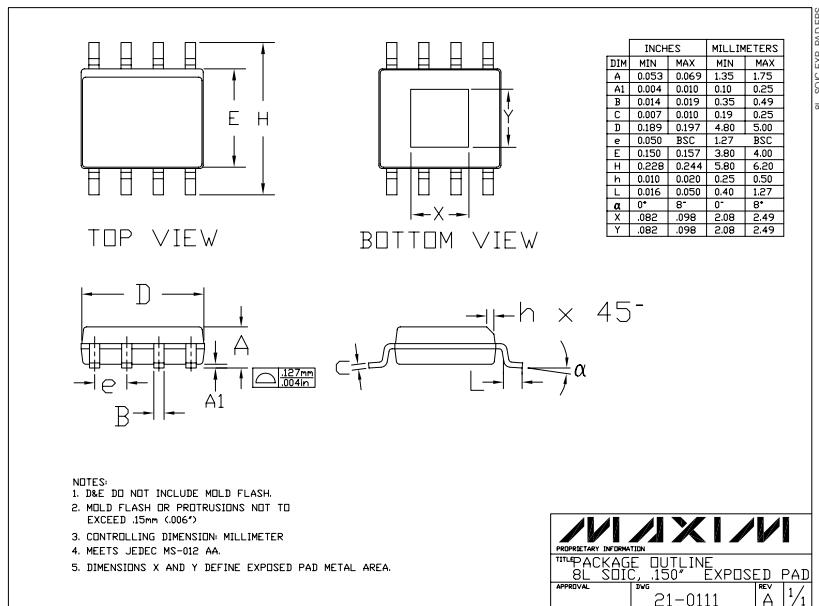
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX9321/MAX9321A



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED REFERENCE TO FLAT FOOT SURFACE PARALLEL TO DATUM "A".
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. EIAJ REF. NUMBER: SC-74 (6 LEAD VERSION)
6. COPLANARITY 4 MILS. MAX.
7. PIN 1 I.D. DOT IS 0.3 MM Ø MIN. LOCATED ABOVE PIN 1.
8. MEETS JEDEC MO178.



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