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CD4051BMS, CD4052BMS CD4053BMS

CMOS Analog Multiplexers/Demultiplexers*

December 1992

Features

- **Logic Level Conversion**
- **High-Voltage Types (20V Rating)**
- **CD4051BMS Signal 8-Channel**
- **CD4052BMS Differential 4-Channel**
- **CD4053BMS Triple 2-Channel**
- **Wide Range of Digital and Analog Signal Levels:**
  - **Digital 3V to 20V**
  - **Analog to 20Vp-p**
- **Low ON Resistance: 125Ω (typ) Over 15Vp-p Signal Input Range for VDD - VEE = 15V**
- **High OFF Resistance: Channel Leakage of ±100pA (typ) at VDD - VEE = 18V**
- **Logic Level Conversion:**
  - **Digital Addressing Signals of 3V to 20V (VDD - VSS = 3V to 20V)**
  - **Switch Analog Signals to 20Vp-p (VDD - VEE = 20V); See Introductory Text**
- **Matched Switch Characteristics: RON = 5Ω (typ) for VDD - VEE = 15V**
- **Very Low Quiescent Power Dissipation Under All Digital Control Input and Supply Conditions: 0.2μW (typ) at VDD - VSS = VDD - VEE = 10V**
- **Binary Address Decoding on Chip**
- **5V, 10V and 15V Parametric Ratings**
- **100% Tested for Quiescent Current at 20V**
- **Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C**
- **Break-Before-Making Switching Eliminates Channel Overlap**

Applications

- **Analog and Digital Multiplexing and Demultiplexing**
- **A/D and D/A Conversion**
- **Signal Gating**

* When these devices are used as demultiplexers the “CHANNEL IN/OUT” terminals are the outputs and the “COMMON OUT/IN” terminals are the inputs.

Description

CD4051BMS, CD4052BMS and CD4053BMS analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20V peak-to-peak can be achieved by digital signal amplitudes of 4.5V to 20V (if VDD-VSS = 3V, a VDD-VEE of up to 13V can be controlled; for VDD-VEE level differences above 13V, a VDD-VSS of at least 4.5V is required). For example, if VDD = +4.5V, VSS = 0, and VEE = -13.5V, analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0 to 5V. These multiplexer circuits dissipate extremely low quiescent power over the full VDD-VSS and VDD-VEE supply voltage ranges, independent of the logic state of the control signals. When a logic “1” is present at the inhibit input terminal all channels are off.

The CD4051BMS is a single 8 channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052BMS is a differential 4 channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053BMS is a triple 2 channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single pole double-throw configuration.

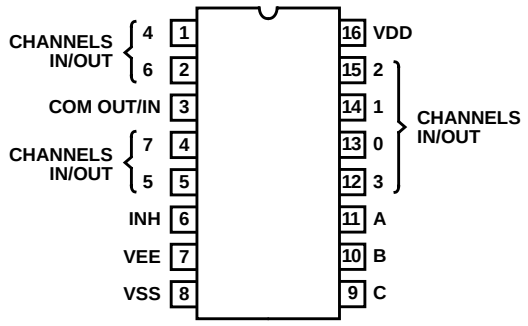
The CD4051BMS, CD4052BMS and CD4053BMS are supplied in these 16 lead outline packages:

Braze Seal DIP	*H4X	†H4T
Frit Seal DIP	H1E	
Ceramic Flatpack	H6W	

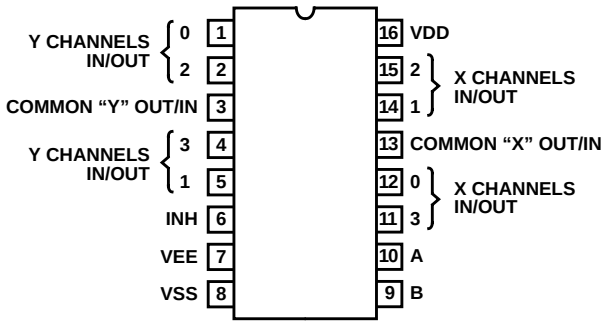
*CD4051B Only †CD4052B, CD4053 Only

Pinouts

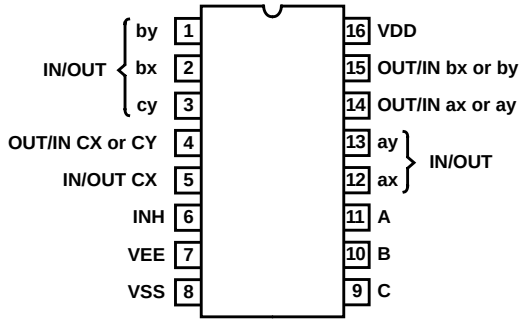
CD4051BM
TOP VIEW



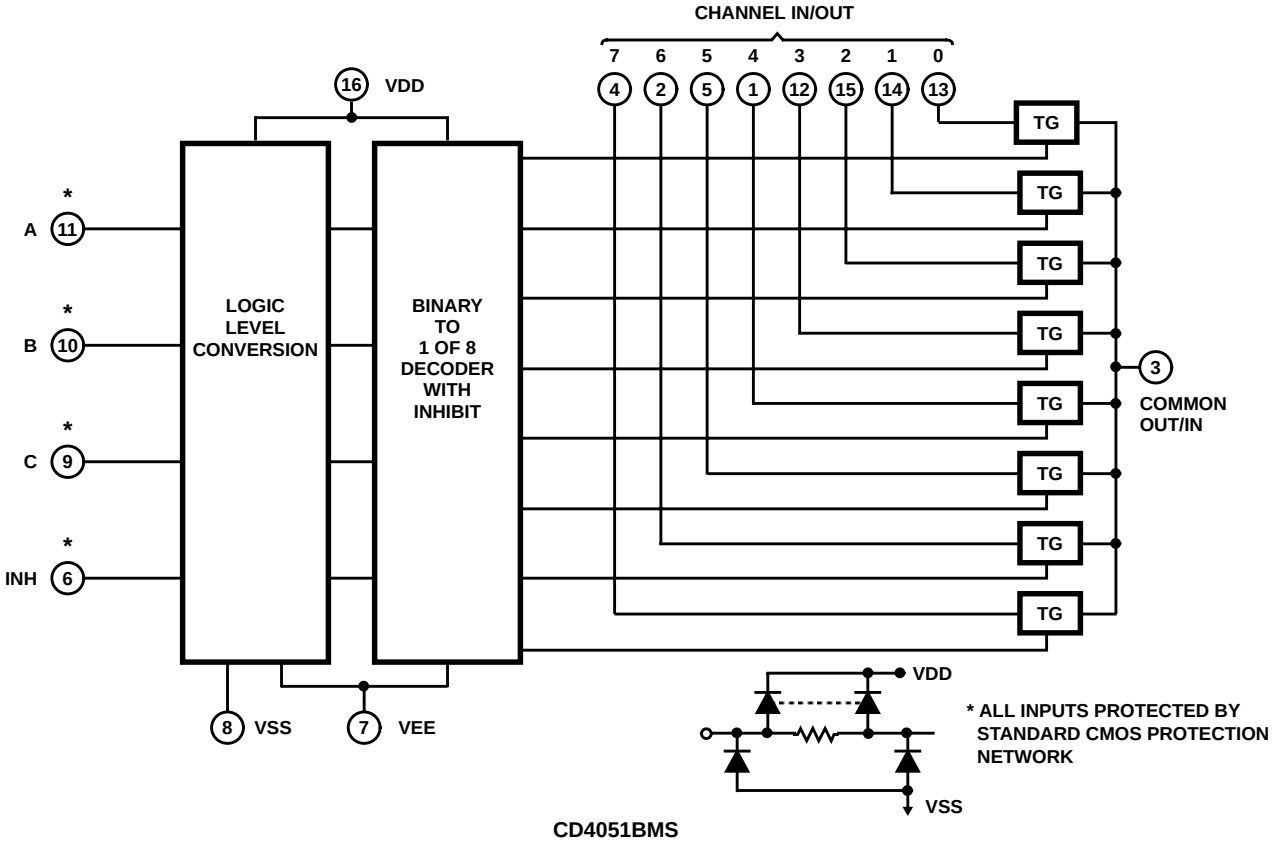
CD4052BMS
TOP VIEW



CD4053BMS
TOP VIEW

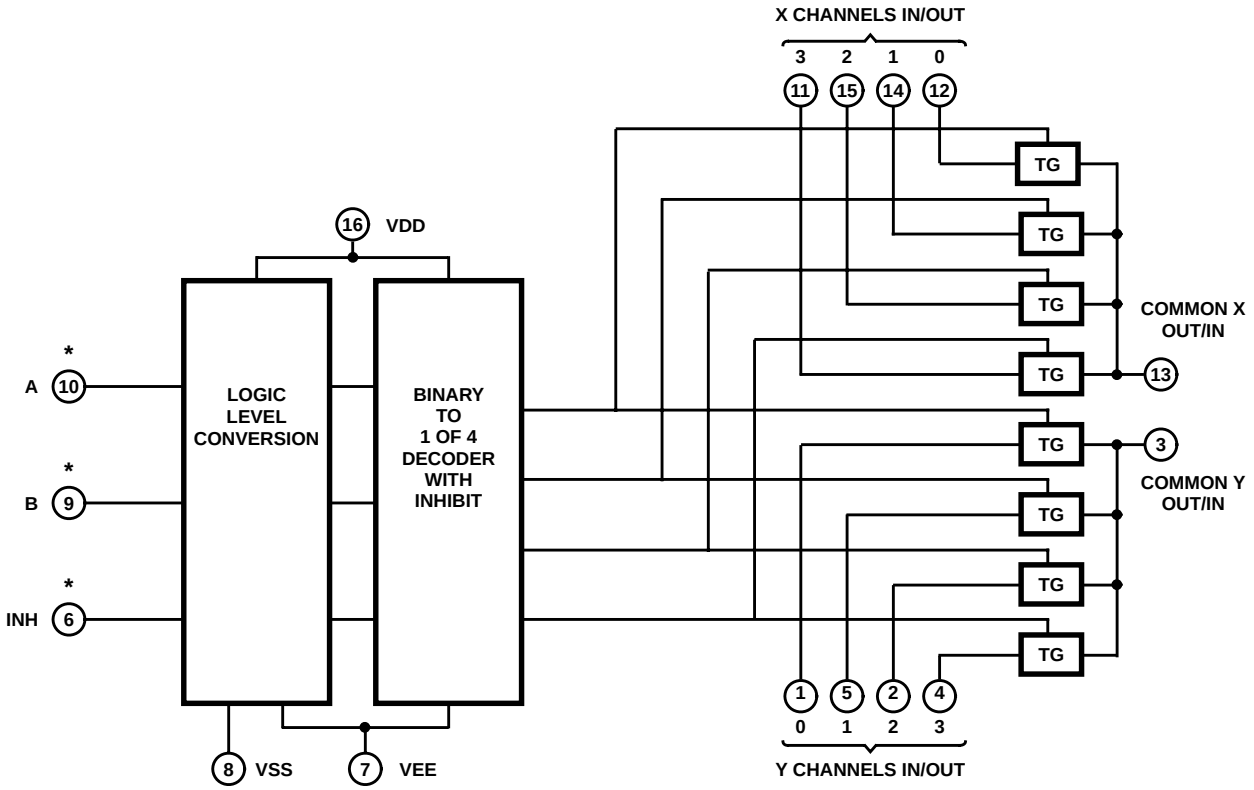


Functional Diagrams

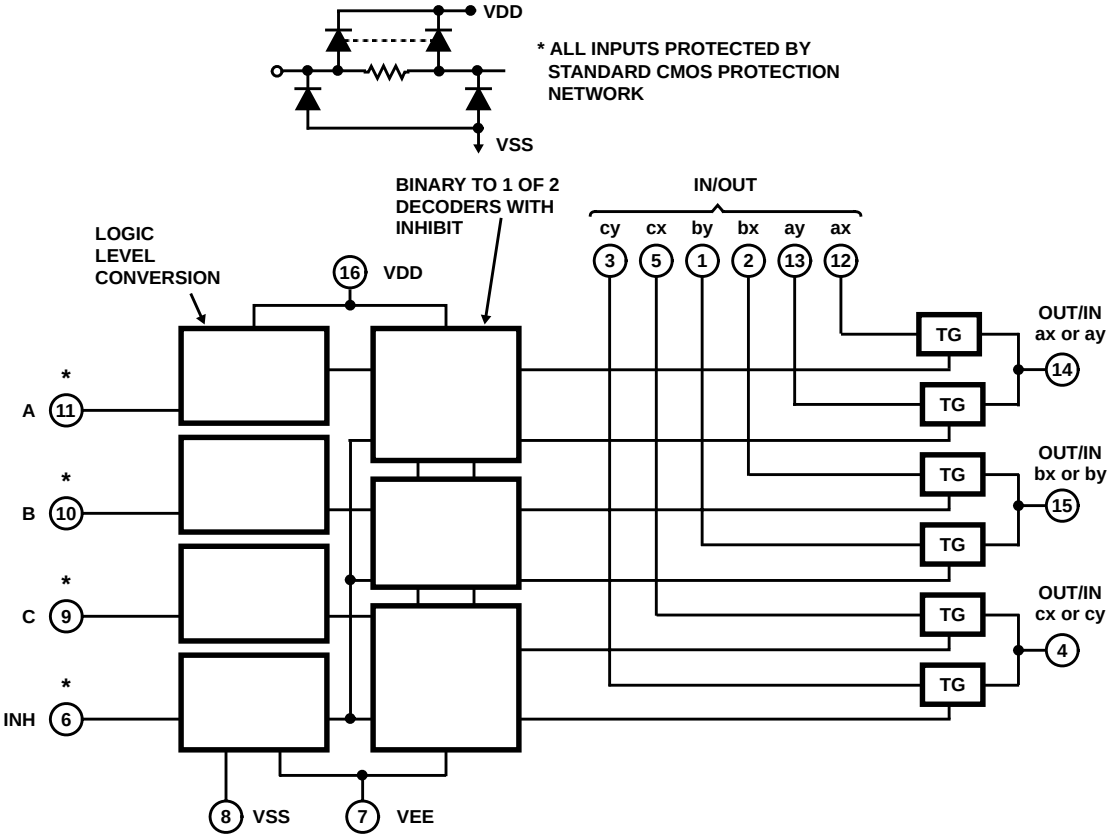


CD4051BMS

Functional Diagrams (Continued)



CD4052BMS



CD4053BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Operating Temperature Range . . . . . -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) . . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
On-State Resistance RL = 10K Returned to VDD - VSS/2	RON	VDD = 5V VIS = VSS to VDD		1	+25°C	-	1050	Ω
				2	+125°C	-	1300	Ω
				3	-55°C	-	800	Ω
		VDD = 10V VIS = VSS to VDD		1	+25°C	-	400	Ω
				2	+125°C	-	550	Ω
				3	-55°C	-	310	Ω
		VDD = 15V VIS = VSS to VDD		1	+25°C	-	240	Ω
				2	+125°C	-	320	Ω
				3	-55°C	-	220	Ω
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional (Note 4)	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V = VIS thru 1k, VEE = VSS RL = 1k to VSS, |IIS| < 2µA OFF Channels		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH			1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V = VIS thru 1K VEE = VSS RL = 1K to VSS, |ISS|, <2µA On All OFF Channels		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH			1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Off Channel Leakage Any Channel OFF Or All Channels Off (Common Out/In)	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.1	-	µA
				2	+125°C	-1.0	-	µA
			VDD = 18V	3	-55°C	-0.1	-	µA
	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.1	µA
				2	+125°C	-	1.0	µA
			VDD = 18V	3	-55°C	-	0.1	µA

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.
4. VDD = 2.8V/3.0V, RL = 200k to VDD
VDD = 20V/18V, RL = 10k to VDD

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (Notes 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay (Note 1) Address to Signal Out Channels On or Off	TPHL TPLH	VDD = 5V, VIN = VDD or GND VEE = VSS = 0V	9	+25°C	-	720	ns
			10, 11	+125°C, -55°C	-	972	ns
Propagation Delay (Note 1) Inhibit to Signal Out (Channel Turning On)	TPZH TPZL	VDD = 5V, VIN = VDD or GND VEE = VSS = 0V	9	+25°C	-	720	ns
			10, 11	+125°C, -55°C	-	972	ns
Propagation Delay (Note 1) Inhibit to Signal Out (Channel Turning Off)	TPHZ TPLZ	VDD = 5V, VIN = VDD or GND VEE = VSS = 0V	9	+25°C	-	450	ns
			10, 11	+125°C, -55°C	-	608	ns

NOTES:

1. -55°C and +125°C limits guaranteed, 100% testing being implemented.
2. CL = 50pF, RL = 10KΩ, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS		NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND		1, 2	-55°C, +25°C	-	5	µA
					+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND		1, 2	-55°C, +25°C	-	10	µA
					+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND		1, 2	-55°C, +25°C	-	10	µA
					+125°C	-	600	µA
Input Voltage Low	VIL	VDD = VIS = 10V, VEE = VSS RL = 1K to VSS |IIS|, 2µA On/Off Channel		1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH			1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Address to Signal Out (Channels On or Off)	TPHL TPLH	VDD = 10V	VEE = VSS = 0V	1, 2, 3	+25°C	-	320	ns
		VDD = 15V		1, 2, 3	+25°C	-	240	ns
		VDD = 5V VEE = -5V		1, 2, 3	+25°C	-	450	ns
Propagation Delay Inhibit to Signal Out (Channel Turning On)	TPZH TPZL	VDD = 10V	VEE = VSS = 0V	1, 2, 3	+25°C	-	320	ns
		VDD = 15V		1, 2, 3	+25°C	-	240	ns
		VDD = 5V VEE = -10V		1, 2, 3	+25°C	-	400	ns
Propagation Delay Inhibit to Signal Out (Channel Turning Off)	TPHZ TPLZ	VDD = 10V	VEE = VSS = 0V	1, 2, 3	+25°C	-	210	ns
		VDD = 15V		1, 2, 3	+25°C	-	160	ns
		VDD = 5V VEE = -15V		1, 2, 3	+25°C	-	300	ns
Input Capacitance	CIN	Any Address or Inhibit Input		1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 10K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
ON Resistance	RONDEL10	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER CD4051BMS						

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	3	1, 2, 4 - 6, 7, 8, 9 - 15	16			
Static Burn-In 2 Note 1	3	7, 8	1, 2, 4 - 6, 9 - 16			
Dynamic Burn-In Note 1	-	4 - 6, 7, 8, 9, 12, 14	1, 2, 13, 15, 16	3	11	10
Irradiation Note 2	3	7, 8	1, 2, 4 - 6, 9 - 16			
PART NUMBER CD4052BMS						
Static Burn-In 1 Note 1	3, 13	1, 2, 4 - 6, 7, 8, 9 - 12, 14, 15	16			
Static Burn-In 2 Note 1	3, 13	7, 8	1, 2, 4 - 6, 9 - 12, 14 - 16			
Dynamic Burn-In Note 1	-	4 - 6, 7, 8, 12, 15	1, 2, 11, 14, 16	3, 13	10	9
Irradiation Note 2	3, 13	7, 8	1, 2, 4 - 6, 9 - 12, 14 - 16			
PART NUMBER CD4053BMS						
Static Burn-In 1 Note 1	4, 14, 15	1 - 3, 5 - 8, 9 - 13	16			
Static Burn-In 2 Note 1	4, 14, 15	7, 8	1 - 3, 5, 6, 9 - 13, 16			
Dynamic Burn-In Note 1	-	1, 5 - 8, 12	2, 3, 13, 16	4, 14, 15	9 - 11	
Irradiation Note 2	4, 14, 15	7, 8	1 - 3, 5, 6, 9 - 13, 16			

NOTE:

1. Each pin except pin 7 VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except pin 7 VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Typical Performance Characteristics

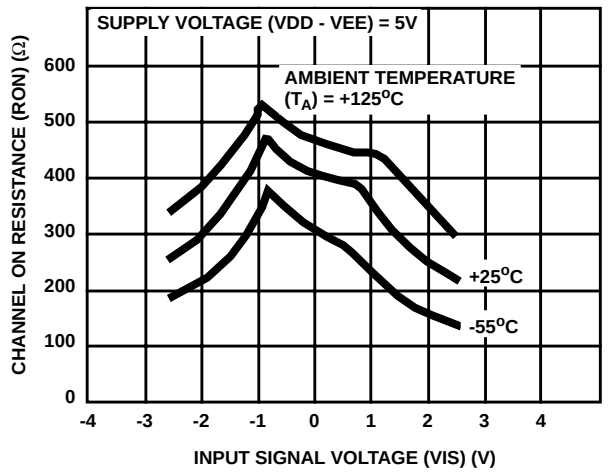


FIGURE 1. TYPICAL CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

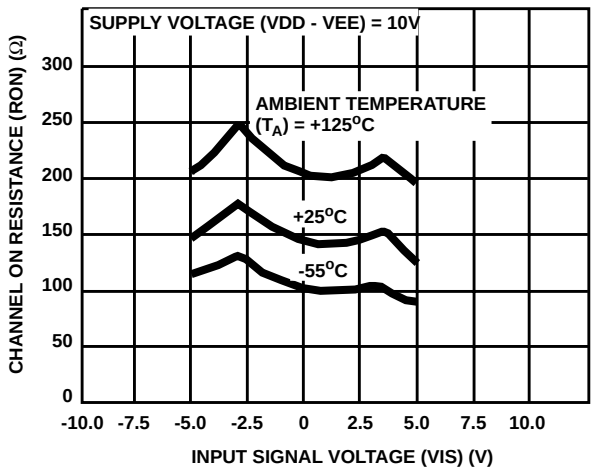


FIGURE 2. TYPICAL CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

Typical Performance Characteristics (Continued)

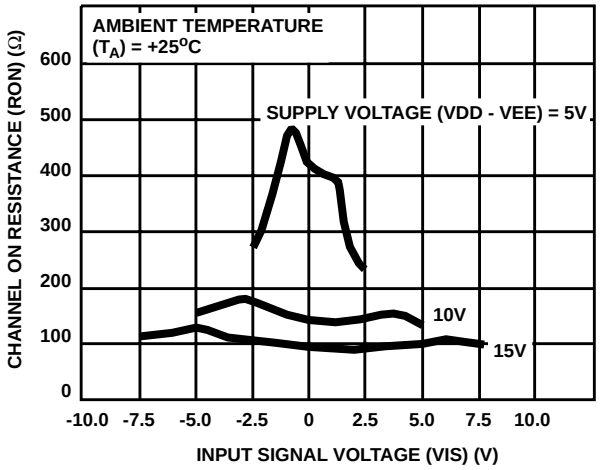


FIGURE 3. TYPICAL CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLATGE (ALL TYPES)

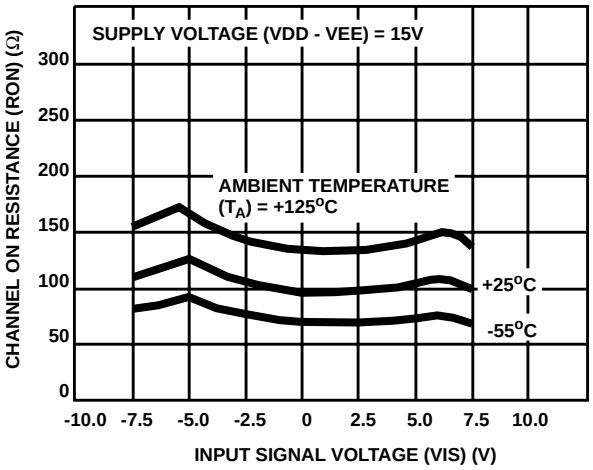


FIGURE 4. TYPICAL CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

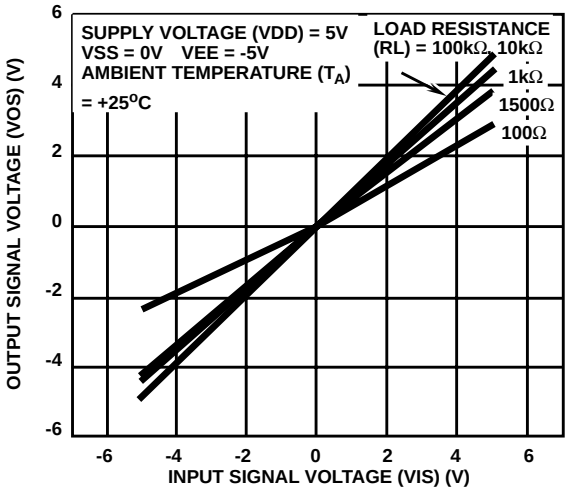


FIGURE 5. TYPICAL ON CHARACTERISTICS FOR 1 OF 8 CHANNELS (CD4051BMS)

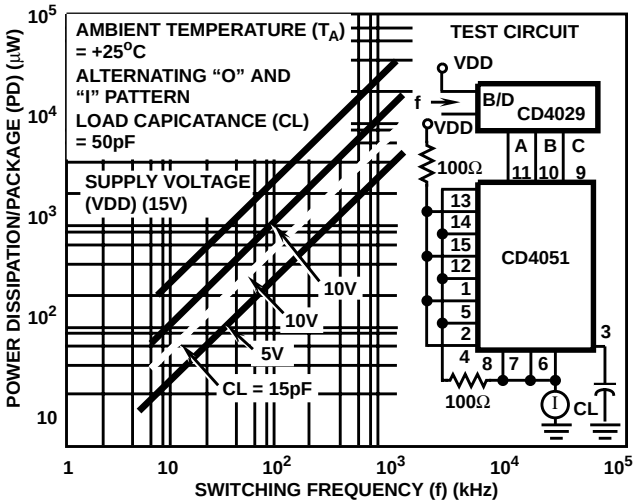


FIGURE 6. TYPICAL DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4051BMS)

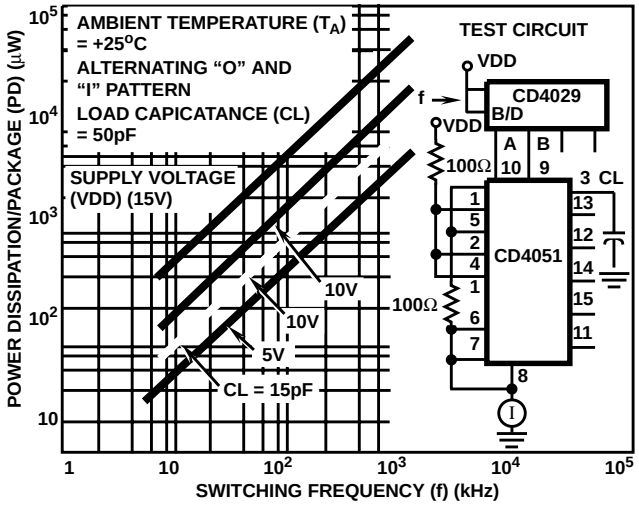


FIGURE 7. TYPICAL DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4052BMS)

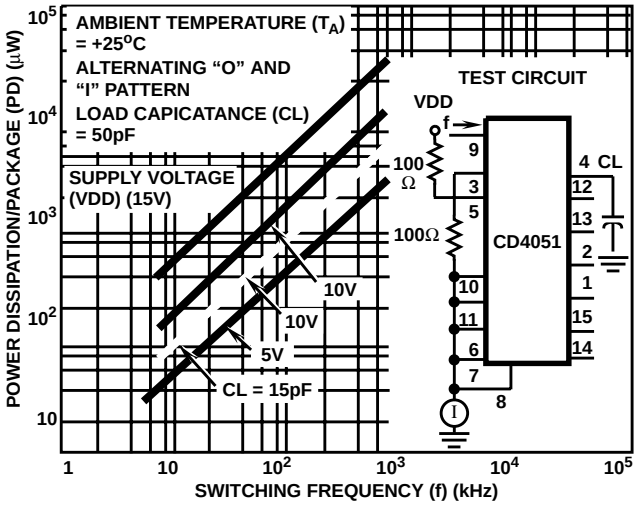
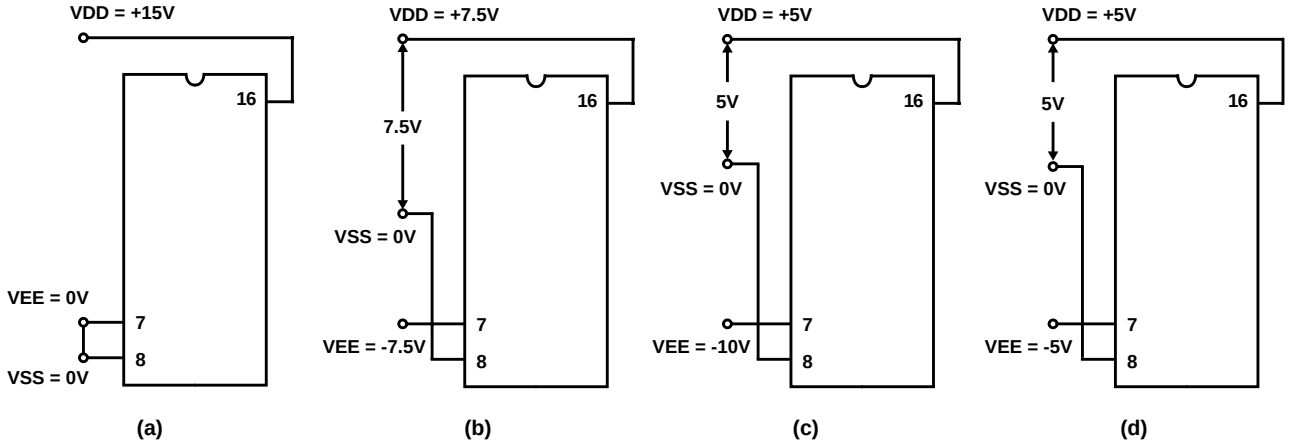


FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4053BMS)



The ADDRESS (digital-control inputs) and INHIBIT logic levels are: “0” = VSS and “1” = VDD. The analog signal (through the TG) may swing from VEE to VDD

FIGURE 9. TYPICAL BIAS VOLTAGES

TRUTH TABLE

INPUT STATES				"ON" CHANNEL(S)
CD4051BMS				
INHIBIT	**C**	**B**	**A**	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	NONE
CD4052BMS				
INHIBIT		**B**	**A**	
0		0	0	0x, 0y
0		0	1	1x, 1y
0		1	0	2x, 2y
0		1	1	3x, 3y
1		x	x	NONE
CD4053BMS				
INHIBIT		**A OR B OR C**		
0		0		ax or bx or cx
0		1		ay or by or cy
1		X		NONE

X = Don't Care

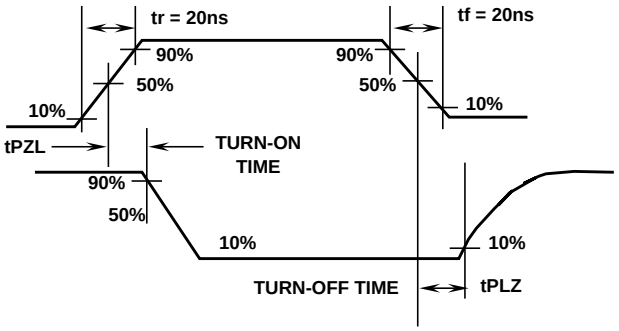


FIGURE 10. WAVEFORM, CHANNEL BEING TURNED ON, OFF (RL = 1kΩ)

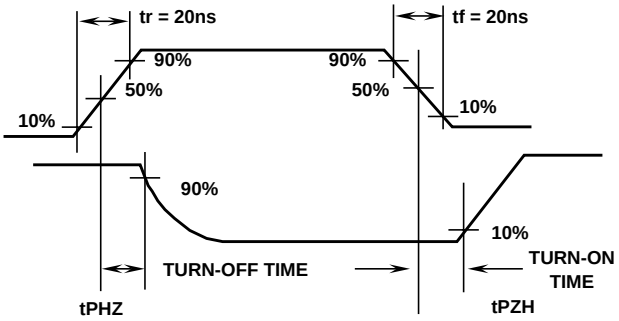
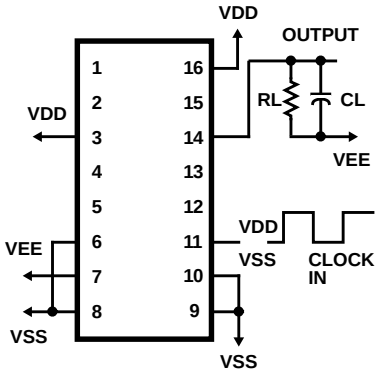
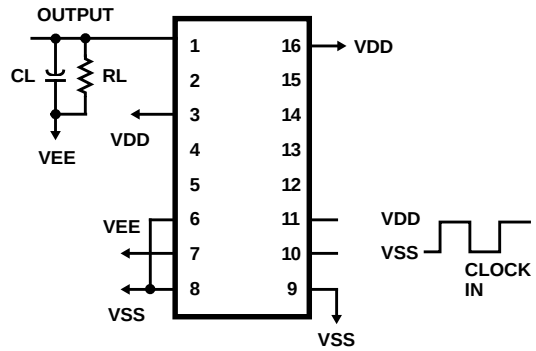


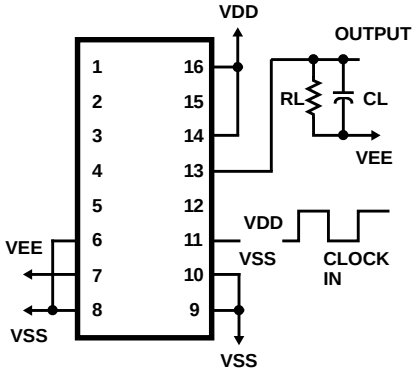
FIGURE 11. WAVEFORM, CHANNEL BEING TURNED OFF, ON (RL = 1kΩ)



CD4051



CD4052



CD4053

FIGURE 12. PROPAGATION DELAY - ADDRESS INPUT TO SIGNAL OUTPUT

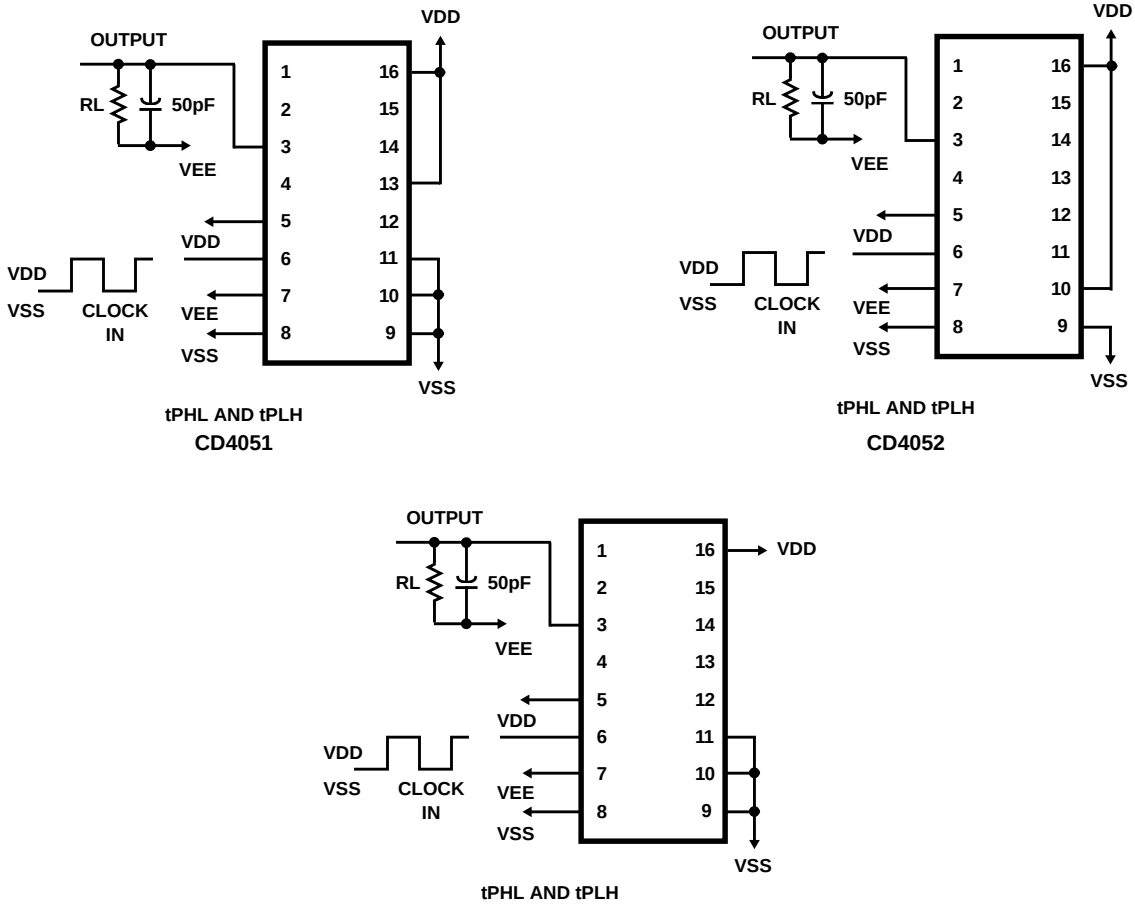


FIGURE 13. PROPAGATION DELAY - INHIBIT INPUT TO SIGNAL OUTPUT

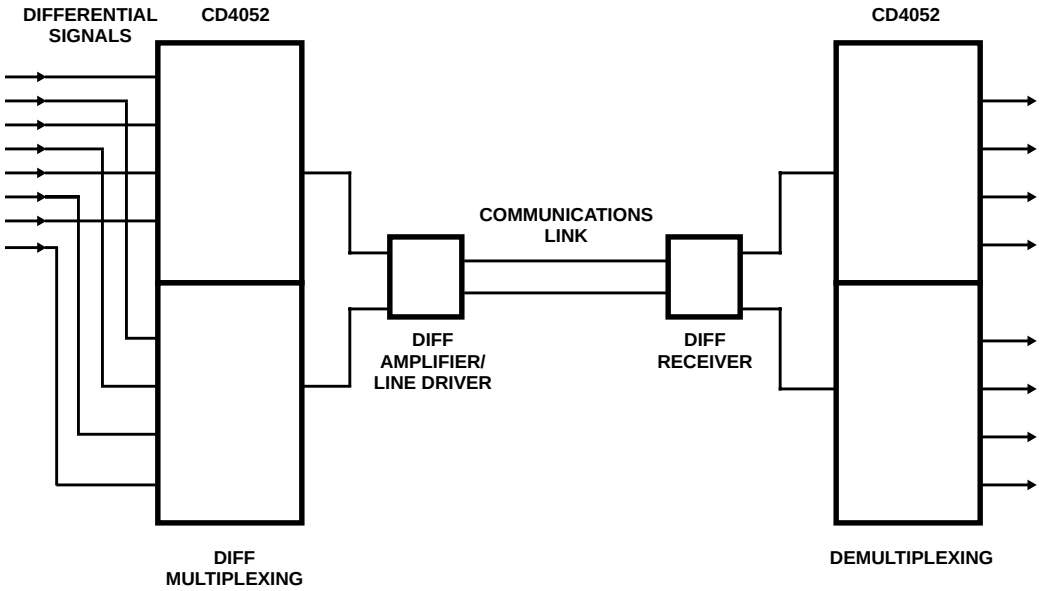
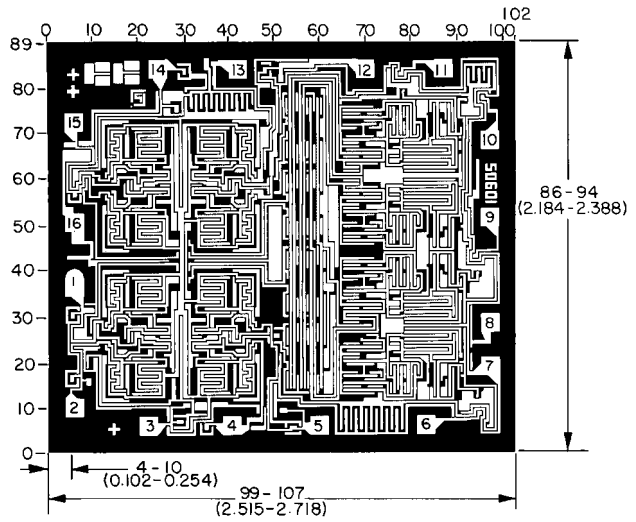
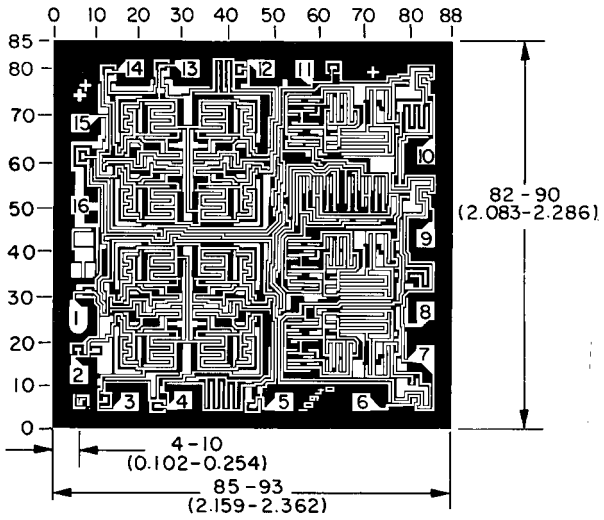


FIGURE 14. TYPICAL TIME-DIVISION APPLICATION OF THE CD4052BMS

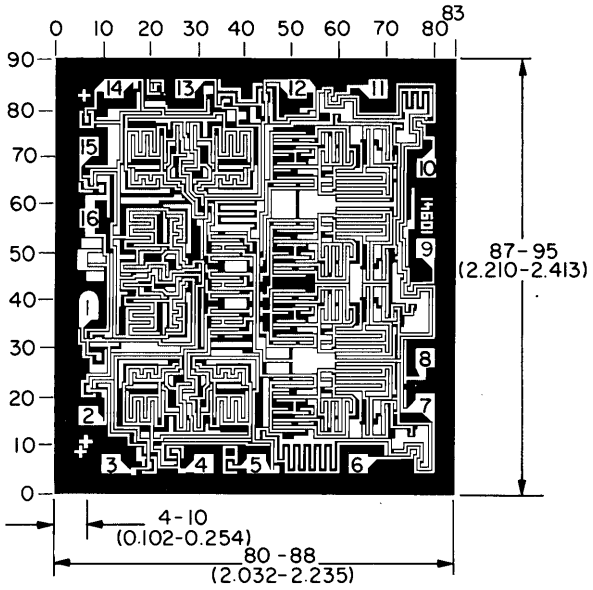
Chip Dimensions and Pad Layouts



CD4051BMSH



CD4052BMSH



CD4053BMSH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.