

## 3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES037C – JULY 1995 – REVISED FEBRUARY 1999

- **Member of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

### description

This 20-bit bus-interface flip-flop is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVCH16821 can be used as two 10-bit flip-flops or one 20-bit flip-flop. The 20 flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16821 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### DGG OR DL PACKAGE (TOP VIEW)

$\overline{1OE}$	1	56	1CLK
1Q1	2	55	1D1
1Q2	3	54	1D2
GND	4	53	GND
1Q3	5	52	1D3
1Q4	6	51	1D4
$V_{CC}$	7	50	$V_{CC}$
1Q5	8	49	1D5
1Q6	9	48	1D6
1Q7	10	47	1D7
GND	11	46	GND
1Q8	12	45	1D8
1Q9	13	44	1D9
1Q10	14	43	1D10
2Q1	15	42	2D1
2Q2	16	41	2D2
2Q3	17	40	2D3
GND	18	39	GND
2Q4	19	38	2D4
2Q5	20	37	2D5
2Q6	21	36	2D6
$V_{CC}$	22	35	$V_{CC}$
2Q7	23	34	2D7
2Q8	24	33	2D8
GND	25	32	GND
2Q9	26	31	2D9
2Q10	27	30	2D10
$\overline{2OE}$	28	29	2CLK

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# SN74ALVCH16821

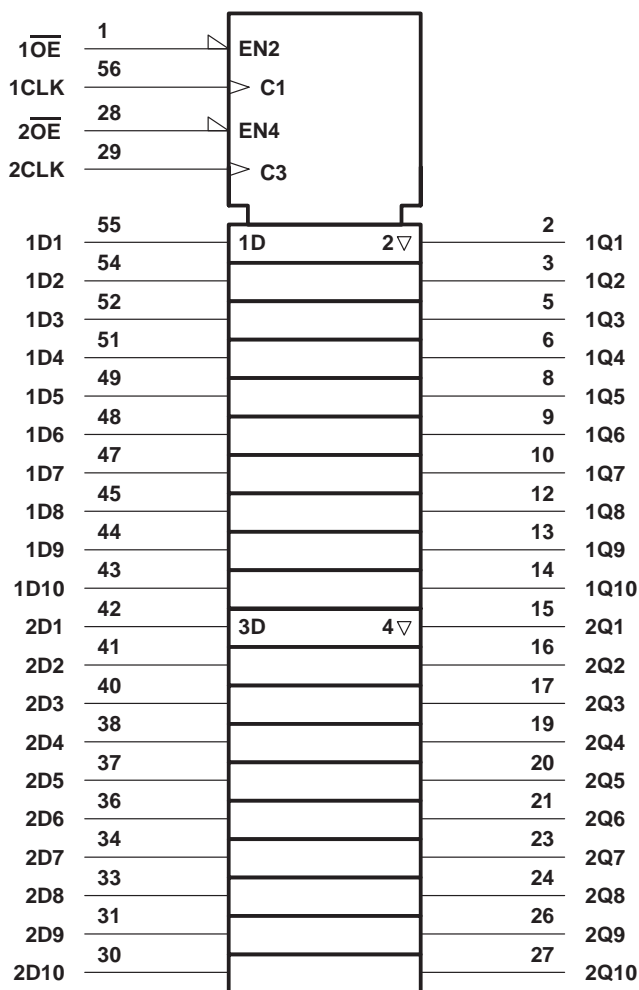
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SCES037C – JULY 1995 – REVISED FEBRUARY 1999

FUNCTION TABLE  
(each 10-bit flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z

### logic symbol†

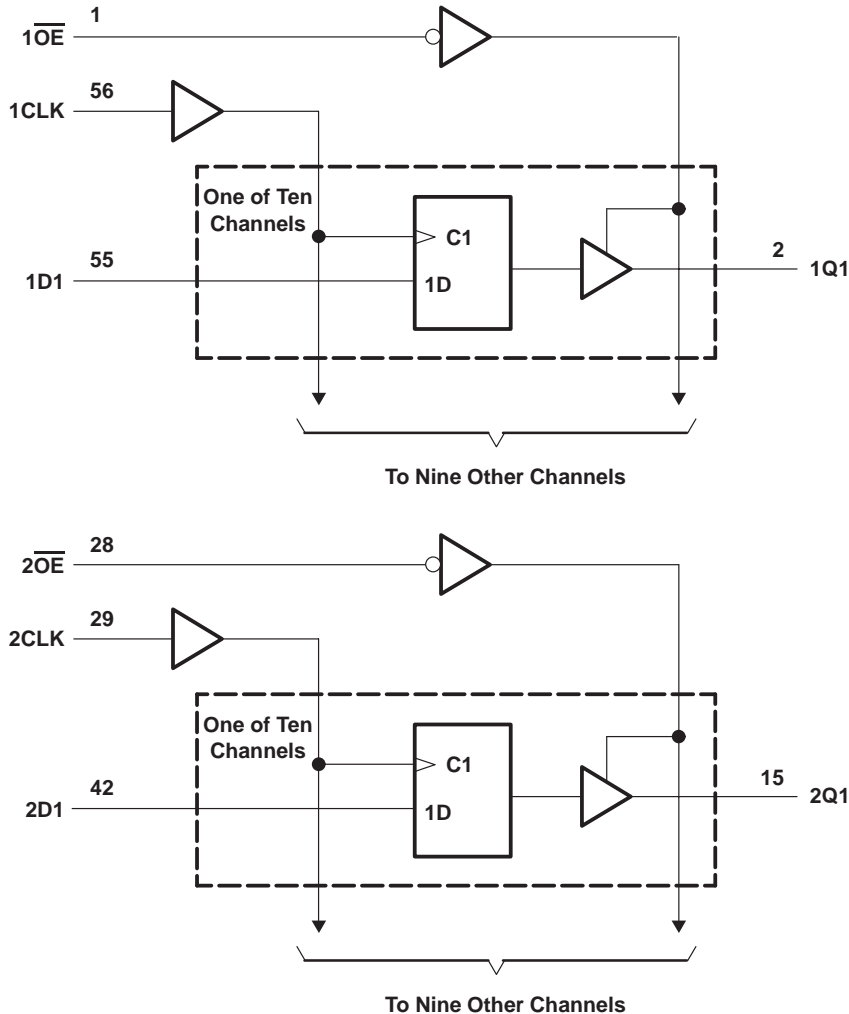


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**SN74ALVCH16821**  
**3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**

SCES037C – JULY 1995 – REVISED FEBRUARY 1999

**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 4.6 V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ .....	$\pm 50$ mA
Continuous current through each $V_{CC}$ or GND .....	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package .....	81°C/W
DL package .....	74°C/W
Storage temperature range, $T_{Stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. This value is limited to 4.6 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51.

**SN74ALVCH16821**  
**3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**

SCES037C – JULY 1995 – REVISED FEBRUARY 1999

**recommended operating conditions (see Note 4)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.65	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	-4	mA
		V <sub>CC</sub> = 2.3 V	-12	
		V <sub>CC</sub> = 2.7 V	-12	
		V <sub>CC</sub> = 3 V	-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V	4	mA
		V <sub>CC</sub> = 2.3 V	12	
		V <sub>CC</sub> = 2.7 V	12	
		V <sub>CC</sub> = 3 V	24	
Δt/Δv	Input transition rise or fall rate		10	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN74ALVCH16821**  
**3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**

SCES037C – JULY 1995 – REVISED FEBRUARY 1999

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 µA	1.65 V to 3.6 V	V <sub>CC</sub> -0.2			V
	I <sub>OH</sub> = -4 mA	1.65 V	1.2			
	I <sub>OH</sub> = -6 mA	2.3 V	2			
	I <sub>OH</sub> = -12 mA	2.3 V	1.7			
		2.7 V	2.2			
		3 V	2.4			
I <sub>OH</sub> = -24 mA	3 V	2				
V <sub>OL</sub>	I <sub>OL</sub> = 100 µA	1.65 V to 3.6 V			0.2	V
	I <sub>OL</sub> = 4 mA	1.65 V			0.45	
	I <sub>OL</sub> = 6 mA	2.3 V			0.4	
	I <sub>OL</sub> = 12 mA	2.3 V			0.7	
		2.7 V			0.4	
	I <sub>OL</sub> = 24 mA	3 V			0.55	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±5	µA
I <sub>I</sub> (hold)	V <sub>I</sub> = 0.58 V	1.65 V		25		µA
	V <sub>I</sub> = 1.07 V	1.65 V		-25		
	V <sub>I</sub> = 0.7 V	2.3 V		45		
	V <sub>I</sub> = 1.7 V	2.3 V		-45		
	V <sub>I</sub> = 0.8 V	3 V		75		
	V <sub>I</sub> = 2 V	3 V		-75		
	V <sub>I</sub> = 0 to 3.6 V‡	3.6 V			±500	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			±10	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			40	µA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	µA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	3.5		pF
	Data inputs			6		
C <sub>o</sub>	Outputs	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	7		pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)**

		V <sub>CC</sub> = 1.8 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	§		150		150		150		MHz
t <sub>w</sub>	Pulse duration, CLK high or low	§		3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before CLK↑	§		4.4		3.9		3.4		ns
t <sub>h</sub>	Hold time, data after CLK↑	§		0		0		0		ns

§ This information was not available at the time of publication.

**SN74ALVCH16821**  
**3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**

SCES037C – JULY 1995 – REVISED FEBRUARY 1999

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			†		150		150		150		MHz
t <sub>pd</sub>	CLK	Q		†	1	5.8		5.3	1	4.5	ns
t <sub>en</sub>	$\overline{OE}$	Q		†	1	6.6		6.2	1	5.1	ns
t <sub>dis</sub>	$\overline{OE}$	Q		†	1	5.7		5	1	4.6	ns

† This information was not available at the time of publication.

**operating characteristics, T<sub>A</sub> = 25°C**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
			TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled	†	36	40	pF
		Outputs disabled	†	22	24	

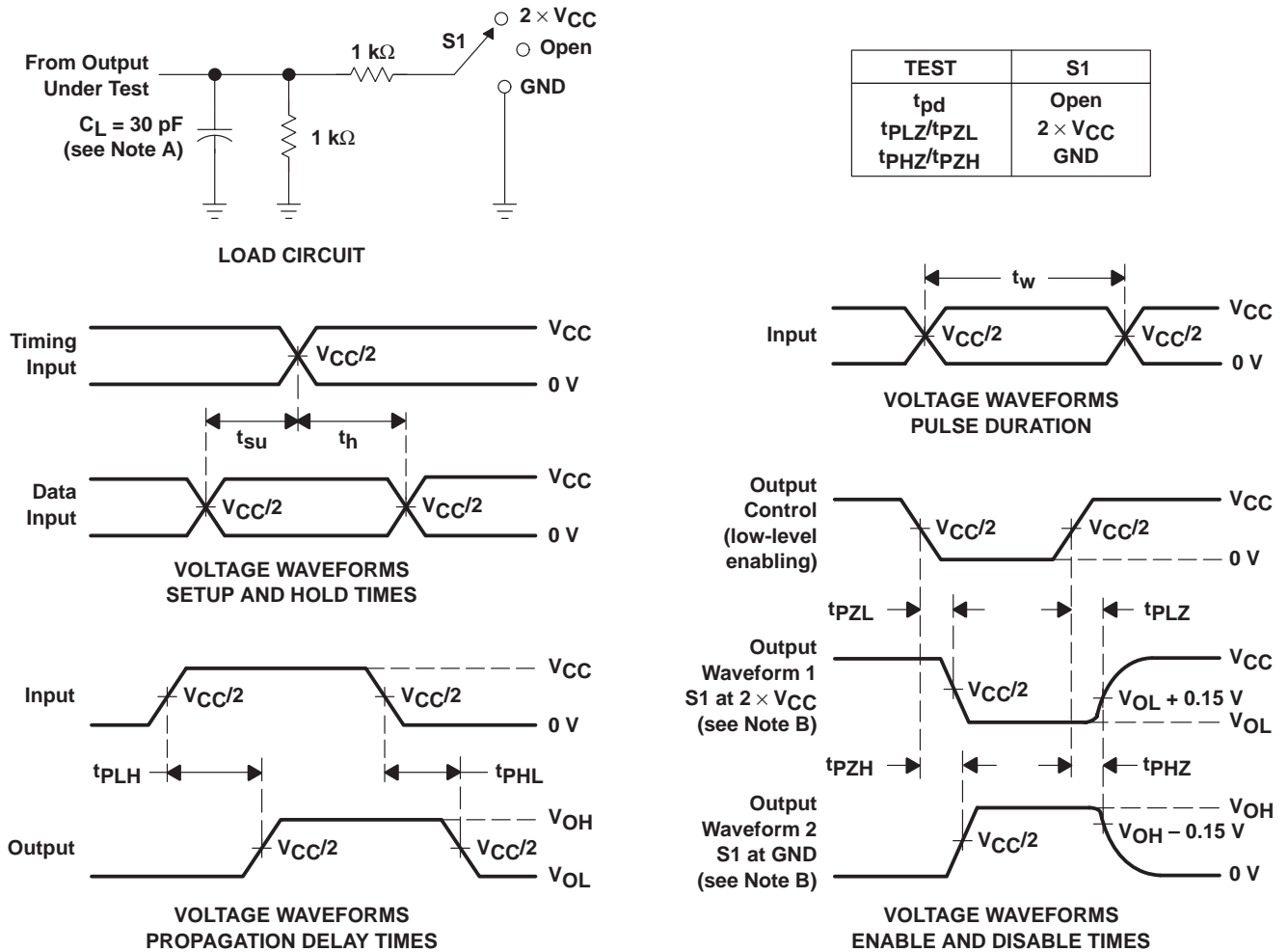
† This information was not available at the time of publication.

**SN74ALVCH16821**  
**3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**

SCES037C – JULY 1995 – REVISED FEBRUARY 1999

**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 1.8\text{ V}$



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

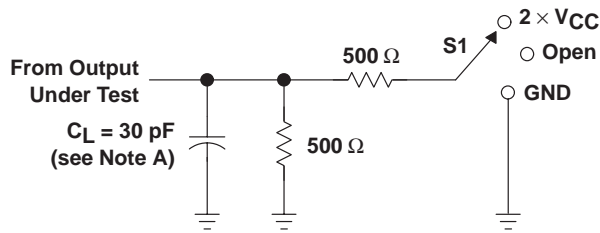
**Figure 1. Load Circuit and Voltage Waveforms**

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SCES037C – JULY 1995 – REVISED FEBRUARY 1999

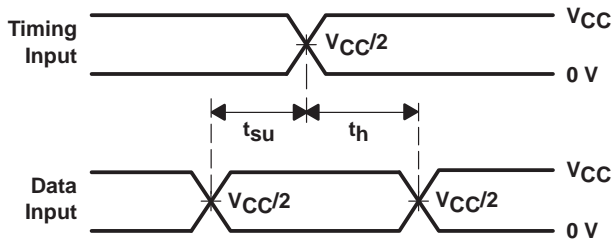
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

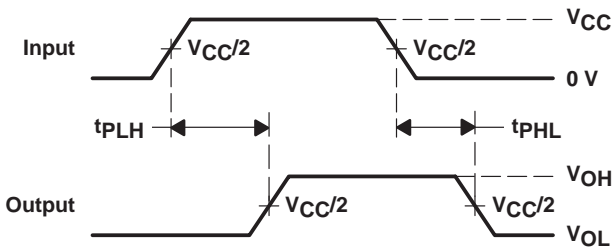


**LOAD CIRCUIT**

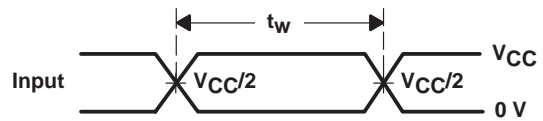
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



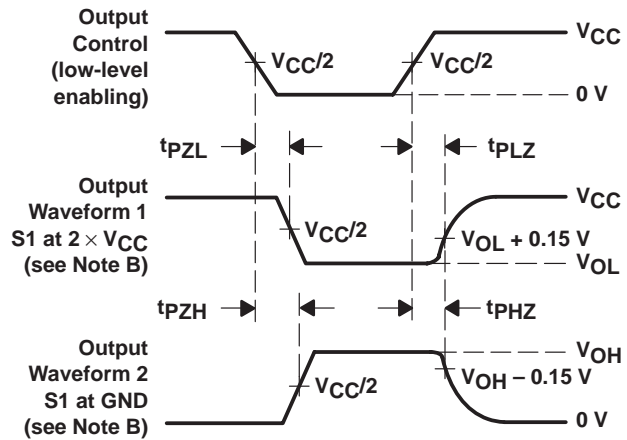
**VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
 PULSE DURATION**



**VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES**

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 2. Load Circuit and Voltage Waveforms**

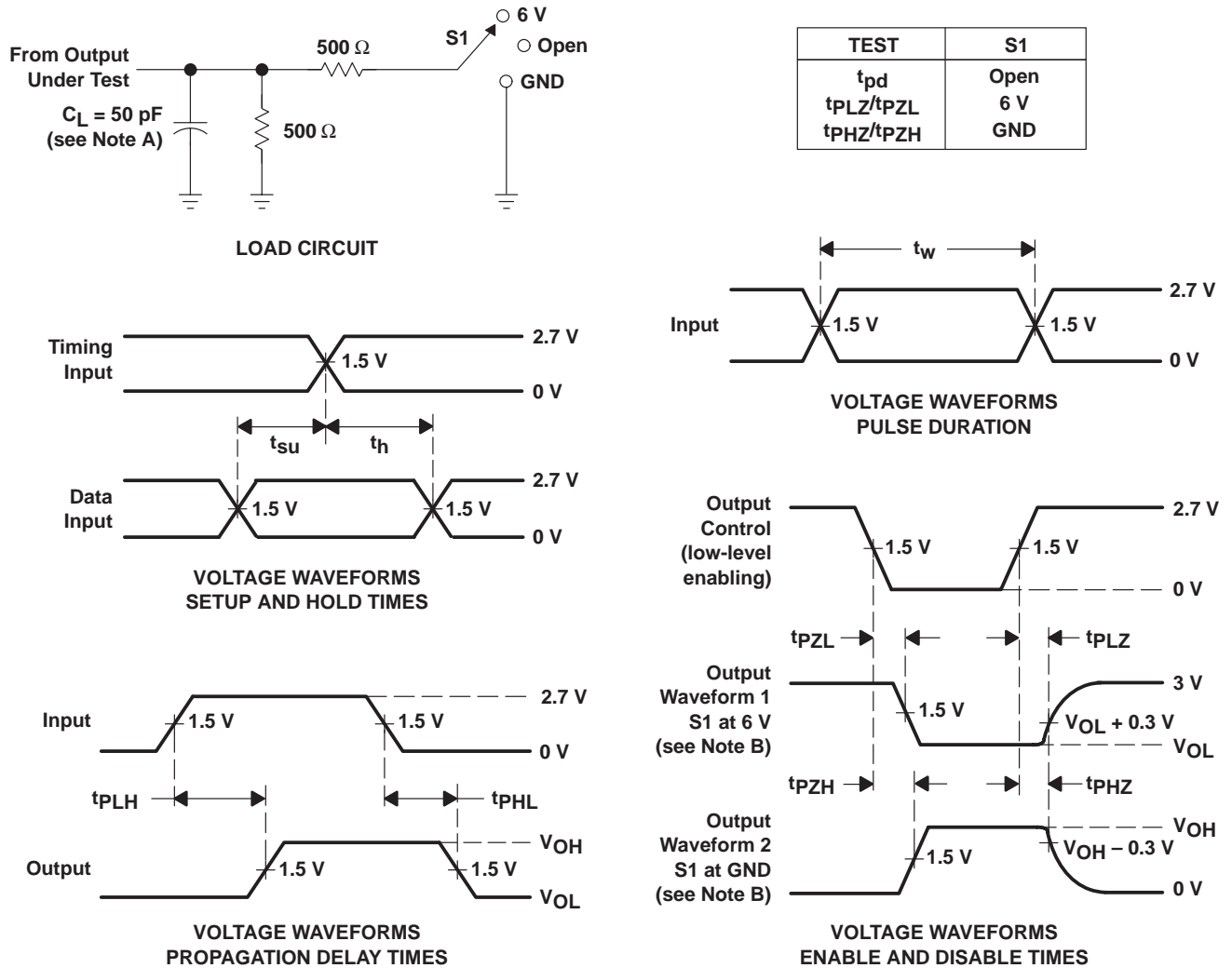


**SN74ALVCH16821**  
**3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**

SCES037C – JULY 1995 – REVISED FEBRUARY 1999

**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 3. Load Circuit and Voltage Waveforms**

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