

# SN74CBTS16211 24-BIT FET BUS SWITCH WITH SCHOTTKY DIODE CLAMPING

SCDS050B – MARCH 1998 – REVISED MAY 1998

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages**

## description

The SN74CBTS16211 provides 24 bits of high-speed TTL-compatible bus switching with Schottky diodes on the I/Os to clamp undershoot. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device can operate as a dual 12-bit bus switch or a single 24-bit bus switch. When  $\overline{1OE}$  is low, 1A is connected to 1B. When  $\overline{2OE}$  is low, 2A is connected to 2B.

The SN74CBTS16211 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**FUNCTION TABLE**  
(each 12-bit bus switch)

| INPUT<br>$\overline{OE}$ | FUNCTION        |
|--------------------------|-----------------|
| L                        | A port = B port |
| H                        | Disconnect      |

**DGG, DGV, OR DL PACKAGE  
(TOP VIEW)**

|                 |    |    |                  |
|-----------------|----|----|------------------|
| NC              | 1  | 56 | $\overline{1OE}$ |
| 1A1             | 2  | 55 | $\overline{2OE}$ |
| 1A2             | 3  | 54 | 1B1              |
| 1A3             | 4  | 53 | 1B2              |
| 1A4             | 5  | 52 | 1B3              |
| 1A5             | 6  | 51 | 1B4              |
| 1A6             | 7  | 50 | 1B5              |
| GND             | 8  | 49 | GND              |
| 1A7             | 9  | 48 | 1B6              |
| 1A8             | 10 | 47 | 1B7              |
| 1A9             | 11 | 46 | 1B8              |
| 1A10            | 12 | 45 | 1B9              |
| 1A11            | 13 | 44 | 1B10             |
| 1A12            | 14 | 43 | 1B11             |
| 2A1             | 15 | 42 | 1B12             |
| 2A2             | 16 | 41 | 2B1              |
| V <sub>CC</sub> | 17 | 40 | 2B2              |
| 2A3             | 18 | 39 | 2B3              |
| GND             | 19 | 38 | GND              |
| 2A4             | 20 | 37 | 2B4              |
| 2A5             | 21 | 36 | 2B5              |
| 2A6             | 22 | 35 | 2B6              |
| 2A7             | 23 | 34 | 2B7              |
| 2A8             | 24 | 33 | 2B8              |
| 2A9             | 25 | 32 | 2B9              |
| 2A10            | 26 | 31 | 2B10             |
| 2A11            | 27 | 30 | 2B11             |
| 2A12            | 28 | 29 | 2B12             |

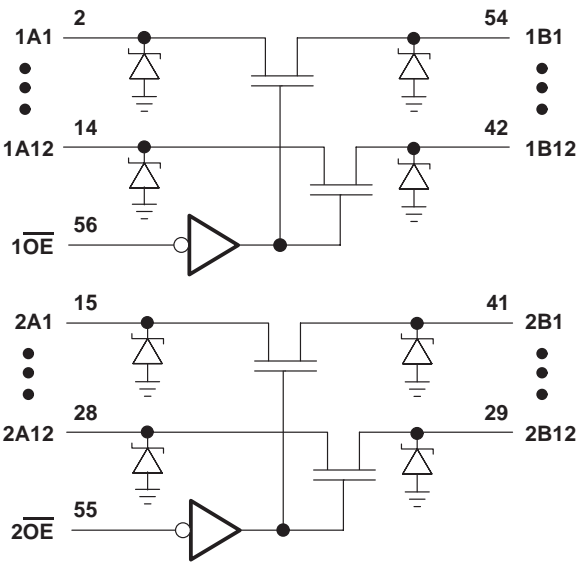
NC – No internal connection

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|  |                |
|--|----------------|
| Supply voltage range, $V_{CC}$                         | –0.5 V to 7 V  |
| Input voltage range, $V_I$ (see Note 1)                | –0.5 V to 7 V  |
| Continuous channel current                             | 128 mA         |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )            | –50 mA         |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): |                |
| DGG package  | 81°C/W         |
| DGV package  | 86°C/W         |
| DL package   | 74°C/W         |
| Storage temperature range, $T_{stg}$                   | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

|   | MIN | MAX | UNIT |
|---|-----|-----|------|
| $V_{CC}$ Supply voltage                   | 4   | 5.5 | V    |
| $V_{IH}$ High-level control input voltage | 2   |     | V    |
| $V_{IL}$ Low-level control input voltage  |     | 0.8 | V    |
| $T_A$ Operating free-air temperature      | –40 | 85  | °C   |

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                |   | TEST CONDITIONS           |   | MIN | TYP† | MAX  | UNIT          |
|--------------------------|---|---------------------------|---|-----|------|------|---------------|
| $V_{IK}$                 |   | $V_{CC} = 4.5\text{ V}$ , | $I_I = -18\text{ mA}$                               |     |      | -1.2 | V             |
| $I_I$                    | $I_{IL}$  | $V_{CC} = 5.5\text{ V}$ , | $V_I = \text{GND}$                                  |     |      | -1   | $\mu\text{A}$ |
|                          | $I_{IH}$  | $V_{CC} = 5.5\text{ V}$ , | $V_I = 5.5\text{ V}$                                |     |      | 150  |               |
| $I_{CC}$                 |   | $V_{CC} = 5.5\text{ V}$ , | $I_O = 0$ , $V_I = V_{CC}$ or GND                   |     |      | 3    | $\mu\text{A}$ |
| $\Delta I_{CC}^\ddagger$ | Control inputs  | $V_{CC} = 5.5\text{ V}$ , | One input at 3.4 V, Other inputs at $V_{CC}$ or GND |     |      | 2.5  | mA            |
| $C_i$                    | Control inputs  | $V_I = 3\text{ V}$ or 0   |   |     |      | 3    | pF            |
| $C_{io}(\text{OFF})$     |   | $V_O = 3\text{ V}$ or 0,  | $\overline{OE} = V_{CC}$                            |     |      | 5.5  | pF            |
| $r_{on}^\S$              | $V_{CC} = 4\text{ V}$ ,<br>TYP at $V_{CC} = 4\text{ V}$ |                           | $V_I = 2.4\text{ V}$ , $I_I = 15\text{ mA}$         |     |      | 14   | $\Omega$      |
|                          | $V_{CC} = 4.5\text{ V}$                                 |                           | $V_I = 0$ , $I_I = 64\text{ mA}$                    |     |      | 5    |               |
|                          |   |                           | $I_I = 30\text{ mA}$                                |     |      | 5    |               |
|                          |   |                           | $V_I = 2.4\text{ V}$ , $I_I = 15\text{ mA}$         |     |      | 8    |               |

† All typical values are at  $V_{CC} = 5\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER   | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 4\text{ V}$ |      | $V_{CC} = 5\text{ V}$<br>$\pm 0.5\text{ V}$ |      | UNIT |
|-------------|-----------------|----------------|-----------------------|------|---|------|------|
|             |                 |                | MIN                   | MAX  | MIN   | MAX  |      |
| $t_{pd}^\P$ | A or B          | B or A         |                       | 0.35 |   | 0.25 | ns   |
| $t_{en}$    | $\overline{OE}$ | A or B         |                       | 9.3  | 3.3   | 8.6  | ns   |
| $t_{dis}$   | $\overline{OE}$ | A or B         |                       | 7.1  | 2.8   | 7.9  | ns   |

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

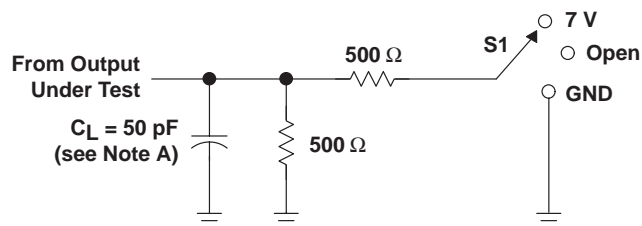
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## 24-BIT FET BUS SWITCH

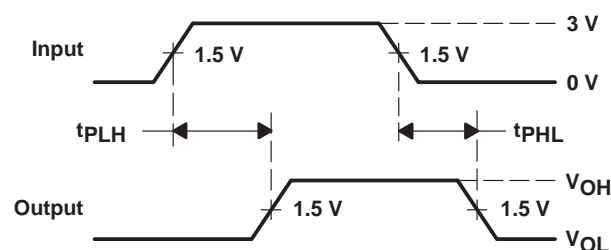
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#### PARAMETER MEASUREMENT INFORMATION

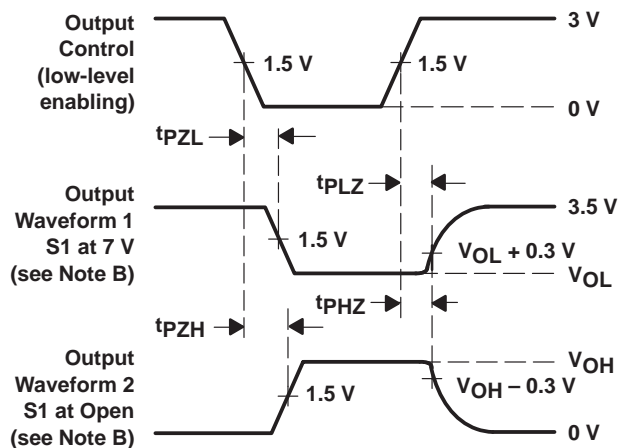


LOAD CIRCUIT



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES

| TEST              | S1   |
|-------------------|------|
| $t_{pd}$          | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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