

MC34151, MC33151

High Speed Dual MOSFET Drivers

The MC34151/MC33151 are dual inverting high speed drivers specifically designed for applications that require low current digital circuitry to drive large capacitive loads with high slew rates. These devices feature low input current making them CMOS and LSTTL logic compatible, input hysteresis for fast output switching that is independent of input transition time, and two high current totem pole outputs ideally suited for driving power MOSFETs. Also included is an undervoltage lockout with hysteresis to prevent erratic system operation at low supply voltages.

Typical applications include switching power supplies, dc to dc converters, capacitor charge pump voltage doublers/inverters, and motor controllers.

These devices are available in dual-in-line and surface mount packages.

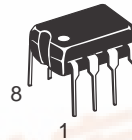
- Two Independent Channels with 1.5 A Totem Pole Output
- Output Rise and Fall Times of 15 ns with 1000 pF Load
- CMOS/LSTTL Compatible Inputs with Hysteresis
- Undervoltage Lockout with Hysteresis
- Low Standby Current
- Efficient High Frequency Operation
- Enhanced System Performance with Common Switching Regulator Control ICs
- Pin Out Equivalent to DS0026 and MMH0026



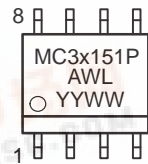
ON Semiconductor

<http://onsemi.com>

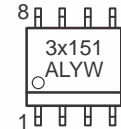
MARKING DIAGRAMS



**PDIP-8
P SUFFIX
CASE 626**

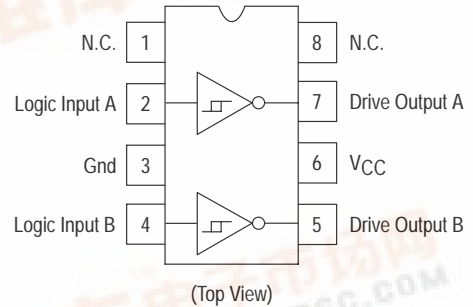


**SO-8
D SUFFIX
CASE 751**

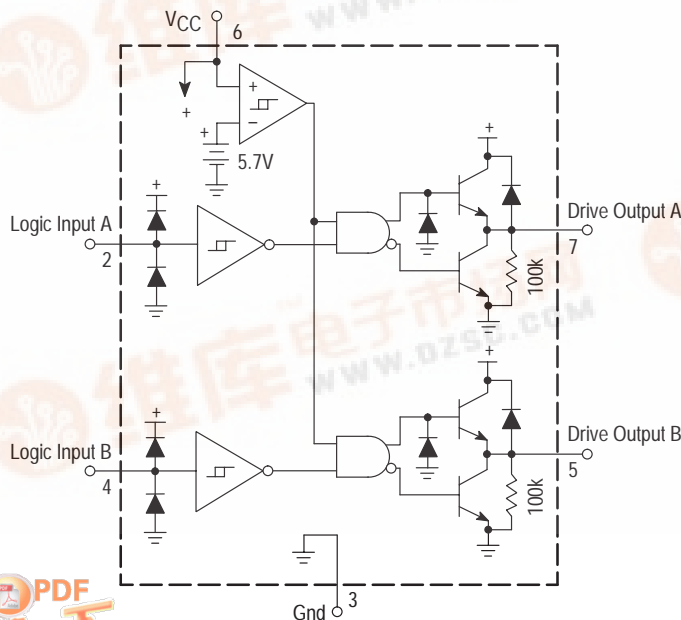


- x = 3 or 4
- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week

PIN CONNECTIONS



Representative Block Diagram



ORDERING INFORMATION

Device	Package	Shipping
MC34151D	SO-8	98 Units/Rail
MC34151DR2	SO-8	2500 Tape & Reel
MC34151P	PDIP-8	50 Units/Rail
MC33151D	SO-8	98 Units/Rail
MC33151DR2	SO-8	2500 Tape & Reel
MC33151P	PDIP-8	50 Units/Rail
MC33151VDR2	SO-8	2500 Units/Rail



MC34151, MC33151

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Logic Inputs (Note 1.)	V_{in}	-0.3 to V_{CC}	V
Drive Outputs (Note 2.) Totem Pole Sink or Source Current Diode Clamp Current (Drive Output to V_{CC})	I_O $I_{O(clamp)}$	1.5 1.0	A
Power Dissipation and Thermal Characteristics D Suffix SO-8 Package Case 751 Maximum Power Dissipation @ $T_A = 50^\circ\text{C}$ Thermal Resistance, Junction-to-Air P Suffix 8-Pin Package Case 626 Maximum Power Dissipation @ $T_A = 50^\circ\text{C}$ Thermal Resistance, Junction-to-Air	P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	0.56 180 1.0 100	W $^\circ\text{C/W}$ W $^\circ\text{C/W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Ambient Temperature MC34151 MC33151	T_A	0 to +70 -40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 12\text{ V}$, for typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the only operating ambient temperature range that applies [Note 3.], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
-----------------	--------	-----	-----	-----	------

LOGIC INPUTS

Input Threshold Voltage – High State Logic 1 – Low State Logic 0	V_{IH} V_{IL}	2.6 –	1.75 1.58	– 0.8	V
Input Current – High State ($V_{IH} = 2.6\text{ V}$) – Low State ($V_{IL} = 0.8\text{ V}$)	I_{IH} I_{IL}	– –	200 20	500 100	μA

DRIVE OUTPUT

Output Voltage – Low State ($I_{Sink} = 10\text{ mA}$) ($I_{Sink} = 50\text{ mA}$) ($I_{Sink} = 400\text{ mA}$) – High State ($I_{Source} = 10\text{ mA}$) ($I_{Source} = 50\text{ mA}$) ($I_{Source} = 400\text{ mA}$)	V_{OL} V_{OH}	– – – 10.5 10.4 9.5	0.8 1.1 1.7 11.2 11.1 10.9	1.2 1.5 2.5 – – –	V
Output Pull-Down Resistor	R_{PD}	–	100	–	$\text{k}\Omega$

SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Propagation Delay (10% Input to 10% Output, $C_L = 1.0\text{ nF}$) Logic Input to Drive Output Rise Logic Input to Drive Output Fall	$t_{PLH(in/out)}$ $t_{PHL(in/out)}$	– –	35 36	100 100	ns
Drive Output Rise Time (10% to 90%) $C_L = 1.0\text{ nF}$ $C_L = 2.5\text{ nF}$	t_r	– –	14 31	30 –	ns
Drive Output Fall Time (90% to 10%) $C_L = 1.0\text{ nF}$ $C_L = 2.5\text{ nF}$	t_f	– –	16 32	30 –	ns

TOTAL DEVICE

Power Supply Current Standby (Logic Inputs Grounded) Operating ($C_L = 1.0\text{ nF}$ Drive Outputs 1 and 2, $f = 100\text{ kHz}$)	I_{CC}	– –	6.0 10.5	10 15	mA
Operating Voltage	V_{CC}	6.5	–	18	V

- For optimum switching speed, the maximum input voltage should be limited to 10 V or V_{CC} , whichever is less.
- Maximum package power dissipation limits must be observed.
- $T_{low} = 0^\circ\text{C}$ for MC34151
–40 $^\circ\text{C}$ for MC33151
 $T_{high} = +70^\circ\text{C}$ for MC34151
+85 $^\circ\text{C}$ for MC33151

MC34151, MC33151

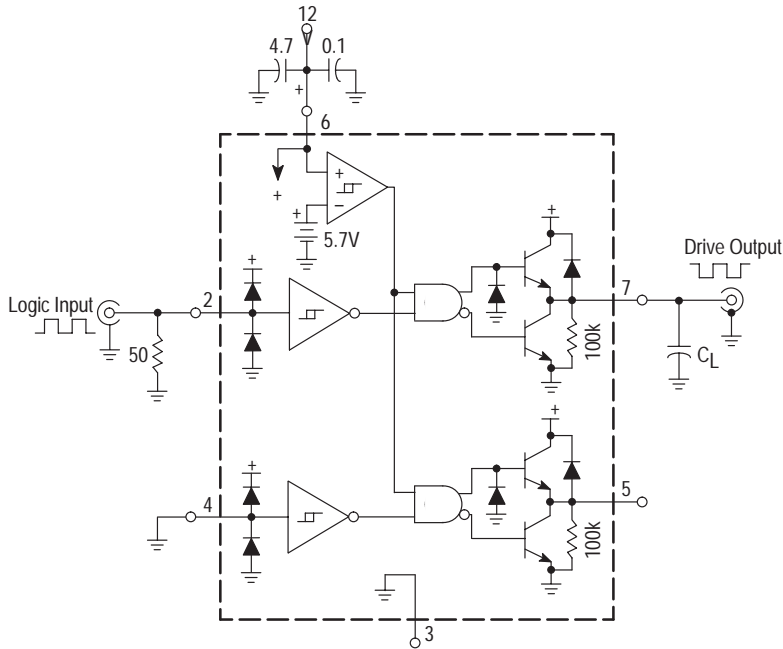


Figure 1. Switching Characteristics Test Circuit

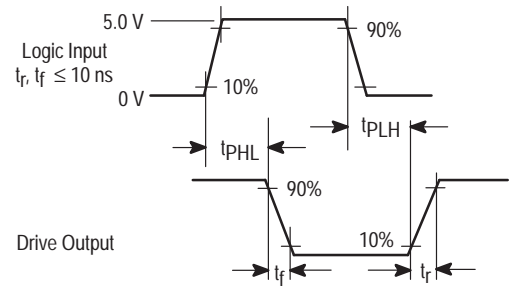


Figure 2. Switching Waveform Definitions

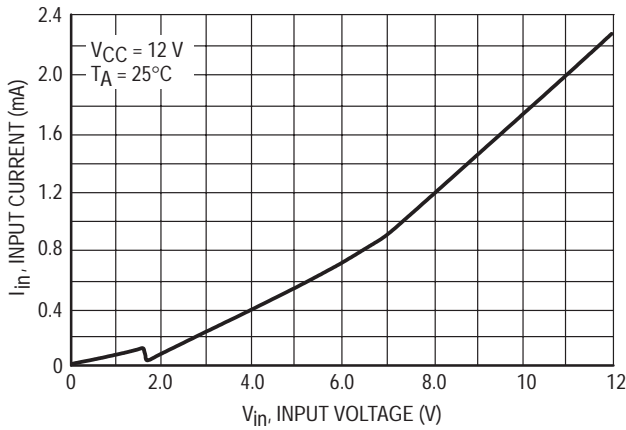


Figure 3. Logic Input Current versus Input Voltage

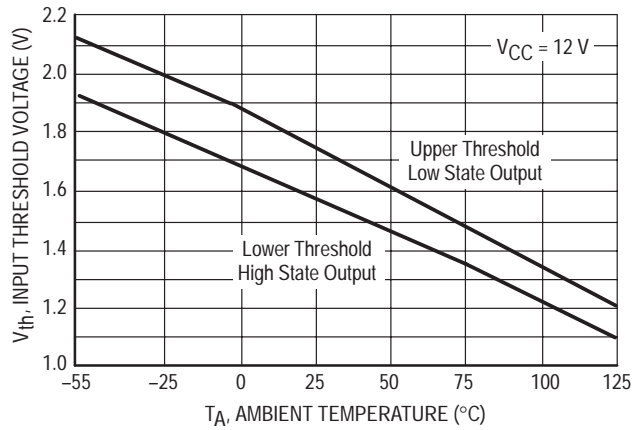


Figure 4. Logic Input Threshold Voltage versus Temperature

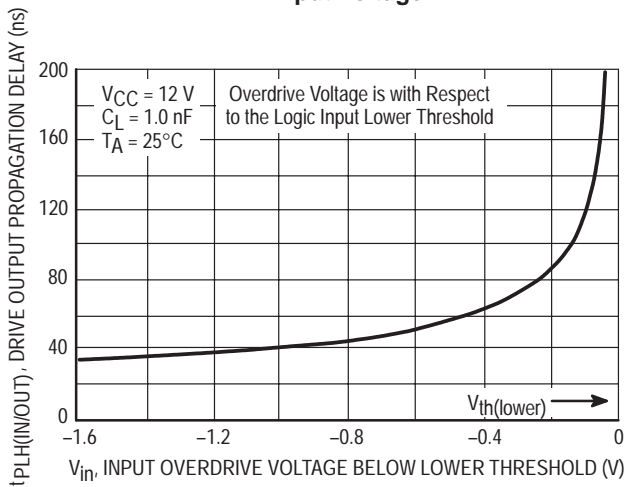


Figure 5. Drive Output Low-to-High Propagation Delay versus Logic Overdrive Voltage

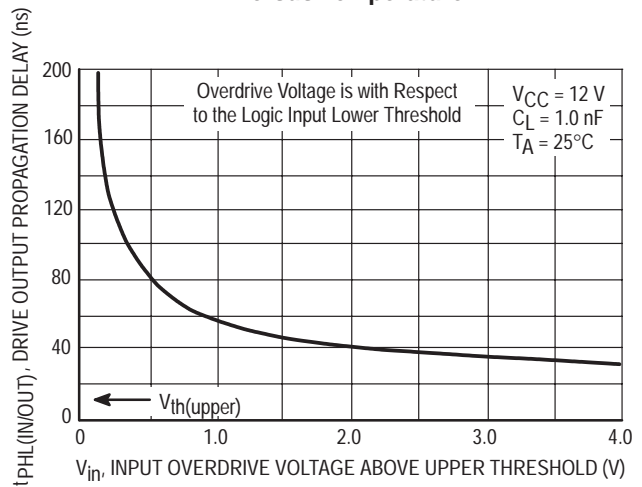


Figure 6. Drive Output High-to-Low Propagation Delay versus Logic Input Overdrive Voltage

MC34151, MC33151

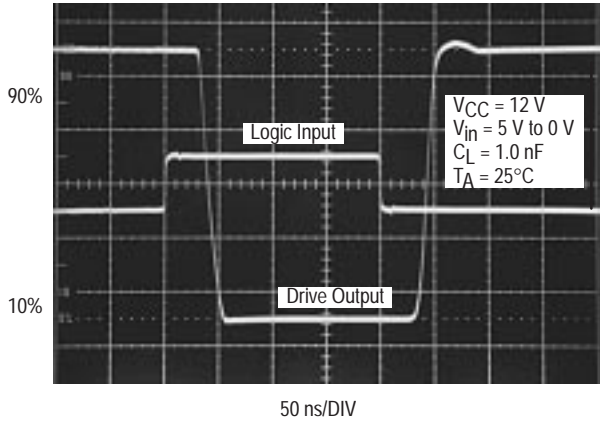


Figure 7. Propagation Delay

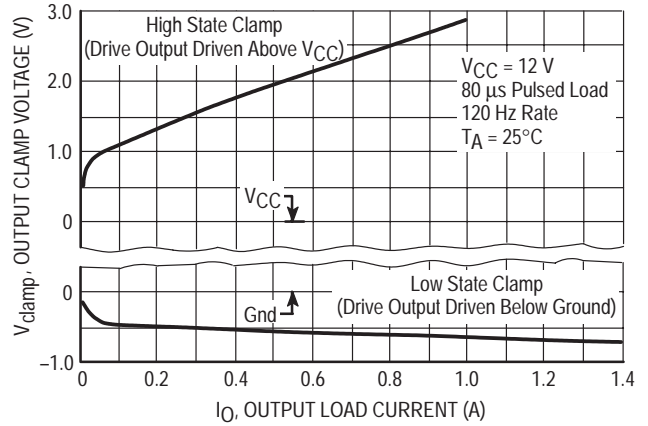


Figure 8. Drive Output Clamp Voltage versus Clamp Current

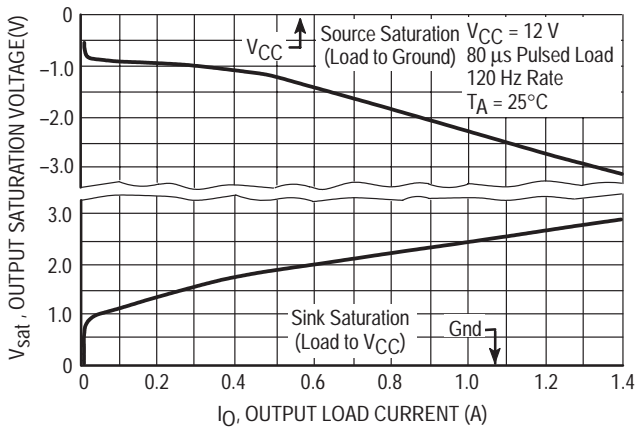


Figure 9. Drive Output Saturation Voltage versus Load Current

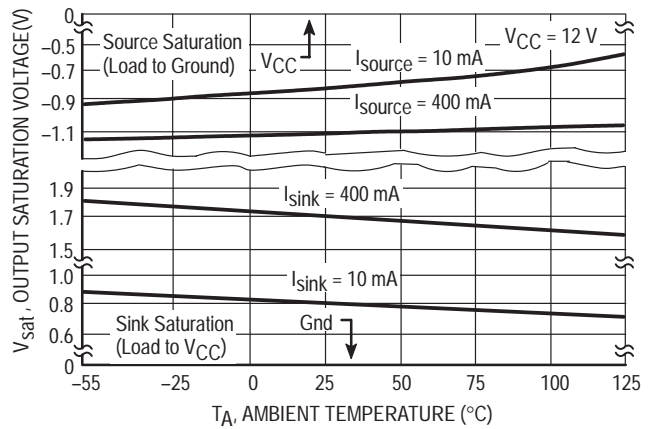


Figure 10. Drive Output Saturation Voltage versus Temperature

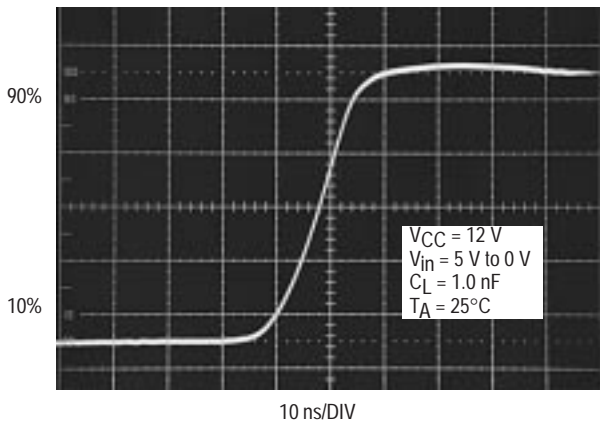


Figure 11. Drive Output Rise Time

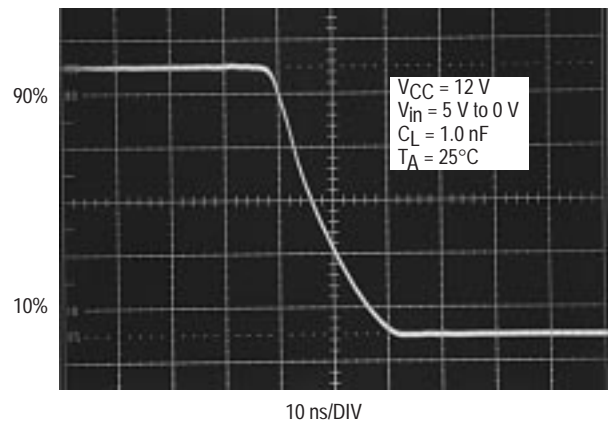


Figure 12. Drive Output Fall Time

MC34151, MC33151

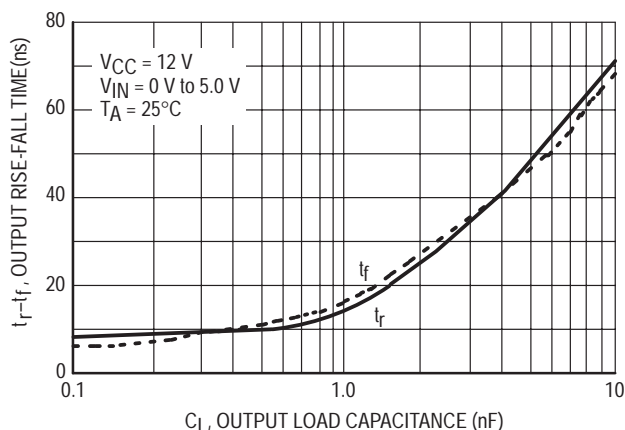


Figure 13. Drive Output Rise and Fall Time versus Load Capacitance

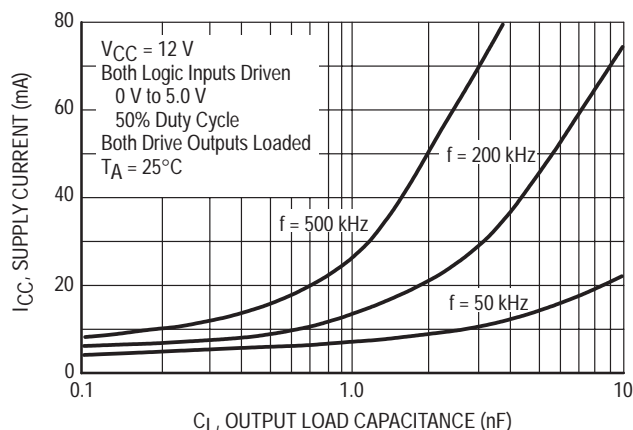


Figure 14. Supply Current versus Drive Output Load Capacitance

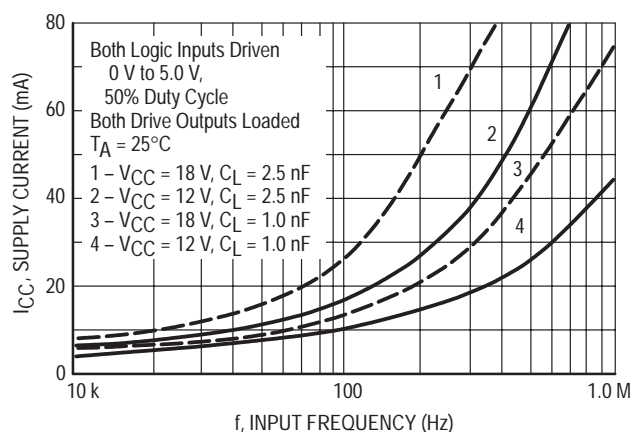


Figure 15. Supply Current versus Input Frequency

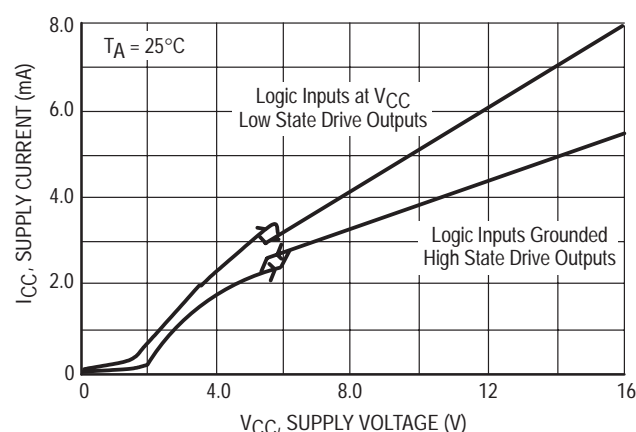


Figure 16. Supply Current versus Supply Voltage

APPLICATIONS INFORMATION

Description

The MC34151 is a dual inverting high speed driver specifically designed to interface low current digital circuitry with power MOSFETs. This device is constructed with Schottky clamped Bipolar Analog technology which offers a high degree of performance and ruggedness in hostile industrial environments.

Input Stage

The Logic Inputs have 170 mV of hysteresis with the input threshold centered at 1.67 V. The input thresholds are insensitive to V_{CC} making this device directly compatible with CMOS and LSTTL logic families over its entire operating voltage range. Input hysteresis provides fast output switching that is independent of the input signal transition time, preventing output oscillations as the input thresholds are crossed. The inputs are designed to accept a signal amplitude ranging from ground to V_{CC} . This allows the output of one channel to directly drive the input of a second channel for master-slave operation. Each input has a 30 k Ω pull-down resistor so that an unconnected open input will cause the associated Drive Output to be in a known high state.

Output Stage

Each totem pole Drive Output is capable of sourcing and sinking up to 1.5 A with a typical 'on' resistance of 2.4 Ω at 1.0 A. The low 'on' resistance allows high output currents to be attained at a lower V_{CC} than with comparative CMOS drivers. Each output has a 100 k Ω pull-down resistor to keep the MOSFET gate low when V_{CC} is less than 1.4 V. No over current or thermal protection has been designed into the device, so output shorting to V_{CC} or ground must be avoided.

Parasitic inductance in series with the load will cause the driver outputs to ring above V_{CC} during the turn-on transition, and below ground during the turn-off transition. With CMOS drivers, this mode of operation can cause a destructive output latch-up condition. The MC34151 is immune to output latch-up. The Drive Outputs contain an internal diode to V_{CC} for clamping positive voltage transients. When operating with V_{CC} at 18 V, proper power supply bypassing must be observed to prevent the output ringing from exceeding the maximum 20 V device rating. Negative output transients are clamped by the internal NPN pull-up transistor. Since full supply voltage is applied across

MC34151, MC33151

the NPN pull-up during the negative output transient, power dissipation at high frequencies can become excessive. Figures 19, 20, and 21 show a method of using external Schottky diode clamps to reduce driver power dissipation.

Undervoltage Lockout

An undervoltage lockout with hysteresis prevents erratic system operation at low supply voltages. The UVLO forces the Drive Outputs into a low state as V_{CC} rises from 1.4 V to the 5.8 V upper threshold. The lower UVLO threshold is 5.3 V, yielding about 500 mV of hysteresis.

Power Dissipation

Circuit performance and long term reliability are enhanced with reduced die temperature. Die temperature increase is directly related to the power that the integrated circuit must dissipate and the total thermal resistance from the junction to ambient. The formula for calculating the junction temperature with the package in free air is:

$$T_J = T_A + P_D (R_{\theta JA})$$

where: T_J = Junction Temperature

T_A = Ambient Temperature

P_D = Power Dissipation

$R_{\theta JA}$ = Thermal Resistance Junction to Ambient

There are three basic components that make up total power to be dissipated when driving a capacitive load with respect to ground. They are:

$$P_D = P_Q + P_C + P_T$$

where: P_Q = Quiescent Power Dissipation

P_C = Capacitive Load Power Dissipation

P_T = Transition Power Dissipation

The quiescent power supply current depends on the supply voltage and duty cycle as shown in Figure 16. The device's quiescent power dissipation is:

$$P_Q = V_{CC} \left(I_{CCL} (1-D) + I_{CCH} (D) \right)$$

where: I_{CCL} = Supply Current with Low State Drive Outputs

I_{CCH} = Supply Current with High State Drive Outputs

D = Output Duty Cycle

The capacitive load power dissipation is directly related to the load capacitance value, frequency, and Drive Output voltage swing. The capacitive load power dissipation per driver is:

$$P_C = V_{CC} (V_{OH} - V_{OL}) C_L f$$

where: V_{OH} = High State Drive Output Voltage

V_{OL} = Low State Drive Output Voltage

C_L = Load Capacitance

f = frequency

When driving a MOSFET, the calculation of capacitive load power P_C is somewhat complicated by the changing gate to source capacitance C_{GS} as the device switches. To aid in this calculation, power MOSFET manufacturers provide

gate charge information on their data sheets. Figure 17 shows a curve of gate voltage versus gate charge for the ON Semiconductor MTM15N50. Note that there are three distinct slopes to the curve representing different input capacitance values. To completely switch the MOSFET 'on', the gate must be brought to 10 V with respect to the source. The graph shows that a gate charge Q_g of 110 nC is required when operating the MOSFET with a drain to source voltage V_{DS} of 400 V.

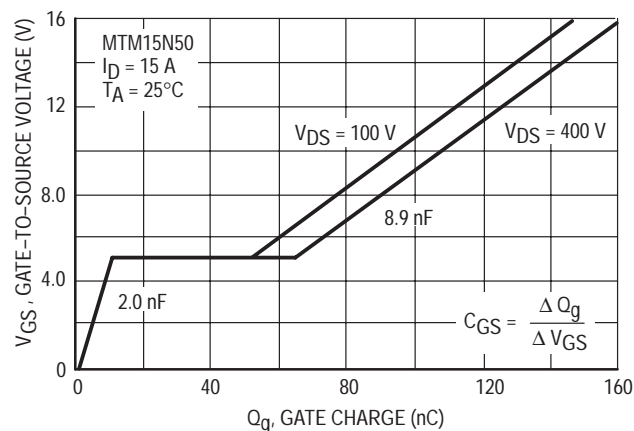


Figure 17. Gate-To-Source Voltage versus Gate Charge

The capacitive load power dissipation is directly related to the required gate charge, and operating frequency. The capacitive load power dissipation per driver is:

$$P_C(\text{MOSFET}) = V_C Q_g f$$

The flat region from 10 nC to 55 nC is caused by the drain-to-gate Miller capacitance, occurring while the MOSFET is in the linear region dissipating substantial amounts of power. The high output current capability of the MC34151 is able to quickly deliver the required gate charge for fast power efficient MOSFET switching. By operating the MC34151 at a higher V_{CC} , additional charge can be provided to bring the gate above 10 V. This will reduce the 'on' resistance of the MOSFET at the expense of higher driver dissipation at a given operating frequency.

The transition power dissipation is due to extremely short simultaneous conduction of internal circuit nodes when the Drive Outputs change state. The transition power dissipation per driver is approximately:

$$P_T \approx 9 V_{CC} (1.08 V_{CC} C_L f - 8 \times 10^{-4})$$

P_T must be greater than zero.

Switching time characterization of the MC34151 is performed with fixed capacitive loads. Figure 13 shows that for small capacitance loads, the switching speed is limited by transistor turn-on/off time and the slew rate of the internal nodes. For large capacitance loads, the switching speed is limited by the maximum output current capability of the integrated circuit.

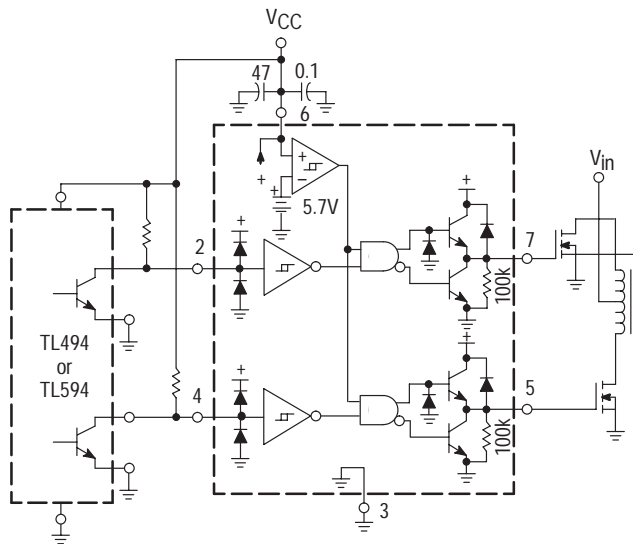
MC34151, MC33151

LAYOUT CONSIDERATIONS

High frequency printed circuit layout techniques are imperative to prevent excessive output ringing and overshoot. **Do not attempt to construct the driver circuit on wire-wrap or plug-in prototype boards.** When driving large capacitive loads, the printed circuit board must contain a low inductance ground plane to minimize the voltage spikes induced by the high ground ripple currents. All high current loops should be kept as short as possible using heavy copper runs to provide a low impedance high frequency path. For

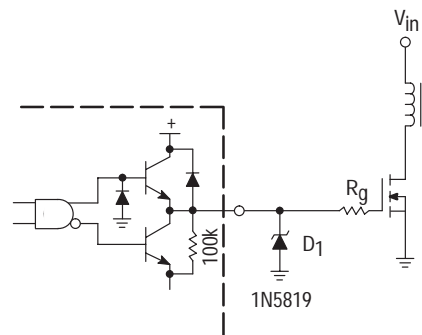
optimum drive performance, it is recommended that the initial circuit design contains dual power supply bypass capacitors connected with short leads as close to the VCC pin and ground as the layout will permit. Suggested capacitors are a low inductance 0.1 μF ceramic in parallel with a 4.7 μF tantalum. Additional bypass capacitors may be required depending upon Drive Output loading and circuit layout.

Proper printed circuit board layout is extremely critical and cannot be over emphasized.



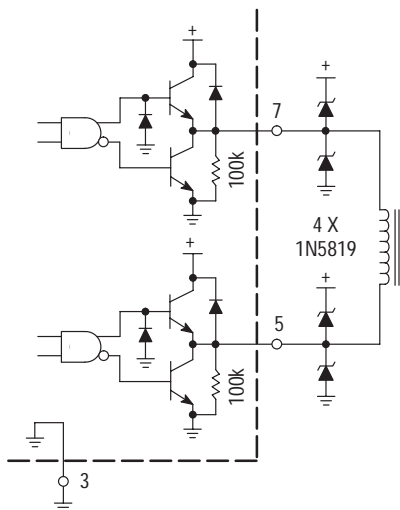
The MC34151 greatly enhances the drive capabilities of common switching regulators and CMOS/TTL logic devices.

Figure 18. Enhanced System Performance with Common Switching Regulators



Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D_1 can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 19. MOSFET Parasitic Oscillations



Output Schottky diodes are recommended when driving inductive loads at high frequencies. The diodes reduce the driver's power dissipation by preventing the output pins from being driven above V_{CC} and below ground.

Figure 20. Direct Transformer Drive

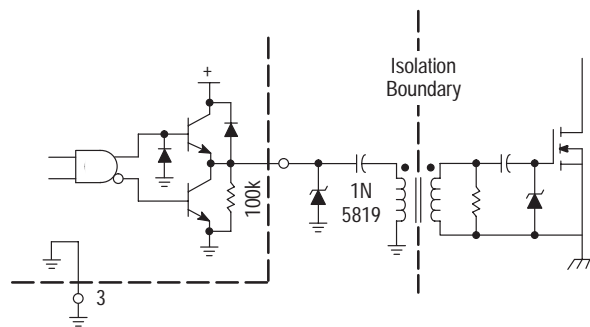
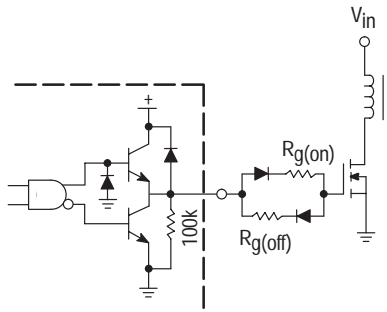


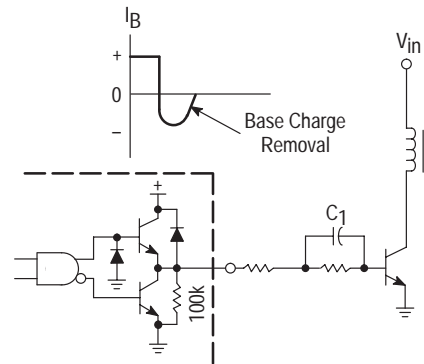
Figure 21. Isolated MOSFET Drive

MC34151, MC33151



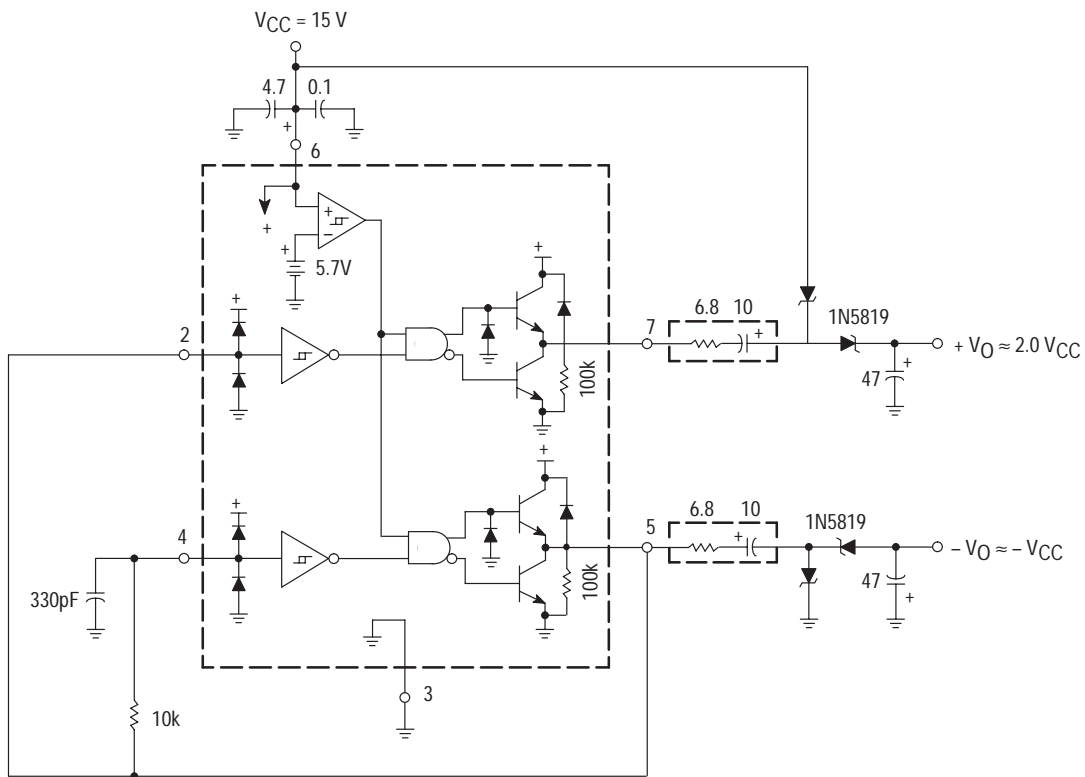
In noise sensitive applications, both conducted and radiated EMI can be reduced significantly by controlling the MOSFET's turn-on and turn-off times.

Figure 22. Controlled MOSFET Drive



The totem-pole outputs can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1 .

Figure 23. Bipolar Transistor Drive



The capacitor's equivalent series resistance limits the Drive Output Current to 1.5 A. An additional series resistor may be required when using tantalum or other low ESR capacitors.

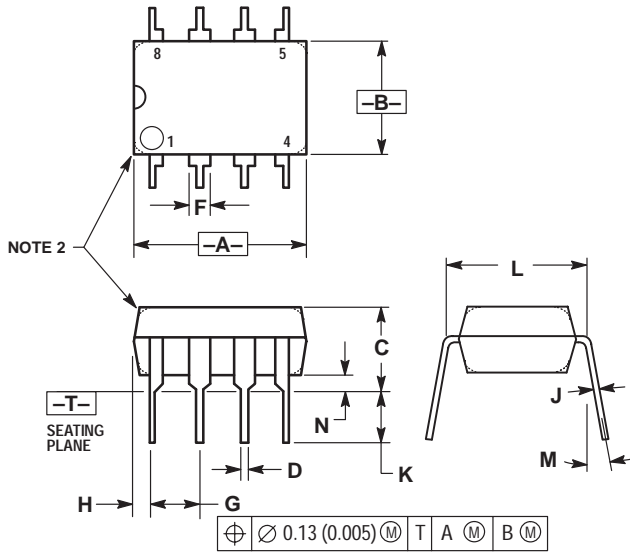
Figure 24. Dual Charge Pump Converter

Output Load Regulation		
I_O (mA)	+ V_O (V)	- V_O (V)
0	27.7	-13.3
1.0	27.4	-12.9
10	26.4	-11.9
20	25.5	-11.2
30	24.6	-10.5
50	22.6	-9.4

MC34151, MC33151

PACKAGE DIMENSIONS

PDIP-8
P SUFFIX
 CASE 626-05
 ISSUE K

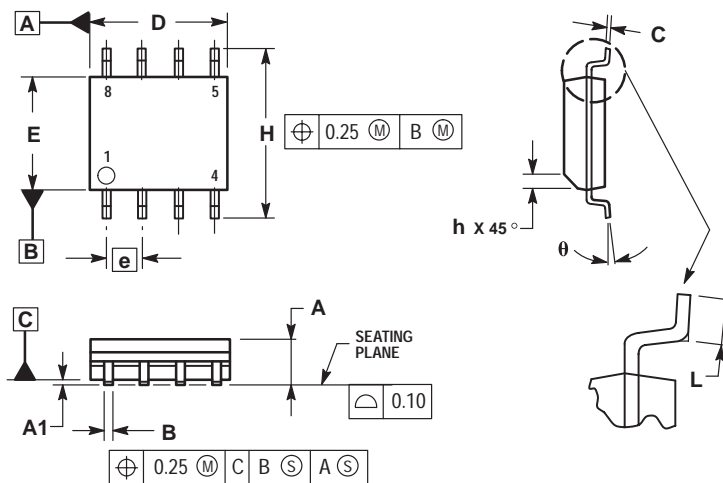


NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

SO-8
D SUFFIX
 CASE 751-06
 ISSUE T



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°


MC34151, MC33151

Notes

MC34151, MC33151

Notes

MC34151, MC33151

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (M-F 1:00pm to 5:00pm Munich Time)
Email: ONlit-german@hibbertco.com
French Phone: (+1) 303-308-7141 (M-F 1:00pm to 5:00pm Toulouse Time)
Email: ONlit-french@hibbertco.com
English Phone: (+1) 303-308-7142 (M-F 12:00pm to 5:00pm UK Time)
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS*: 00-800-4422-3781

*Available from Germany, France, Italy, England, Ireland

CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)
Email: ONlit-spanish@hibbertco.com

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001-800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549

Phone: 81-3-5740-2745
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.