



## LTC1981/LTC1982

Single and Dual Micropower  
High Side Switch Controllers  
in SOT-23

## FEATURES

- No External Components Required
- Internal Voltage Triplers Produce High Side Gate Drive for Logic Level FETs
- Ultralow Power:
  - 10 $\mu$ A Per Driver ON Current (LTC1982)
  - 20 $\mu$ A ON Current (LTC1981)
  - <1 $\mu$ A Shutdown Current
- V<sub>CC</sub> Range: 1.8V to 5V
- Gate Drive Outputs Driven to Ground During Shutdown
- Gate Drive Outputs Internally Clamped to 7.5V Max
- "Gate Drive Ready" Output (LTC1981)
- Ultrasmall Application Circuit
- 5-Pin SOT-23 Package (LTC1981)
- 6-Pin SOT-23 Package (LTC1982)

## APPLICATIONS

- Cellular Telephones
- Portable POS Terminal
- Handheld Battery Powered Equipment

## DESCRIPTION

The LTC<sup>®</sup>1981/LTC1982 are low-power, self-contained N-channel MOSFET drivers. An internal voltage tripler allows gates to be driven without the use of any external components. Internal regulation circuitry allows quiescent current to drop to 10 $\mu$ A per driver (20 $\mu$ A for LTC1981) once the gates are charged.

Low quiescent current and low shutdown current (under 1 $\mu$ A) make these parts ideal for battery and other power constrained systems. The wide input voltage range accommodates a variety of battery/input configurations.

Gate drive is internally clamped to 7.5V providing protection to the external MOSFET gate. The MOSFETs can be driven in either high side or low side mode.

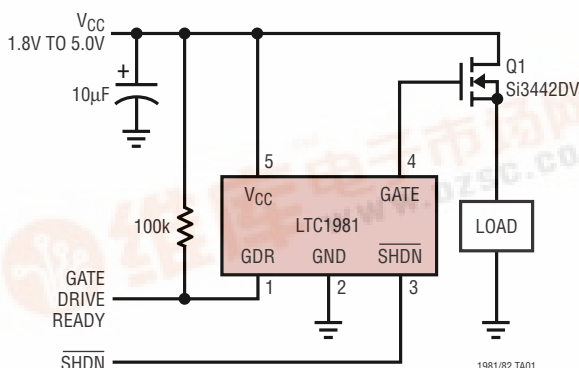
The LTC1981 single driver version also includes a gate drive ready pin and twice the drive current capacity of the dual driver LTC1982.

The LTC1981 is available in a 5-pin SOT-23. The LTC1982 is available in a 6-pin SOT-23.

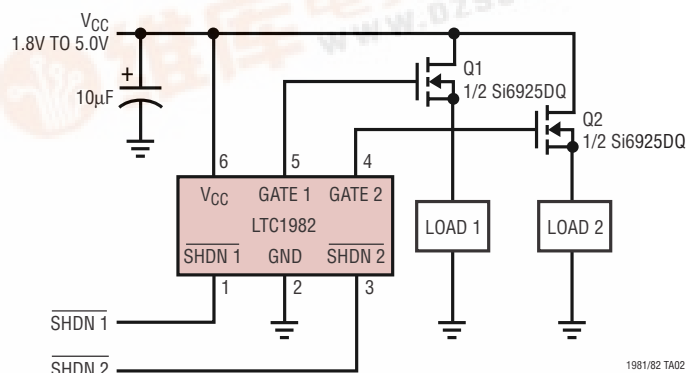
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## TYPICAL APPLICATIONS

Single High Side Switch Controller



Dual High Side Switch Controller



# LTC1981/LTC1982

## ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

### Terminal Voltage

LTC1981:  $V_{CC}$ , GATE,  $\overline{SHDN}$ , GDR ..... -0.3V to 7.5V

LTC1982:  $V_{CC}$ , GATE 1, GATE 2,  
SHDN 1, SHDN 2 ..... -0.3V to 7.5V

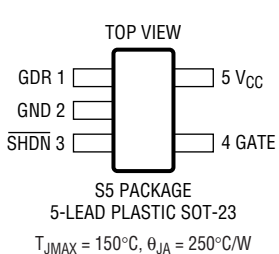
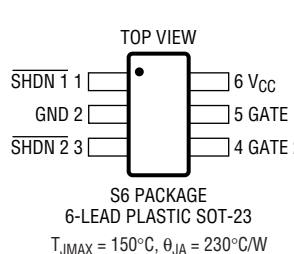
### Operating Temperature Range

LTC1981E/LTC1982E (Note 3) ..... -40°C to 85°C

Storage Temperature Range ..... -65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION

|   |                   |  |                   |
|---|-------------------|--|-------------------|
|  | ORDER PART NUMBER |  | ORDER PART NUMBER |
|   | LTC1981ES5        |  | LTC1982ES6        |
|   | S5 PART MARKING   |  | S6 PART MARKING   |
|   | LTSF              |  | LTPF              |

Consult factory for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ . $V_{CC} = 5\text{V}$ unless otherwise specified. $C_{GATE\ 1} = C_{GATE\ 2} = C_{GATE} = 1000\text{pF}$ .

| SYMBOL     | PARAMETER                               | CONDITIONS  | MIN | TYP  | MAX     | UNITS         |
|------------|---|---|-----|------|---------|---------------|
| $V_{CC}$   | Operating Supply Voltage                | ●   | 1.8 |      | 5.5     | V             |
| $I_{CC}$   | Supply Current                          | GATE 1 and GATE 2 Outputs High  | ●   | 17   | 30      | $\mu\text{A}$ |
|            |   | GATE 1 or GATE 2 Outputs High   | ●   | 10   | 20      | $\mu\text{A}$ |
|            |   | GATE Output High (LTC1981)  | ●   | 17   | 30      | $\mu\text{A}$ |
| $I_{SHDN}$ | $\overline{SHDN}$ Supply Current        | $\overline{SHDN}$ 1 and $\overline{SHDN}$ 2 Inputs Low  | ●   |      | 1       | $\mu\text{A}$ |
|            |   | $\overline{SHDN}$ Input Low (LTC1981)   | ●   |      | 1       | $\mu\text{A}$ |
| $V_{GATE}$ | GATE Drive Output Voltage               | $V_{CC} = 1.8\text{V}$  | ●   | 4.27 | 4.50    | V             |
|            |   | $V_{CC} = 2.7\text{V}$  | ●   | 6.40 | 6.75    | V             |
|            |   | $V_{CC} = 3.3\text{V}$  | ●   | 6.90 | 7.25    | V             |
|            |   | $V_{CC} = 5\text{V}$  | ●   | 6.90 | 7.25    | V             |
| $f_{OSC}$  | Charge Pump Oscillator Frequency        | Measured with 10k Resistor from Output to GND   |     | 600  |         | kHz           |
| $t_{ON}$   | Turn-on Time into 1000pF                | From $\overline{SHDN}$ 1, $\overline{SHDN}$ 2 Going High to GATE 1, GATE 2 = $V_{CC} + 1\text{V}$ |     | 110  |         | $\mu\text{s}$ |
|            |   | From $\overline{SHDN}$ Going High to GATE = $V_{CC} + 1\text{V}$ (LTC1981)                        |     | 85   |         | $\mu\text{s}$ |
| $t_{OFF}$  | Turn-off Time into 1000pF               | From $\overline{SHDN}$ 1, $\overline{SHDN}$ 2 Going Low to GATE 1, GATE 2, GATE = 100mV           |     | 12   |         | $\mu\text{s}$ |
| $V_{IL}$   | $\overline{SHDN}$ Input Low Voltage     | $V_{CC} = 1.8\text{V}$ to 5.5V  | ●   | 0.4  |         | V             |
| $V_{IH}$   | $\overline{SHDN}$ Input High Voltage    | $V_{CC} = 1.8\text{V}$ to 5.5V  | ●   |      | 1.6     | V             |
| $C_{IN}$   | $\overline{SHDN}$ Input Capacitance     | (Note 4)  |     | 5    |         | pF            |
| $I_{IN}$   | $\overline{SHDN}$ Input Leakage Current |   |     |      | $\pm 1$ | $\mu\text{A}$ |

**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 5\text{V}$  unless otherwise specified.  $C_{\text{GATE}1} = C_{\text{GATE}2} = C_{\text{GATE}} = 1000\text{pF}$ . (LTC1981 only)

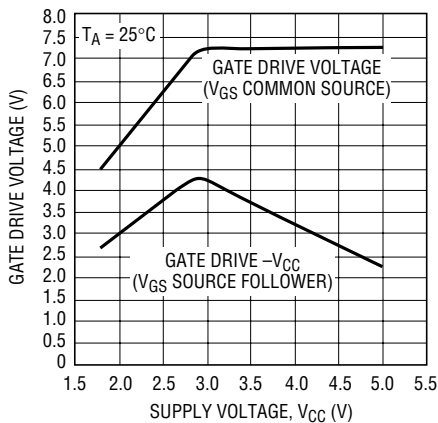
| SYMBOL   | PARAMETER                   | CONDITIONS  | MIN              | TYP                        | MAX                          | UNITS            |
|----------|-----------------------------|---|------------------|----------------------------|------------------------------|------------------|
| $V_{OL}$ | GDR Output Voltage Low      | $I_{\text{SINK}} = 100\mu\text{A}$ , $V_{CC} = 1.8\text{V}$   | ●                | 0.05                       | 0.4                          | V                |
|          | GATE Drive Ready Trip Point | GATE Voltage Rising<br>$V_{CC} = 1.8\text{V}$<br>$V_{CC} = 2.7\text{V}$<br>$V_{CC} = 3.3\text{V}$<br>$V_{CC} = 5\text{V}$ | ●<br>●<br>●<br>● | 4.05<br>6.08<br>6.5<br>6.5 | 4.25<br>6.38<br>6.82<br>6.82 | V<br>V<br>V<br>V |
|          | GDR Hysteresis              | GATE Voltage Falling  |                  | 2                          |                              | %                |
|          | GDR Delay                   | After GATE is Above the GDR Trip Threshold<br>10k Pull-Up to $V_{CC}$   |                  | 2                          |                              | $\mu\text{s}$    |

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

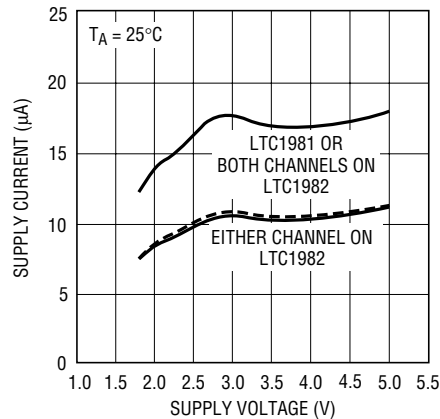
**Note 2:** All voltage values are with respect to GND.

**Note 3:** the LTC1982E is guaranteed to meet performance specifications from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ . Specifications over the  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  operating temperature range are assured by design, characterization and correlation with statistical process controls.

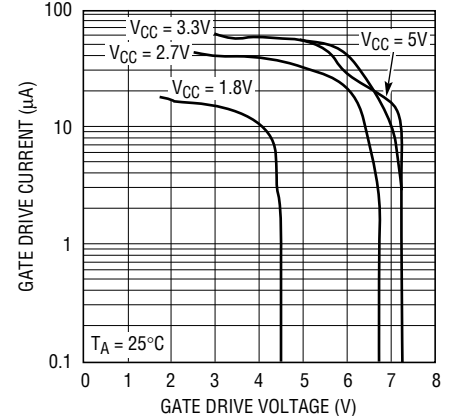
**Note 4:** Guaranteed by design not subject to test.

**TYPICAL PERFORMANCE CHARACTERISTICS****GATE Drive Voltage vs Supply Voltage**

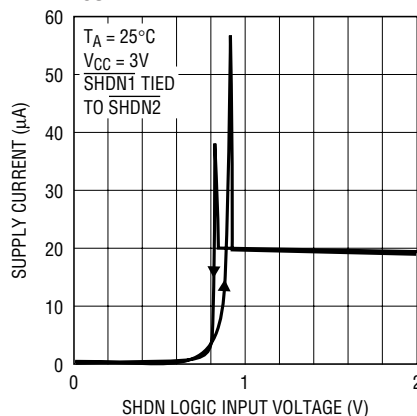
1982 G01

**Supply Current vs Supply Voltage**

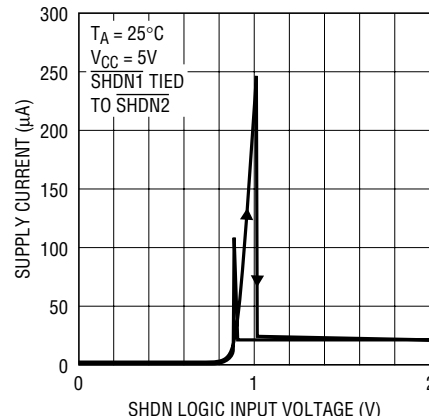
1982 G02

**GATE Drive Current (LTC1982)**

1982 G03

**ISUPPLY**

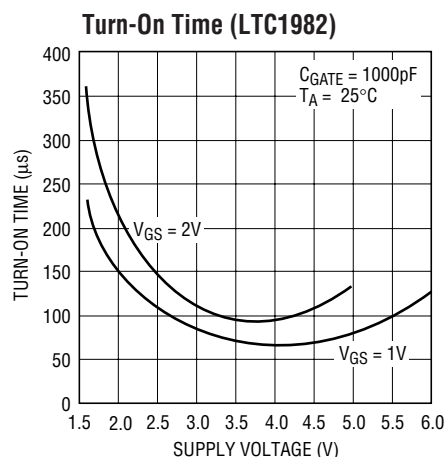
1981/82 G04

**ISUPPLY**

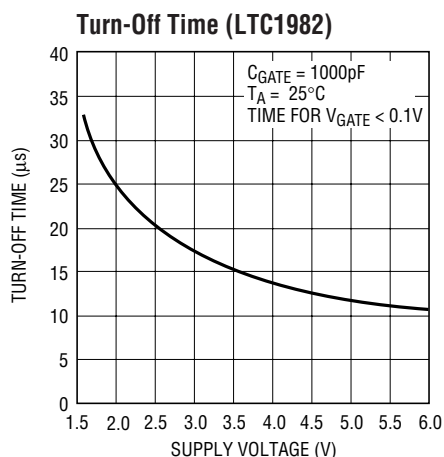
1981/82 G05

# LTC1981/LTC1982

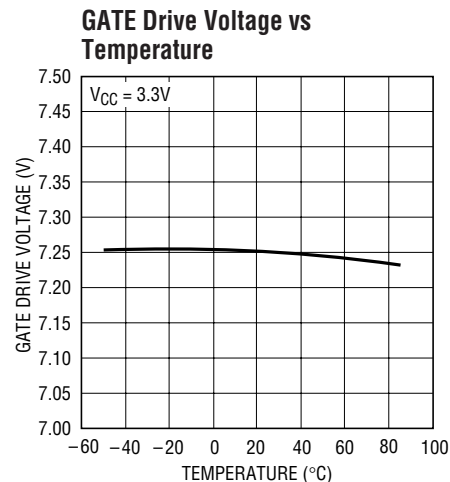
## TYPICAL PERFORMANCE CHARACTERISTICS



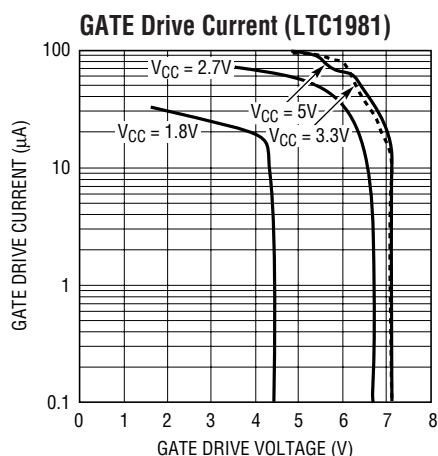
1982 G06



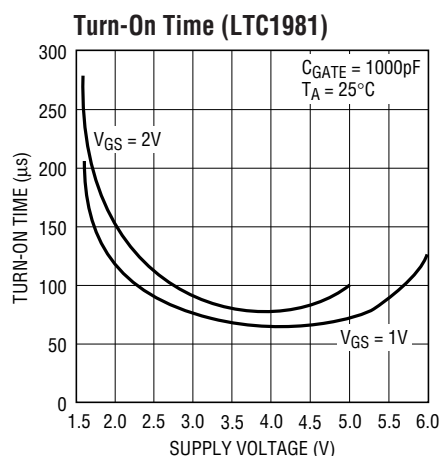
1982 G07



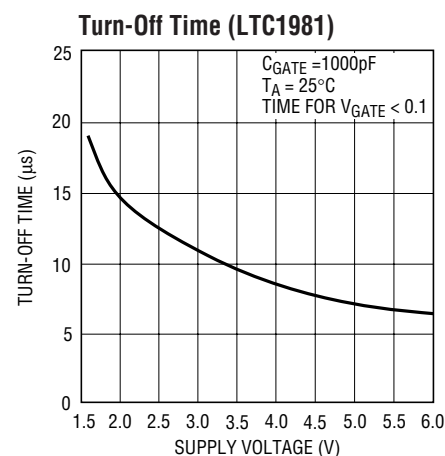
1982 G08



1981/82 G09



1981/82 G10



1981/82 G11

## PIN FUNCTIONS

### LTC1981:

**GDR (Pin 1):** Gate Drive Ready Active High Open Drain Output. Used to indicate when the gate drive output is greater than 90% of its final value.

**GND (Pin 2):** Ground.

**SHDN (Pin 3):** SHDN Active Low Input. Used to shut down the part and force the GATE output pin to ground.

**GATE (Pin 4):** Gate Drive Output to an External High Side Switch. Fully enhanced by internal charge pump. Controlled by the SHDN input pin. Output voltage on this pin will be approximately 2.5 times  $V_{CC}$  or 7.25V, whichever is less.

**$V_{CC}$  (Pin 5):** Input Supply Voltage. Range from 1.8V to 5.5V.

### LTC1982:

**SHDN 1 (Pin 1):** SHDN 1 Active Low Input. Used to shut down the GATE 1 charge pump and force the GATE 1 output pin to ground.

**GND (Pin 2):** Ground.

**SHDN 2 (Pin 3):** SHDN 2 Active Low Input. Used to shut down the GATE 2 charge pump and force the GATE 2 output pin to ground.

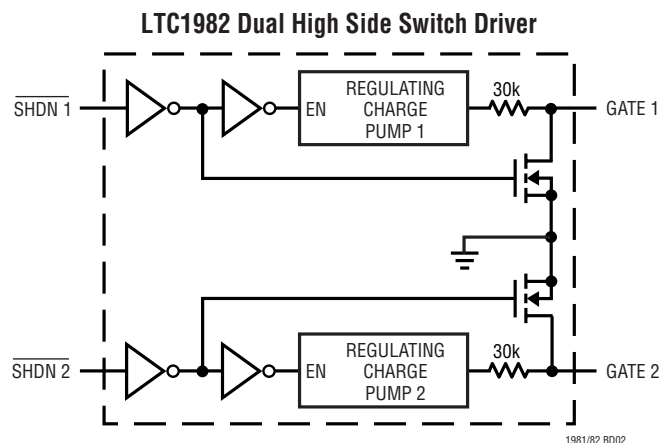
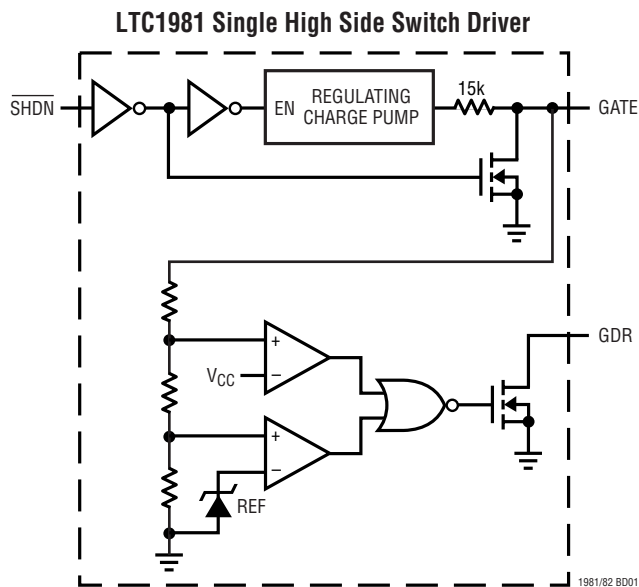
## PIN FUNCTIONS

**GATE 2 (Pin 4):** Gate Drive Output to an External High Side Switch. Fully enhanced by internal charge pump. Controlled by the  $\overline{\text{SHDN 2}}$  input pin. Output voltage on this pin will be approximately 2.5 times  $V_{CC}$  or 7.25V, whichever is less.

**GATE 1 (Pin 5):** Gate Drive Output to an External High Side Switch. Fully enhanced by internal charge pump. Controlled by the  $\overline{\text{SHDN 1}}$  input pin. Output voltage on this pin will be approximately 2.5 times  $V_{CC}$  or 7.25V, whichever is less.

**$V_{CC}$  (Pin 6):** Input Supply Voltage. Range from 1.8V to 5.5V.

## BLOCK DIAGRAMS



## OPERATION

### Charge Pump

To fully enhance the external N-channel switches, internal charge pumps are used to boost the output gate drive to approximately 2.5 times the supply voltage, or 7.25V, whichever is less. A feedback network is used to regulate the output gate drive. This keeps the supply current low in addition to providing a maximum output voltage limit. The reason for the maximum output voltage limit is to avoid switch gate source breakdown due to excessive gate overdrive.

The gate drive outputs (GATE 1, GATE 2, or GATE) are controlled by the shutdown input pins ( $\overline{\text{SHDN 1}}$ ,  $\overline{\text{SHDN 2}}$  or  $\overline{\text{SHDN}}$ ). A logic high input on one of the shutdown input pins enables the corresponding charge pump and drives

the related gate drive output pin high. A logic low input on one of the shutdown input pins disables the corresponding charge pump and drives the related gate drive output pin low. If shutdown input on the LTC1981 is low or both of the shutdown input pins on the LTC1982 are low, the part will be placed into a low current shutdown mode ( $<1\mu\text{A}$ ).

### Gate Drive Ready (LTC1981 Only)

The gate drive ready pin (GDR) is used to indicate when the gate drive output (GATE) is greater than 90% of its final value. This can be useful in applications that require knowledge of the state of the gate drive for initialization purposes or as fault detection should something be loading the gate drive down.

## APPLICATIONS INFORMATION

### Logic-Level MOSFET Switches

The LTC1981/LTC1982 are designed to operate with logic-level N-channel MOSFET switches. Although there is some variation among manufacturers, logic-level MOSFET switches are typically rated with  $V_{GS} = 4V$  with a maximum continuous  $V_{GS}$  rating of  $\pm 8V$ .  $R_{DS(ON)}$  and maximum  $V_{DS}$  ratings are similar to standard MOSFETs and there is generally little price differential. When operating at supply voltages of 5V or greater, care must be taken when selecting the MOSFET. The LTC1981/LTC1982 limit the output voltage to between 6.9V and 7.5V. The  $V_{GS}$  developed for the MOSFET may be too low to sufficiently turn on the MOSFET. MOSFETs rated at 2.5V, or less, will be better suited for applications where the supply voltages approach 5V.

### Powering Large Capacitive Loads

Electrical subsystems in portable battery-powered equipment are typically bypassed with large filter capacitors to reduce supply transients and supply induced glitching. If not properly powered however, these capacitors may themselves become the source of supply glitching. For example, if a 100 $\mu F$  capacitor is powered through a switch with a slew rate of 0.1V/ $\mu s$ , the current during start-up is:

$$\begin{aligned} I_{START} &= C(\Delta V/\Delta t) \\ &= (100 \cdot 10^{-6})(1 \cdot 10^5) \\ &= 10A \end{aligned}$$

Obviously, this is too much current for the regulator (or output capacitor) to supply and the output will glitch by as much as a few volts.

The start up current can be substantially reduced by limiting the slew rate at the gate of an N-channel as shown in Figure 1. The gate drive output of the LTC1981/LTC1982 have an internal 30k resistor (15k LTC1981) in series with each of the output gate drive pins (see Functional Block Diagram). Therefore, it only needs an external 0.1 $\mu F$  capacitor (0.22 $\mu F$  for the LTC1981) to create enough RC delay to substantially slow the slew rate of the MOSFET gate to approximately 0.6V/ms. Since the MOSFET is operating as a source follower, the slew rate at the source is essentially the same as that at the gate, reducing the startup current to approximately 60mA which is easily

managed by the system regulator. R1 is required to eliminate the possibility of parasitic MOSFET oscillations during switch transitions. It is a good practice to isolate the gates of paralleled MOSFETs with 1k resistors to decrease the possibility of interaction between switches.

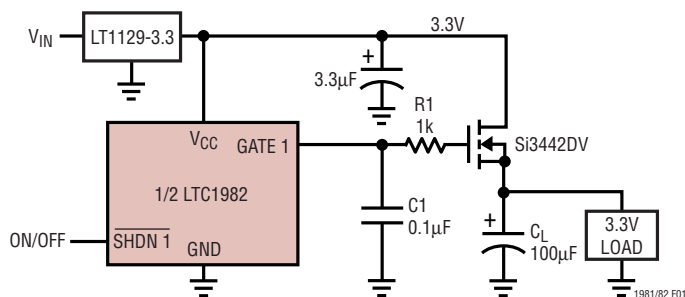


Figure 1. Powering a Large Capacitive Load

### Mixed 5V/3V Systems

Because the input ESD protection diodes are referenced to the GND pin instead of the supply pin, it is possible to drive the LTC1981/LTC1982 inputs from 5V CMOS or TTL logic even though the LTC1981/LTC1982 is powered from a 3.3V supply as shown in Figure 2. Likewise, because the input threshold voltage high is never greater than 1.6V, the reverse situation is true. The LTC1981/LTC1982 can be driven with 3V CMOS or TTL even when the supply to the device is as high as 5V as shown in Figure 3.

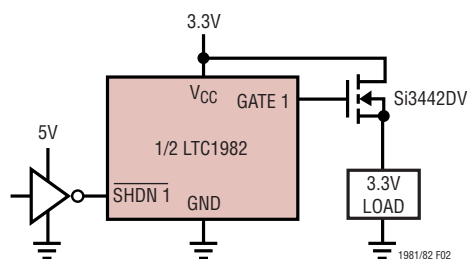


Figure 2. Direct Interface to 5V Logic

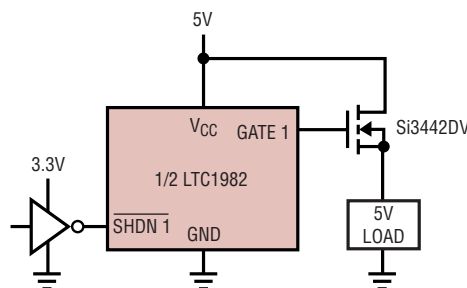


Figure 3. Direct Interface to 3.3V Logic

## APPLICATIONS INFORMATION

### Reverse Battery Protection

The LTC1981/LTC1982 can be protected against reverse battery conditions by connecting a  $150\Omega$  resistor in series with the supply pin as shown in Figure 4. The resistor limits the supply current to less than 24mA with  $-3.6V$  applied. Because the LTC1981/LTC1982 draw very little current while in normal operation, the drop across the resistor is minimal. Control logic can be protected by adding 10k resistors in series with the input pins.

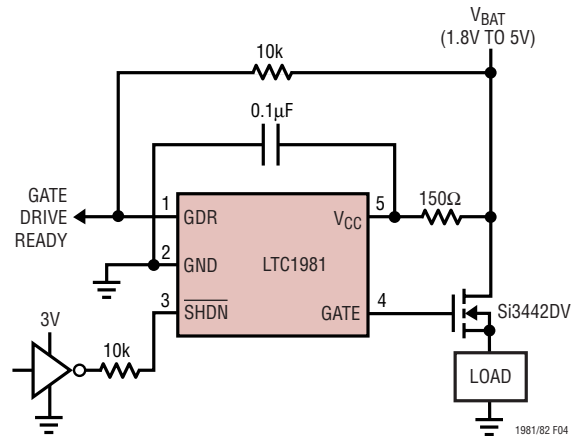
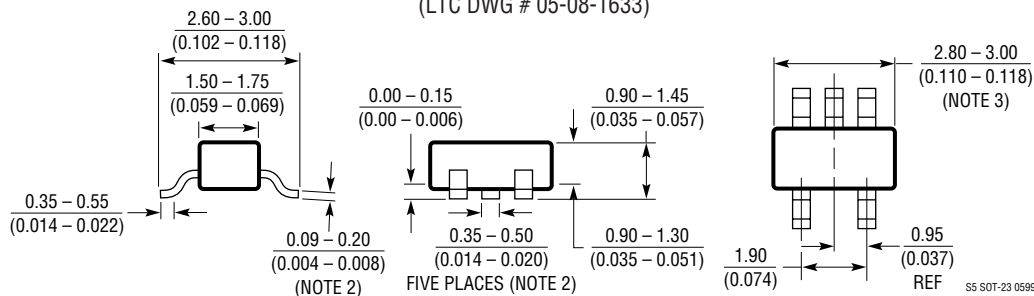


Figure 4. Reverse Battery Protection

## PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

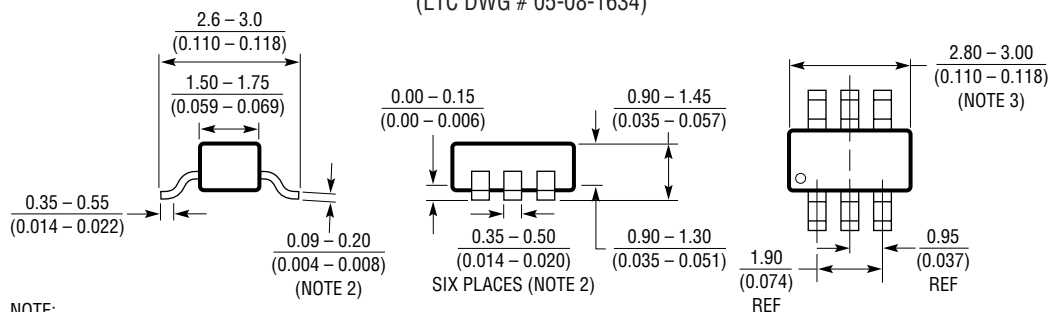
### S5 Package 5-Lead Plastic SOT-23 (LTC DWG # 05-08-1633)



NOTE:

1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
4. MOLD FLASH SHALL NOT EXCEED 0.254mm
5. PACKAGE EIAJ REFERENCE IS SC-74A (EIAJ)

### S6 Package 6-Lead Plastic SOT-23 (LTC DWG # 05-08-1634)



NOTE:

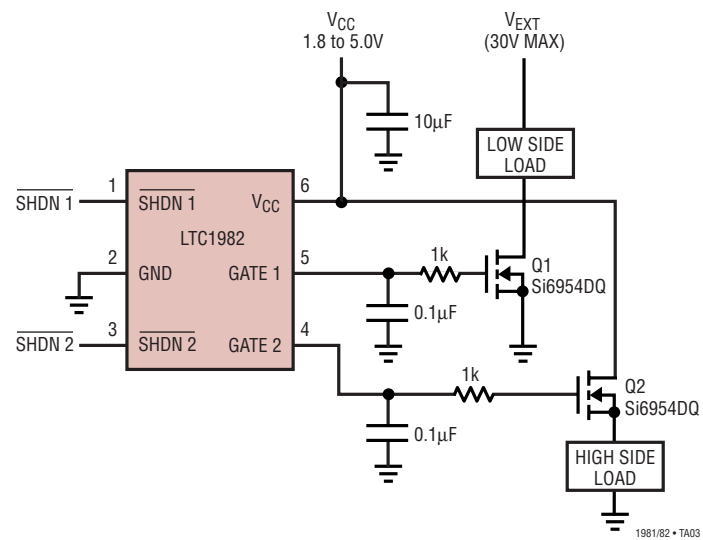
1. DIMENSIONS ARE IN MILLIMETERS
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4. MOLD FLASH SHALL NOT EXCEED 0.254mm
5. PACKAGE EIAJ REFERENCE IS SC-74A (EIAJ)



# LTC1981/LTC1982

## TYPICAL APPLICATION

Driving Both High Side and Low Side Switches



## RELATED PARTS

| PART NUMBER     | DESCRIPTION                                | COMMENTS   |
|-----------------|--|--|
| LTC1153/LTC1154 | Single High Side Micropower MOSFET Drivers | Circuit Breaker with Auto Reset                      |
| LTC1155/LTC1255 | Dual High Side Micropower MOSFET Drivers   | Latchoff Current Limit                               |
| LTC1163/LTC1165 | Triple 1.8V to 6V High Side MOSFET Driver  | Three MOSFET Drivers in 8-Lead SO Package            |
| LTC1623         | SMBus Dual High Side Switch Controller     | Uses External Switches, Two Three-State Address Pins |
| LTC1710         | SMBus Dual Monolithic High Side Switch     | Uses Internal Switches, One Three-State Address Pin  |