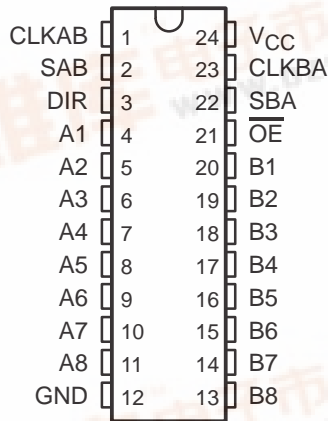


# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

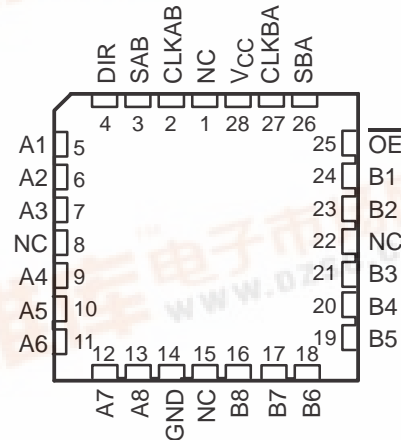
SCBS037D – AUGUST 1989 – REVISED MAY 2004

- State-of-the-Art BiCMOS Design Significantly Reduces  $I_{CCZ}$
- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

SN54BCT646 . . . JT OR W PACKAGE  
SN74BCT646 . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54BCT646 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'BCT646 devices.

Output-enable ( $\overline{OE}$ ) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when  $\overline{OE}$  is low. In the isolation mode ( $\overline{OE}$  high), A data can be stored in one register and/or B data can be stored in the other register.

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – NT	Tube	SN74BCT646NT	SN74BCT646NT
	SOIC – DW	Tube	SN74BCT646DW	BCT646
		Tape and reel	SN74BCT646DWR	
–55°C to 125°C	CDIP – JT	Tube	SNJ54BCT646JT	SNJ54BCT646JT
	CFP – W	Tube	SNJ54BCT646W	SNJ54BCT646W
	LCCC – FK	Tube	SNJ54BCT646FK	SNJ54BCT646FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



Copyright © 2004, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS037D – AUGUST 1989 – REVISED MAY 2004

---

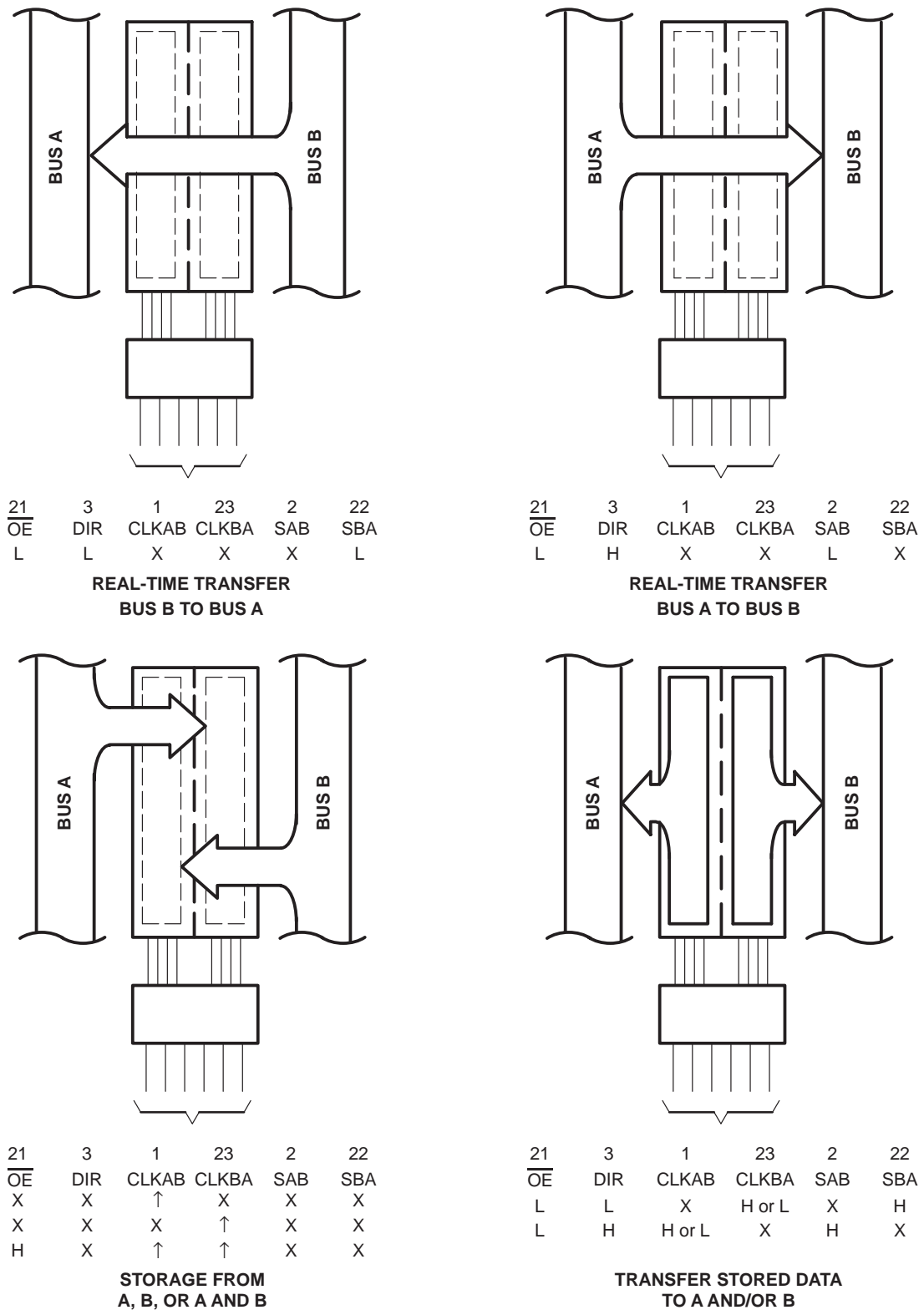
## description/ordering information(continued)

When an output function is disabled, the input function still is enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS037D – AUGUST 1989 – REVISED MAY 2004



Pin numbers shown are for the DW, JT, NT, and W packages.

**Figure 1. Bus-Management Functions**

# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

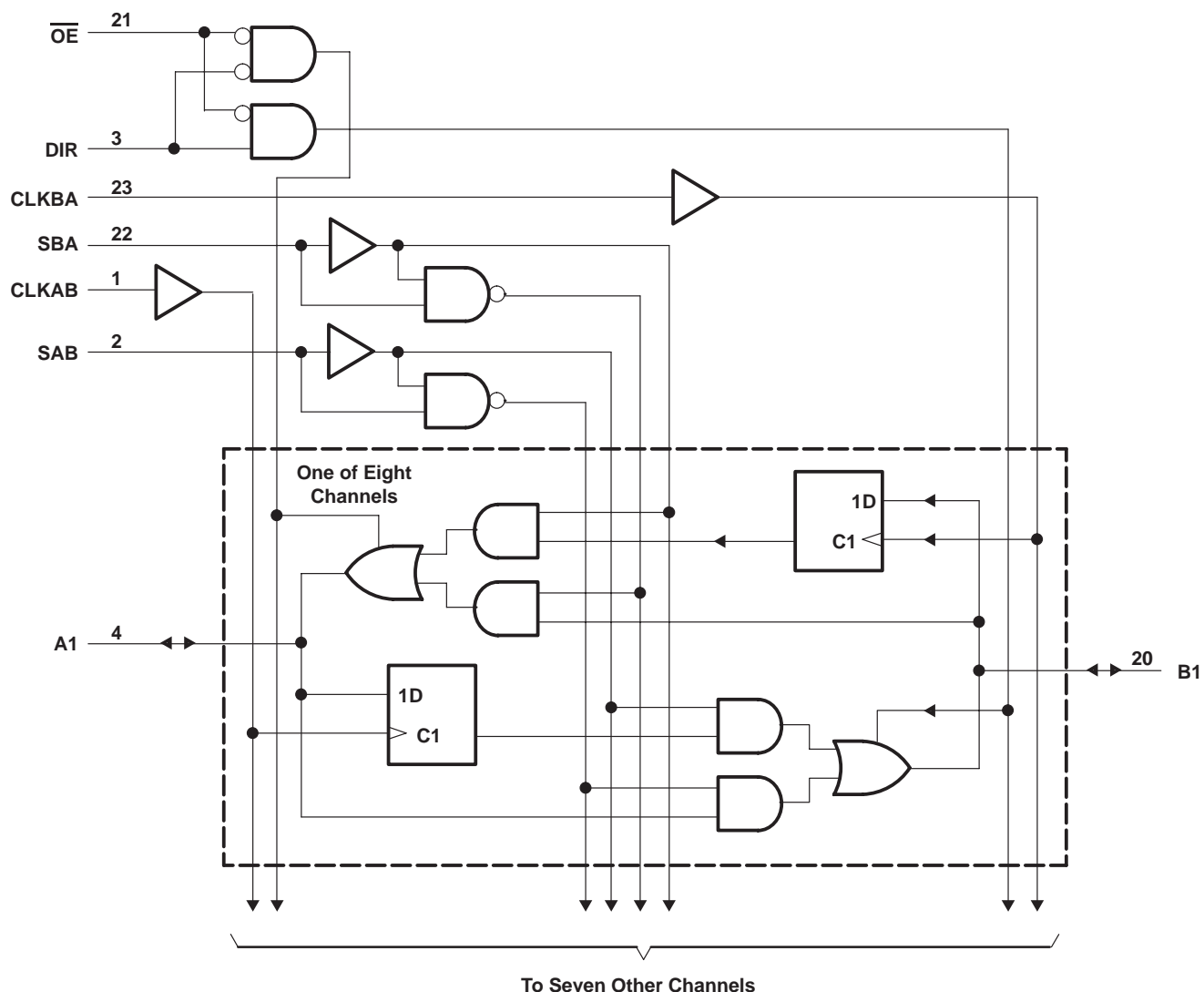
SCBS037D – AUGUST 1989 – REVISED MAY 2004

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions can be enabled or disabled by various signals at the  $\overline{OE}$  and DIR inputs. Data input functions always are enabled, i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

## logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS037D – AUGUST 1989 – REVISED MAY 2004

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range: Control inputs (see Note 1) .....	–0.5 V to 7 V
I/O ports (see Note 1) .....	–0.5 V to 5.5 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ .....	–0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ .....	–0.5 V to $V_{CC}$
Current into any output in the low state: SN54BCT646 .....	96 mA
SN74BCT646 .....	128 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package .....	46°C/W
(see Note 3): NT package .....	67°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.  
 3. The package thermal impedance is calculated in accordance with JESD 51-3.

## recommended operating conditions (see Note 4)

		SN54BCT646			SN74BCT646			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{IK}$	Input clamp current			–18			–18	mA
$I_{OH}$	High-level output current			–12			–15	mA
$I_{OL}$	Low-level output current			48			64	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS037D – AUGUST 1989 – REVISED MAY 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT646			SN74BCT646			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA		-1.2			-1.2			V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -3 mA	2.4	3.3		2.4	3.3		V
		I <sub>OH</sub> = -12 mA	2	3.2					
		I <sub>OH</sub> = -15 mA				2	3.1		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA	0.38	0.55					V
		I <sub>OL</sub> = 64 mA				0.42	0.55		
I <sub>I</sub>	A or B port	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 5.5 V	1			1			mA
	Control inputs		1			1			
I <sub>IH</sub> ‡	A or B port	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V	70			70			µA
	Control inputs		20			20			
I <sub>IL</sub> ‡	A or B port	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.5 V	-0.7			-0.7			mA
	Control inputs		-0.7			-0.7			
I <sub>OS</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0		-100		-225	-100		-225	mA
I <sub>CCL</sub>	A or B port	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = GND	42	67		42	67		mA
I <sub>CCH</sub>	A or B port	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 4.5 V	5.6	9		5.6	9		mA
I <sub>CCZ</sub>	A or B port	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = GND	10	16		10	16		mA
C <sub>i</sub>	Control inputs	V <sub>CC</sub> = 5 V, V <sub>I</sub> = 2.5 V or 0.5 V	6			6			pF
C <sub>io</sub>	A or B port	V <sub>CC</sub> = 5 V, V <sub>O</sub> = 2.5 V or 0.5 V	12			14			pF

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54BCT646		SN74BCT646		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	83		83		83		MHz
t <sub>w</sub>	Pulse duration, CLK high or low	6		6		6		ns
t <sub>su</sub>	Setup time, A or B before CLKAB↑ or CLKBA↑	6		7		6		ns
t <sub>h</sub>	Hold time, A or B after CLKAB↑ or CLKBA↑	0.5		0.5		0.5		ns

# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS037D – AUGUST 1989 – REVISED MAY 2004

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 2)

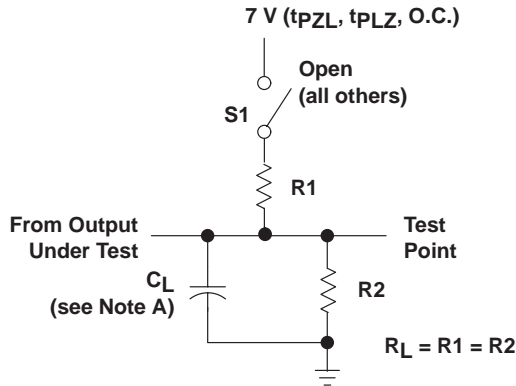
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54BCT646		SN74BCT646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			83			83		83		MHz
$t_{PLH}$	CLKBA or CLKAB	A or B	3.6	7	9.4	3.6	12.4	3.6	11.2	ns
$t_{PHL}$			3.9	7	9.2	3.9	11.5	3.9	10.6	
$t_{PLH}$	A or B	B or A	3.1	6	8.1	3.1	11.1	3.1	9.5	ns
$t_{PHL}$			3.7	6.8	8.9	3.7	12.1	3.7	10.5	
$t_{PLH}$	SAB or SBA $\dagger$ (with A or B high)	A or B	4.5	8.8	11.2	4.5	15.2	4.5	13.8	ns
$t_{PHL}$			3.3	6	8.1	3.3	9.8	3.3	9.1	
$t_{PLH}$	SAB or SBA $\dagger$ (with A or B low)	A or B	3.9	7.7	10.2	3.9	13.3	3.9	12	ns
$t_{PHL}$			4.7	8.3	10.8	4.7	13.7	4.7	12.9	
$t_{PZH}$	$\overline{OE}$	A or B	4	7.9	10.7	4	14	4	13.2	ns
$t_{PZL}$			4.6	8.8	11.8	4.6	15.4	4.6	14.4	
$t_{PHZ}$	$\overline{OE}$	A or B	4	7.2	9.4	4	12	4	10.9	ns
$t_{PLZ}$			3.4	7	9.3	3.4	11.6	3.4	10.5	
$t_{PZH}$	DIR	A or B	2.8	7.8	10.7	2.8	14	2.8	13.1	ns
$t_{PZL}$			3.8	8.9	11.9	3.8	15.6	3.8	14.6	
$t_{PHZ}$	DIR	A or B	3.8	8.4	10.7	3.8	13.2	3.8	12.6	ns
$t_{PLZ}$			3.2	7.3	9.9	3.2	12.6	3.2	11.8	

$\dagger$  These parameters are measured with the internal output state of the storage register opposite that of the bus input.

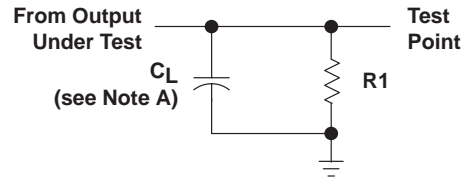
# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS037D – AUGUST 1989 – REVISED MAY 2004

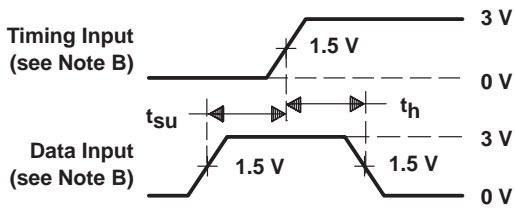
## PARAMETER MEASUREMENT INFORMATION



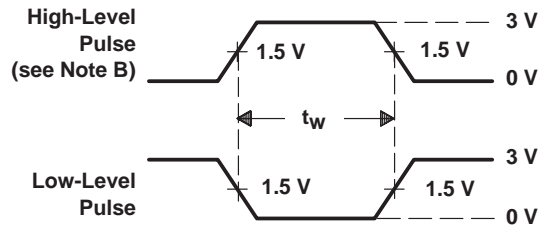
LOAD CIRCUIT FOR 3-STATE AND OPEN-COLLECTOR OUTPUTS



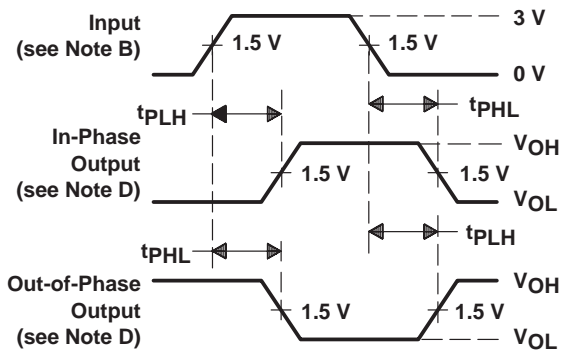
LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS



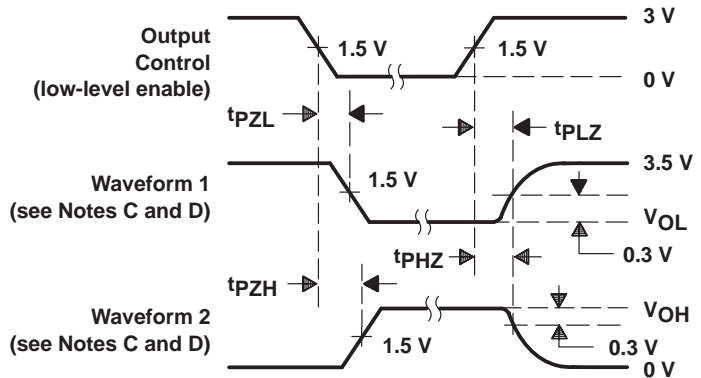
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $t_r = t_f \leq 2.5$  ns, duty cycle = 50%.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - The outputs are measured one at a time, with one transition per measurement.
  - When measuring propagation delay times of 3-state outputs, switch S1 is open.
  - All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9155501M3A	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Level-NC-NC-NC
5962-9155501MKA	ACTIVE	CFP	W	24	1	TBD	Call TI	Level-NC-NC-NC
5962-9155501MLA	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
SN74BCT646DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT646DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT646DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT646DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT646NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74BCT646NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SNJ54BCT646FK	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Level-NC-NC-NC
SNJ54BCT646JT	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
SNJ54BCT646W	ACTIVE	CFP	W	24	1	TBD	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

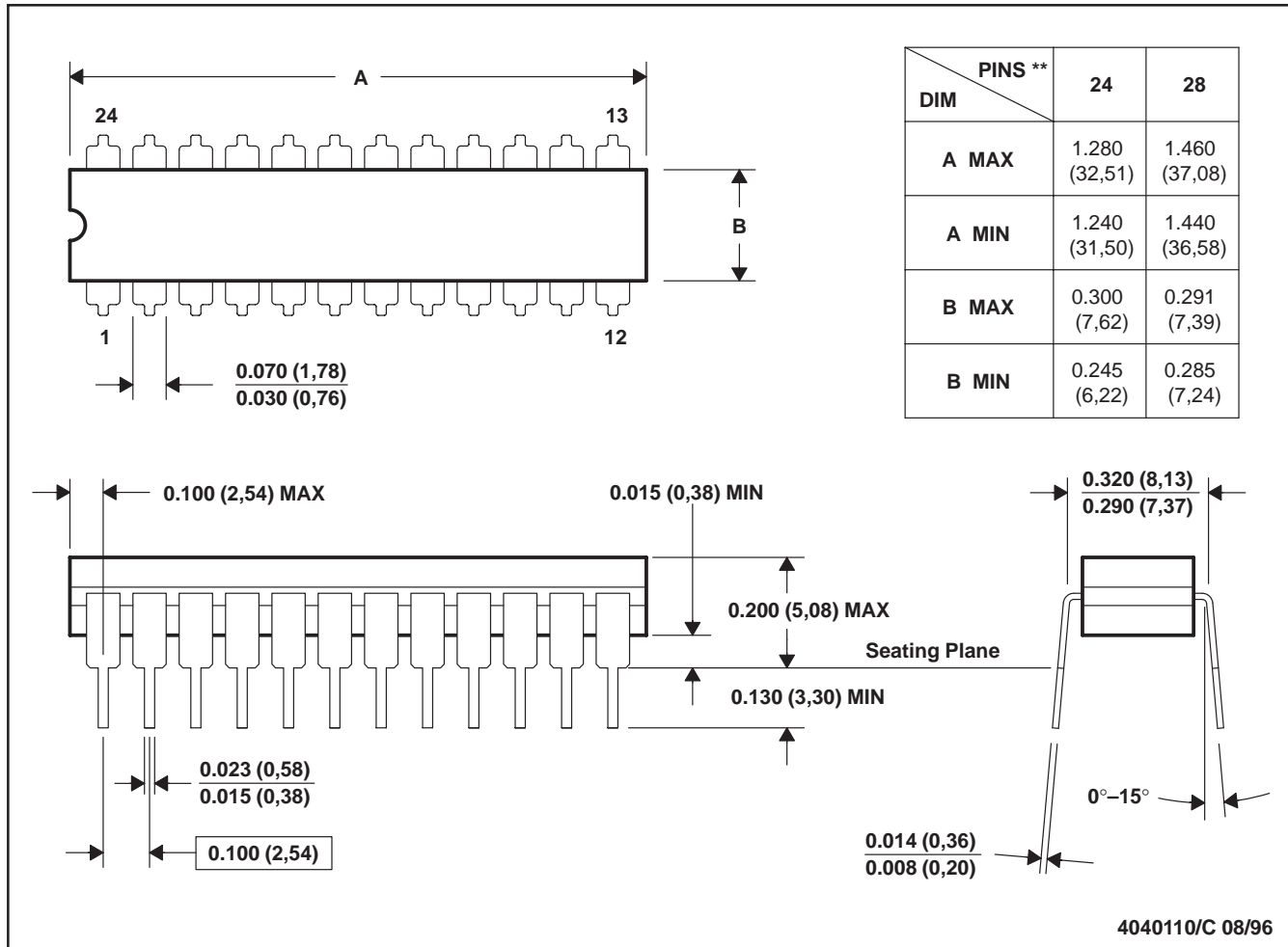
# MECHANICAL DATA

MCER004A – JANUARY 1995 – REVISED JANUARY 1997

## JT (R-GDIP-T\*\*)

## CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



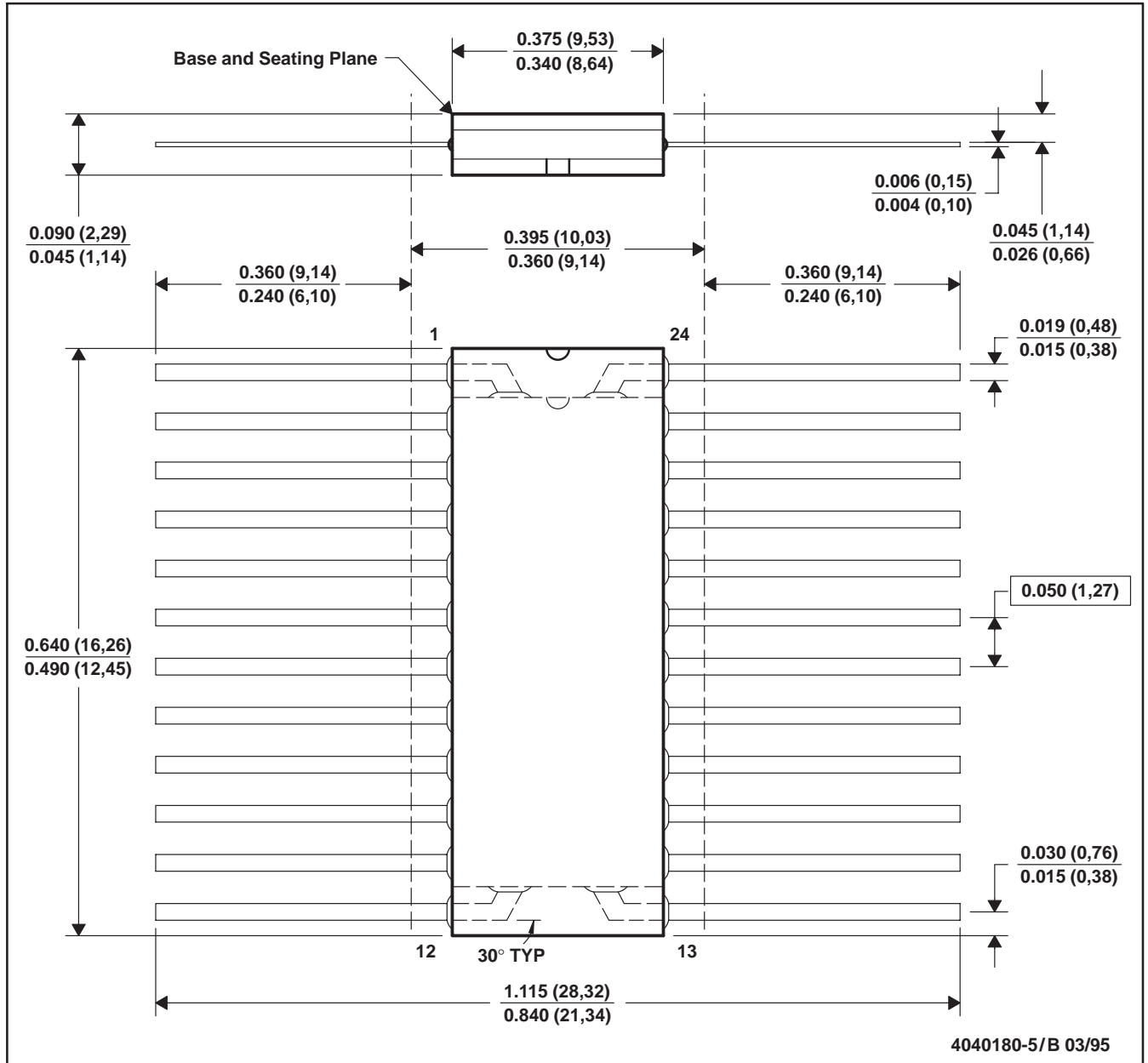
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification.
  - E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

# MECHANICAL DATA

MCFP007 – OCTOBER 1994

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
  - Index point is provided on cap for terminal identification only.

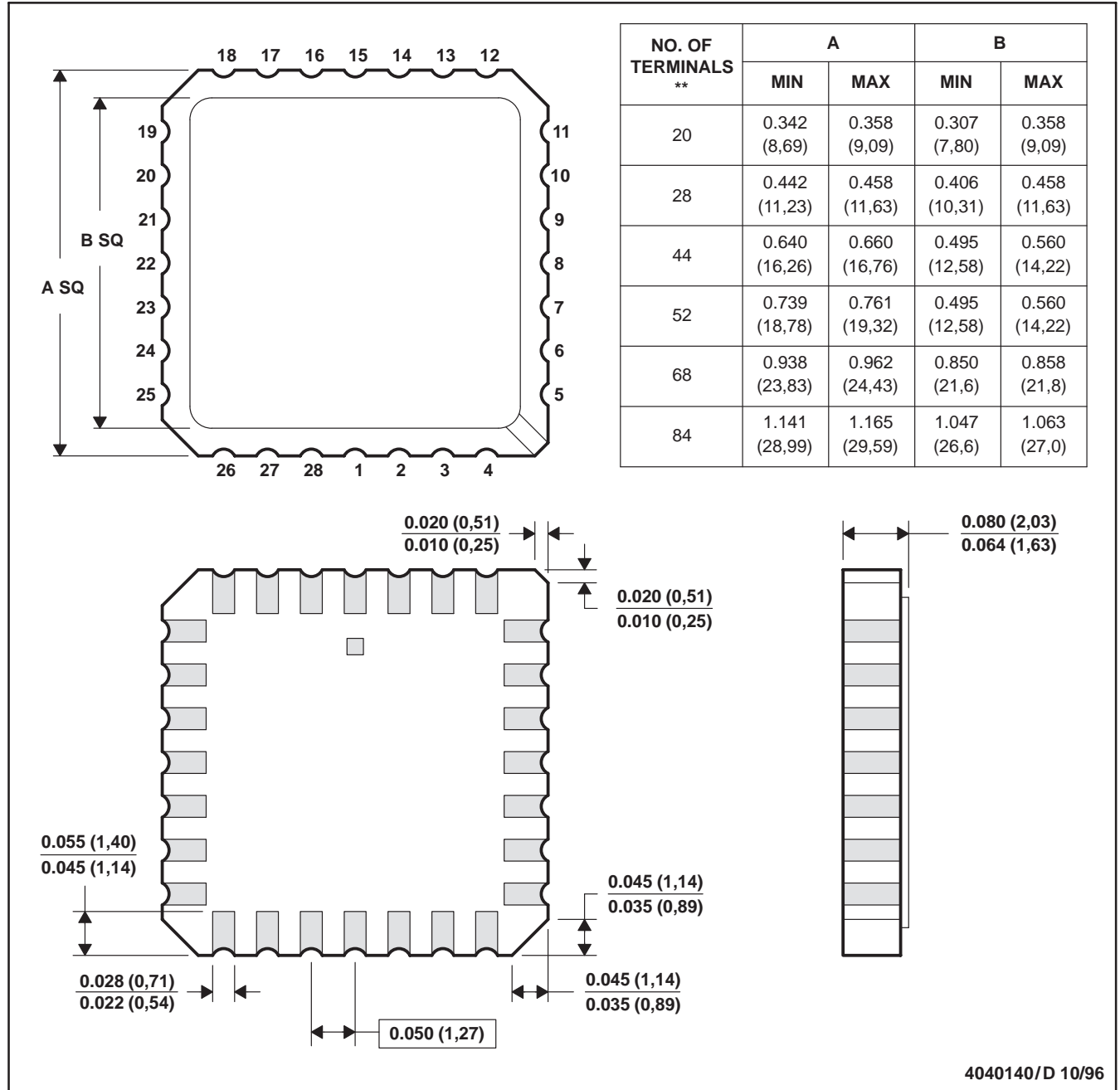
# MECHANICAL DATA

MLCC006B – OCTOBER 1996

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004

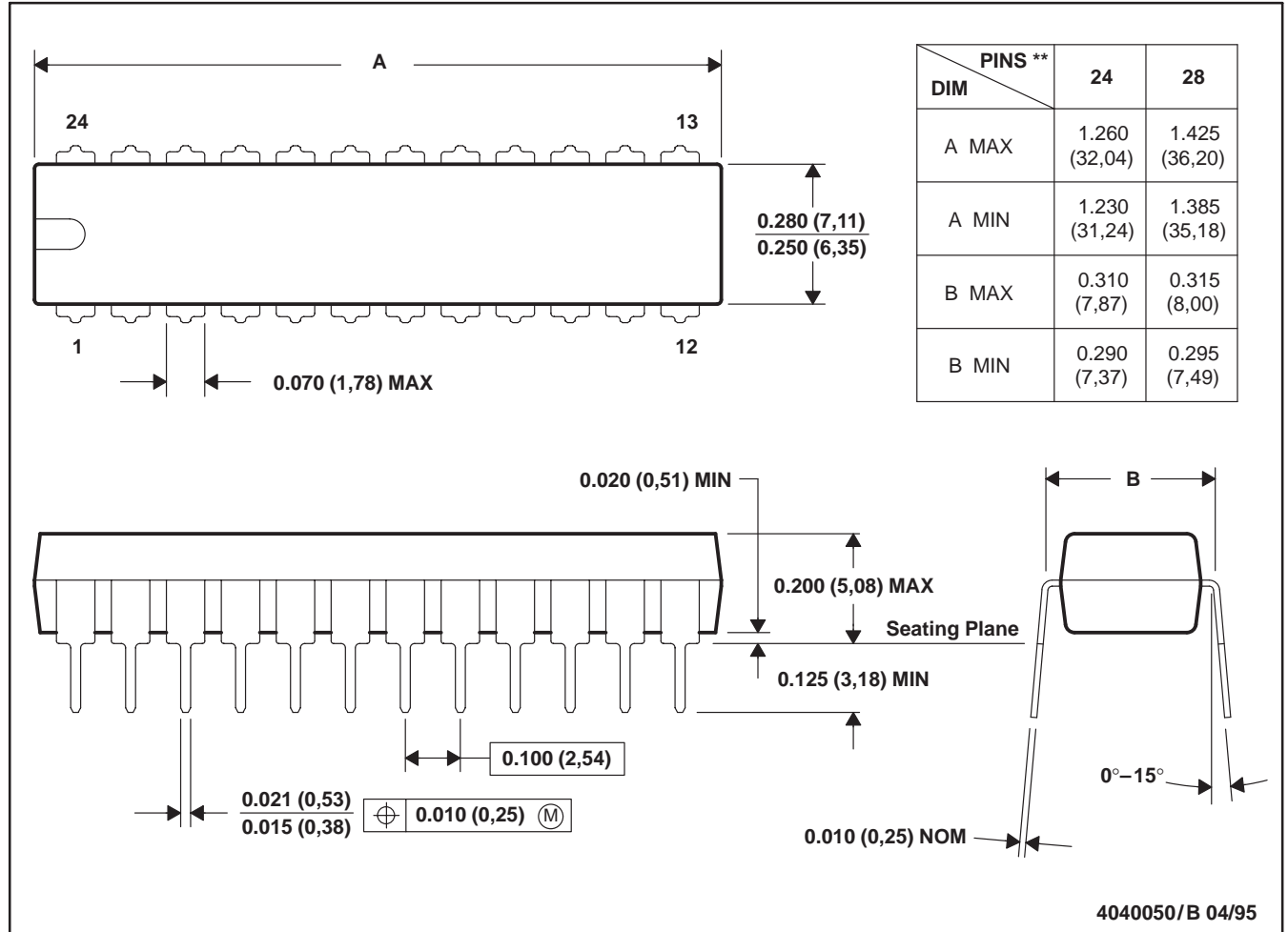
# MECHANICAL DATA

MPDI004 – OCTOBER 1994

NT (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265