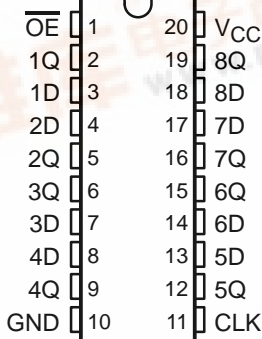


SN54BCT374, SN74BCT374 OCTAL EDGE-TRIGGERED D-TYPE LATCHES WITH 3-STATE OUTPUTS

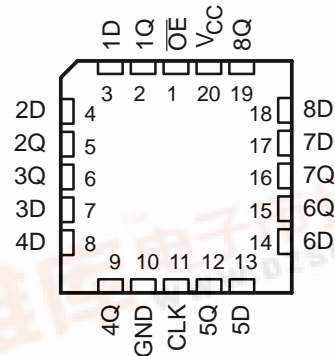
SCBS019C – SEPTEMBER 1988 – REVISED MARCH 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- Full Parallel Access for Loading
- Buffered Control Inputs
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds JESD 22 – 2000-V Human-Body Model (A114-A)

SN54BCT374 . . . J OR W PACKAGE
SN74BCT374 . . . DW, N, OR NS PACKAGE
(TOP VIEW)



SN54BCT374 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'BCT374 devices are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. The output-enable (\overline{OE}) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74BCT374N	SN74BCT374N
	SOIC – DW	Tube	SN74BCT374DW	
		Tape and reel	SN74BCT374DWR	BCT374
–55°C to 125°C	SOP – NS	Tape and reel	SN74BCT374NSR	BCT374
	CDIP – J	Tube	SNJ54BCT374J	SNJ54BCT374J
	CFP – W	Tube	SNJ54BCT374W	SNJ54BCT374W
	LCCC – FK	Tube	SNJ54BCT374FK	SNJ54BCT374FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

SN54BCT374, SN74BCT374 OCTAL EDGE-TRIGGERED D-TYPE LATCHES WITH 3-STATE OUTPUTS

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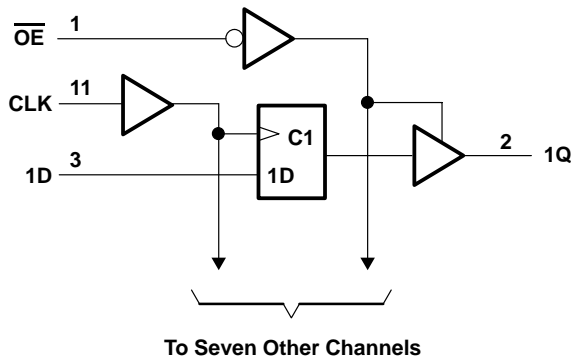
description/ordering information (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O	–0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O	–0.5 V to V_{CC}
Input clamp current, I_{IK}	–30 mA
Current into any output in the low state: SN54BCT374	96 mA
SN74BCT374	128 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54BCT374, SN74BCT374 OCTAL EDGE-TRIGGERED D-TYPE LATCHES WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

		SN54BCT374			SN74BCT374			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{IK}	Input clamp current			-18			-18	mA
I _{OH}	High-level output current			-2			-15	mA
I _{OL}	Low-level output current			48			64	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54BCT374			SN74BCT374			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.4	3.3		2.4	3.3	V
			2	3.2				
						2	3.1	
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 48 mA		0.38	0.55				V
						0.42	0.55	
I _I	V _{CC} = 5.5 V, V _I = 5.5 V			0.4			0.4	mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V			20			20	μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.5 V			-0.6			-0.6	mA
I _{OS} ‡	V _{CC} = 5.5 V, V _O = 0	-100		-225	-100		-225	mA
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V			50			50	μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.5 V			-50			-50	μA
I _{CCL}	V _{CC} = 5.5 V		37	60		37	60	mA
I _{CCH}	V _{CC} = 5.5 V		2	5		2	5	mA
I _{CCZ}	V _{CC} = 5.5 V		5	8		5	8	mA
C _i	V _{CC} = 5 V, V _I = 2.5 V or 0.5 V		6			6		pF
C _o	V _{CC} = 5 V, V _O = 2.5 V or 0.5 V		10			10		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

SN54BCT374, SN74BCT374 OCTAL EDGE-TRIGGERED D-TYPE LATCHES WITH 3-STATE OUTPUTS

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V _{CC} = 5 V, T _A = 25°C		SN54BCT374		SN74BCT374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	70		70		70		MHz
t _w	Pulse duration	CLK high		7	8	7		ns
t _{su}	Setup time before CLK↑	Data high or low		6.5	6.5	6.5		ns
t _h	Hold time after CLK↑	Data high or low		0	0	0		ns

switching characteristics (see Figure 1)

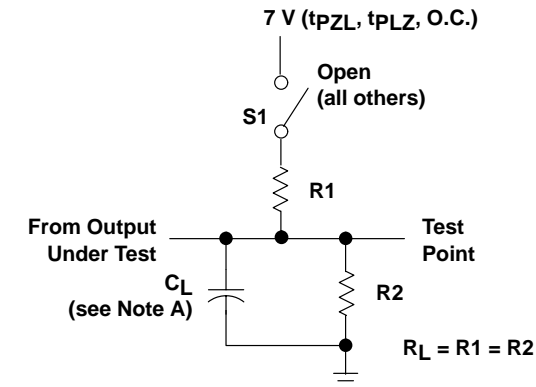
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†				UNIT
			'BCT374			SN54BCT374		SN74BCT374		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			70			70		70		MHz
t _{PLH}	CLK	Q	2	7.2	9.1	2	11.6	2	10.6	ns
t _{PHL}			2	7.1	8.8	2	10.6	2	10	
t _{PZH}	\overline{OE}	Q	1	8.3	10.1	1	12.7	1	12.3	ns
t _{PZL}			1	8.6	10.6	1	13	1	12.7	
t _{PHZ}	\overline{OE}	Q	1	4.7	6.3	1	7.1	1	6.8	ns
t _{PLZ}			1	4.8	6.3	1	7.5	1	6.8	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

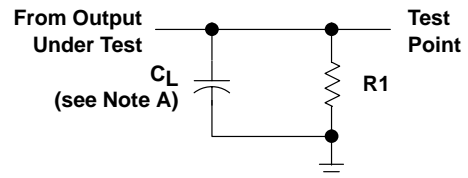
SN54BCT374, SN74BCT374 OCTAL EDGE-TRIGGERED D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS019C – SEPTEMBER 1988 – REVISED MARCH 2003

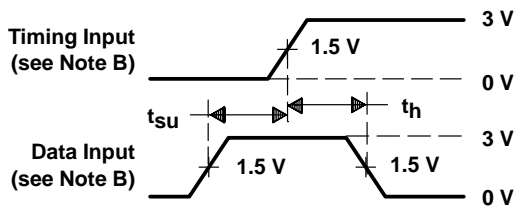
PARAMETER MEASUREMENT INFORMATION



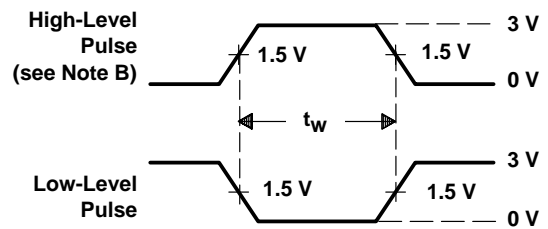
LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS



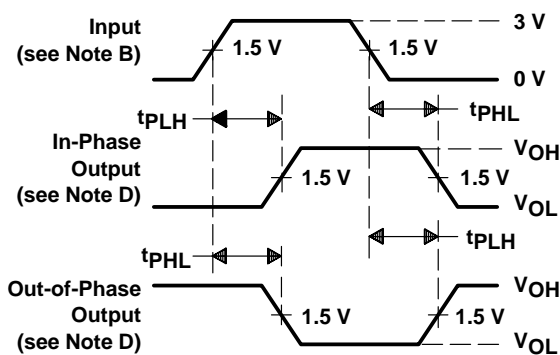
LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



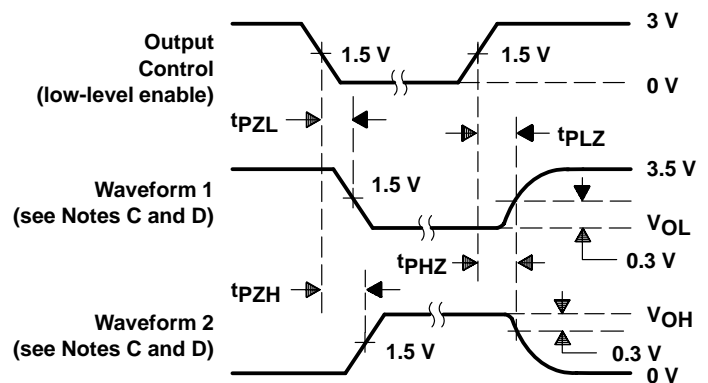
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. When measuring propagation delay times of 3-state outputs, switch S1 is open.
F. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9051601M2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
5962-9051601MRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
5962-9051601MSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SN74BCT374DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74BCT374DBR	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74BCT374DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT374DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT374DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT374N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74BCT374NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74BCT374NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT374NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54BCT374FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54BCT374J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54BCT374W	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

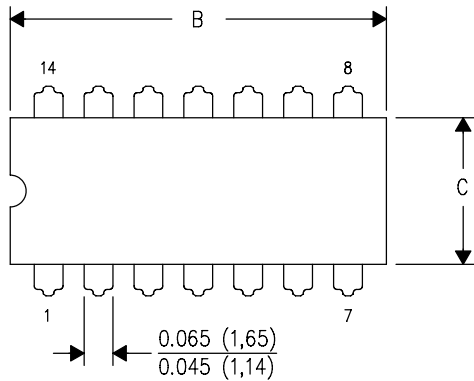
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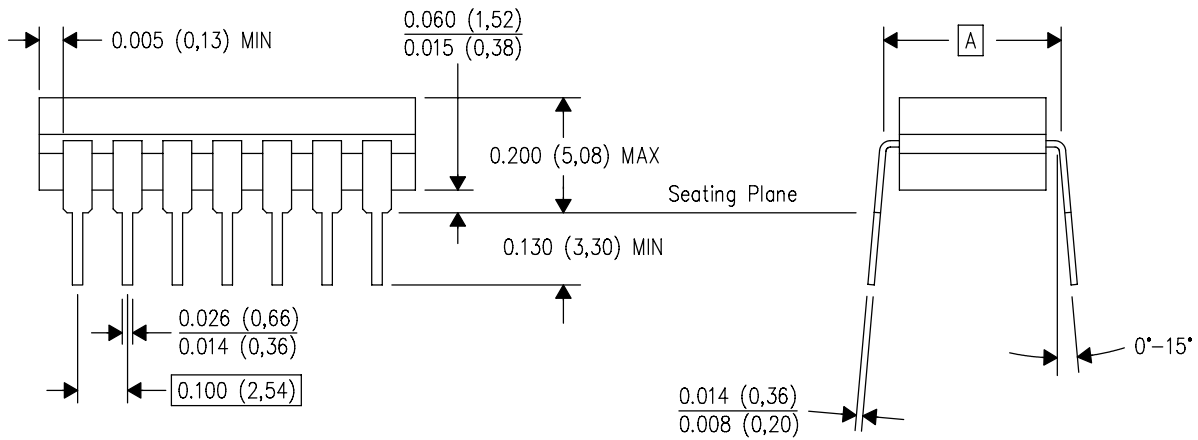
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



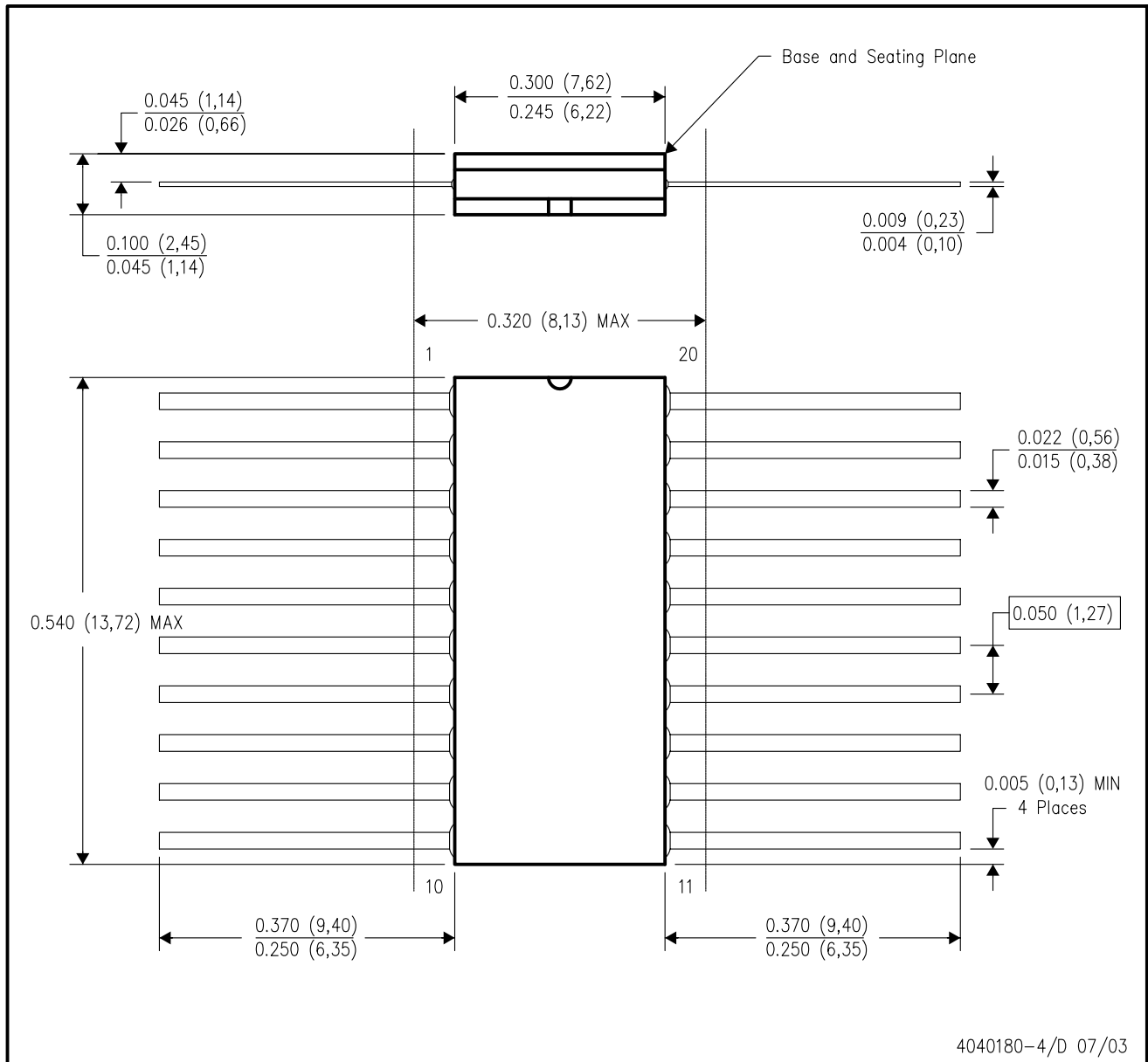
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

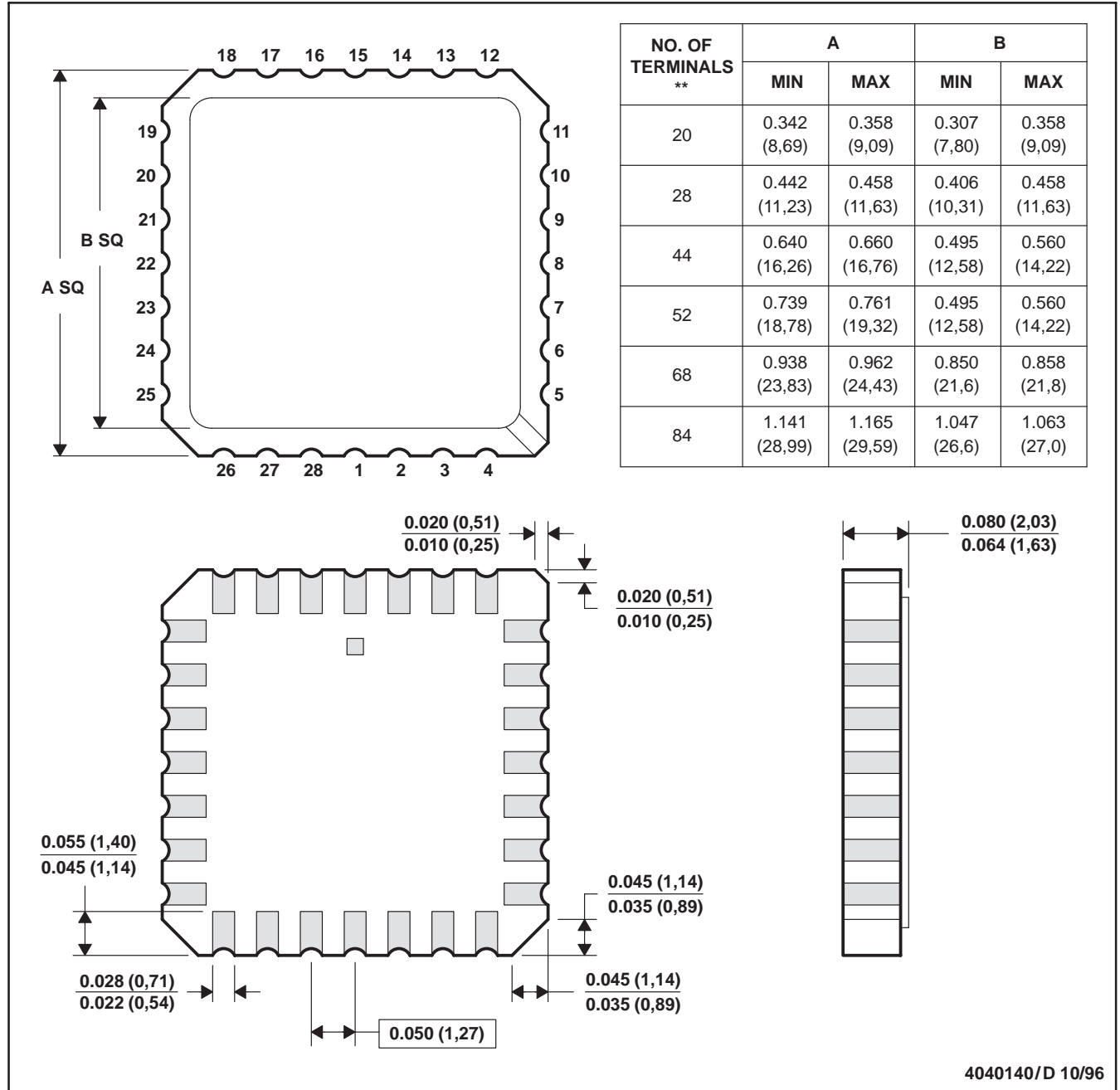
MECHANICAL DATA

MLCC006B – OCTOBER 1996

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



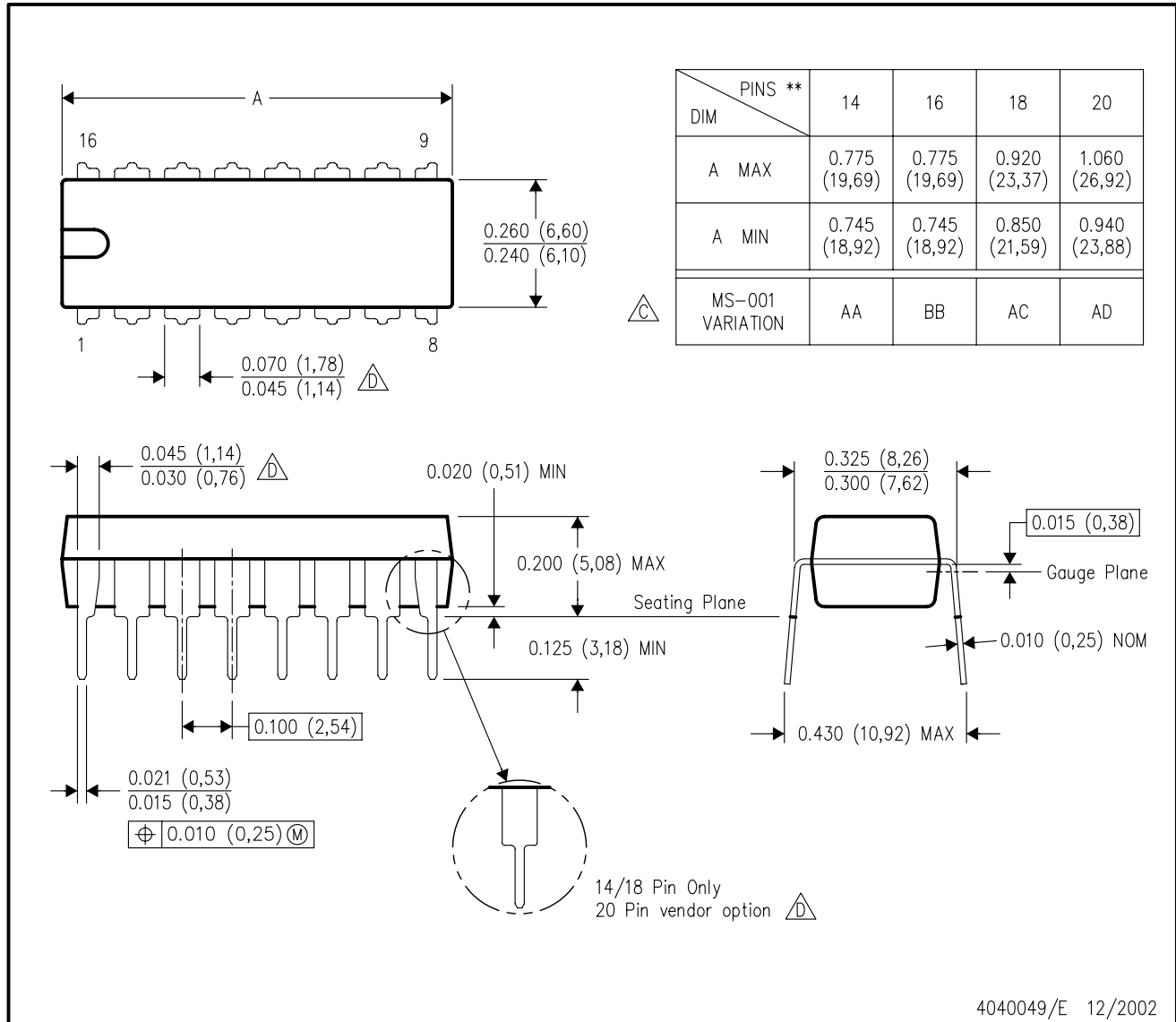
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

MECHANICAL DATA

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

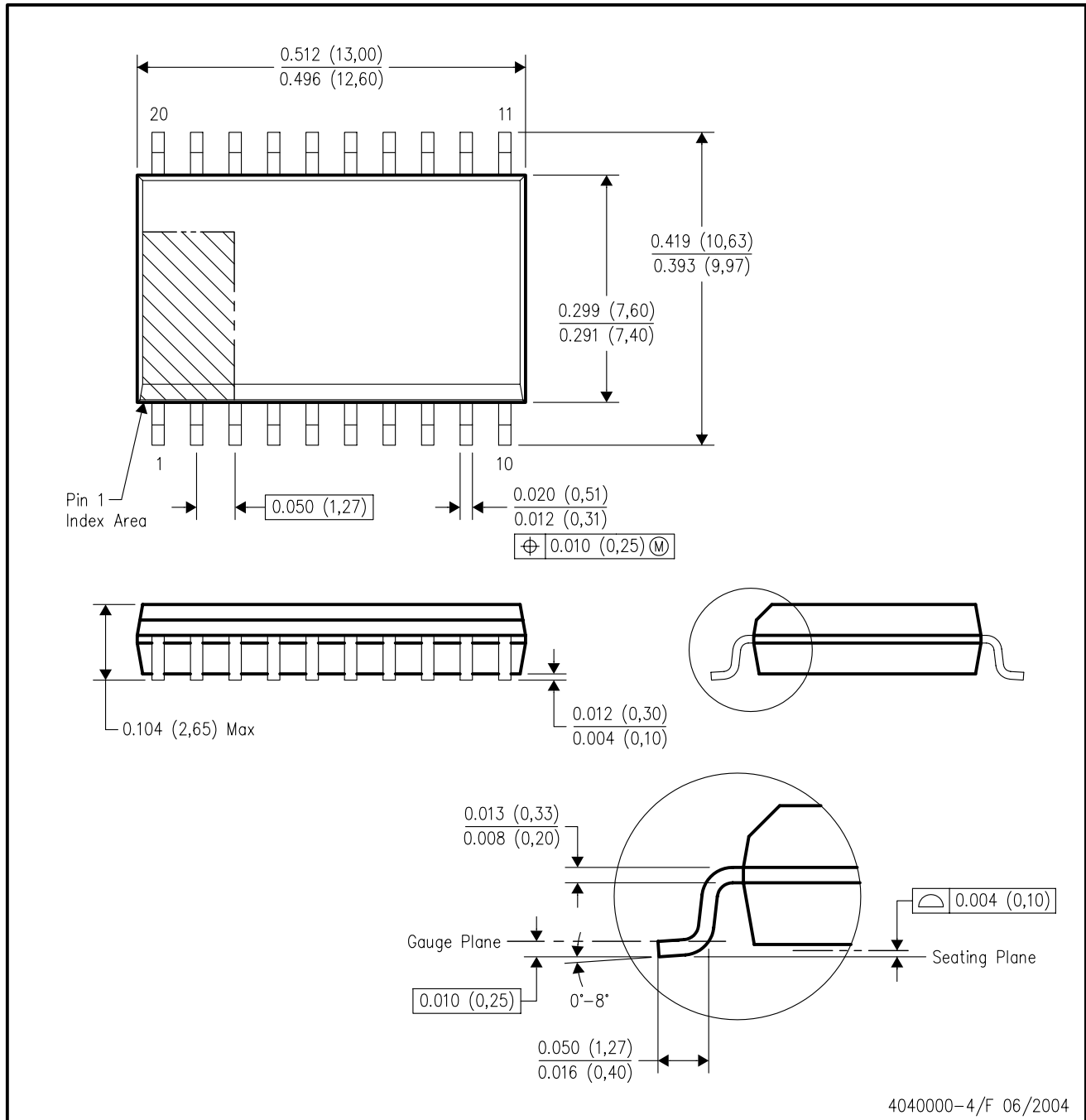


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



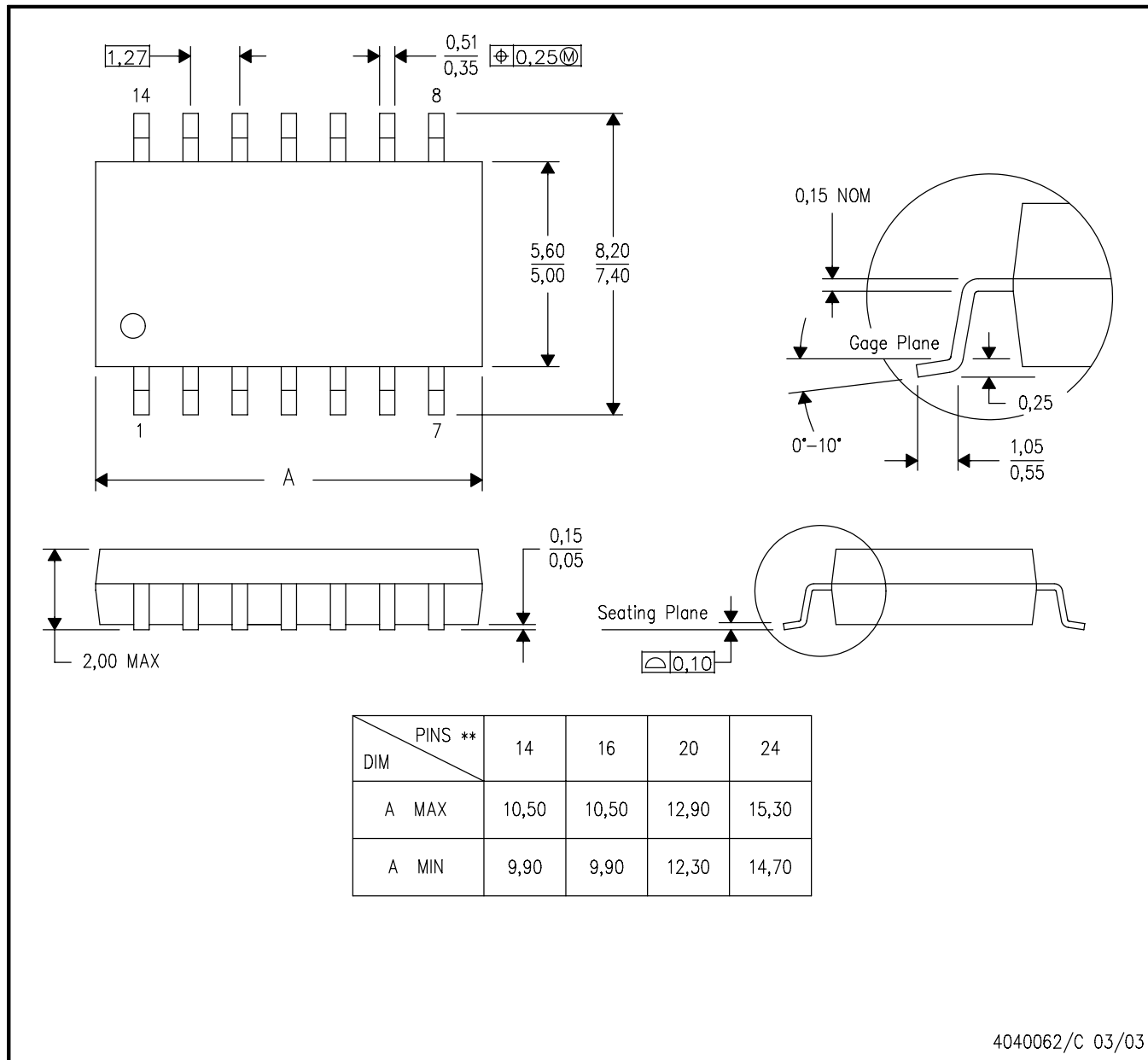
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

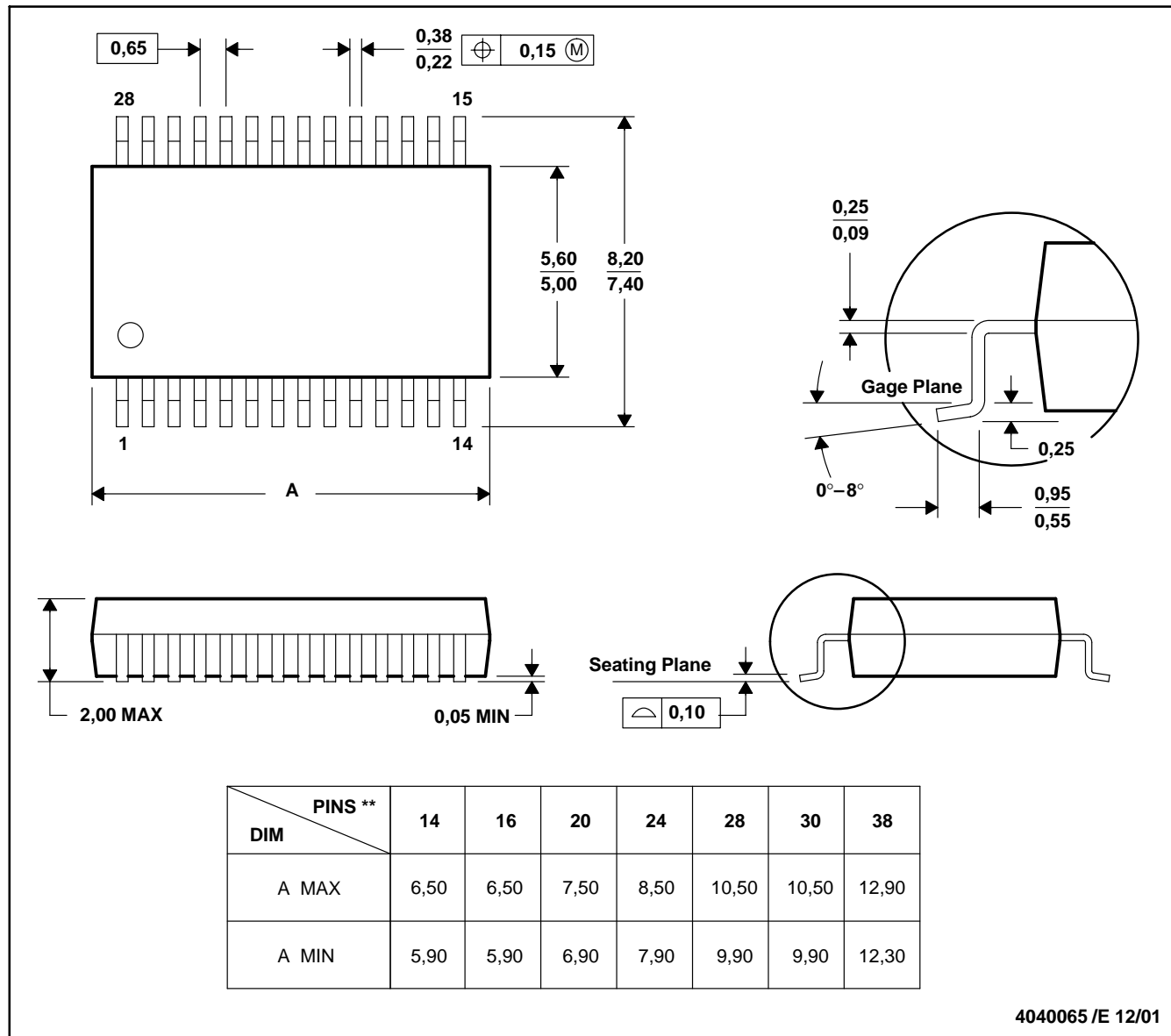
MECHANICAL DATA

MSS0002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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